Thin Film Crystalline Silicon Solar Cells

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Plan of Talk

• Introduction to Si PV
• Methods of thin film poly-Si growth
• Device results
• Developments in Si Nanowire Cells
• Conclusions
The PV Market

- PV is the most rapidly growing power generation technology.
- An estimated 17 GW of PV capacity was added worldwide in 2010
- Driven by falling costs and strong policy support

Source: REN21 report 2011
Decreasing Prices

Data from Germany shows that the installation cost per kW has halved in the last five years.

This progress has largely been driven by crystalline Si wafer technology which dominates PV with ~ 85% market share.
Crystalline Si Wafer Technology

- Based on a single p-n junction solar cell technology
- Lab efficiency record 25%
- Industrial efficiency 14-18% (>20% for Sunpower technology with rear contacts)
Thin Film Si Technology – Amorphous Si

- Cost of Si wafers is relatively high - contributes ~50% to the module cost
- This has been a driver for developing thin film approaches and reducing wafer thicknesses
- Thin film Si PV technology has been in commercial production for many years.
- It is based on amorphous Si (a-Si:H) – band gap ~1.7-1.8 eV
- Suffers from issues of low efficiency (6-7 % in production) and light induced degradation

Cell Structure (Zeman)
Deposition of Amorphous Si

+ Plasma enhanced chemical vapour deposition (PECVD)
+ Low deposition temperature
+ Cheap substrates (glass, steel, etc)
+ Large area of deposition
- Low deposition rate (1-2 A/s)

Source: Zeman
Microcrystalline Si - Micromorph Technology

- Microcrystalline (µc-Si:H) was developed to improve stability
- A mixture of nano crystalline Si grains and a-Si:H – band gap ~1.1 eV
- Micromorph is a tandem a-Si:H/µc-Si:H technology
- Approaching 10% in production (e.g. Oerlikon Solar, production cost € 0.5 / Wp)

Cell Structure (Zeman)

- Stability and performance are issues
• A fully crystalline thin film Si technology would offer all the advantages of wafer c-Si at potentially lower cost (stable operation, non toxicity, no resource constraints, etc.)

• This could be monocrystalline - e.g. thin foils produced from Si wafers or it could be polycrystalline – grown on low cost foreign substrates e.g. glass

• Challenge is to develop such a technology with efficient light trapping to overcome c-silicon’s poor absorption characteristics – Si is an indirect band-gap semiconductor!

• With light trapping potential exits for high efficiencies even in single junction thin film cells
Approaches to Thin Film Poly Silicon Growth

- Thin film poly-Si: grain sizes $\geq 1 \, \mu m$, no amorphous content
- Successful approaches fall into 2 main areas:

**Crystallisation of a-Si Layers**
- Solid phase crystallisation (SPC)
- Laser crystallisation
- Zone melting crystallisation $\rightarrow$ high temperature substrates

**Seed Layer Approach**
- Form a thin (up to few 100 nm) c-Si layer on the substrate to act as seed
- Epitaxially thicken to form absorber layer

- Growth on low cost substrates (e.g. Glass) is very challenging due to temperature constraints ($< 600 \, ^\circ C$)
Poly Silicon Growth and Devices:
Crystallisation of Amorphous Silicon
Solid Phase Crystallisation (SPC) on Glass

- a-Si layers with n+pp+ structure deposited by PECVD to thickness of ~2 µm on textured glass substrates
- Thermally anneal at ~600 ºC for several tens of hours to crystallise
- Grain sizes of the order of ~1 µm
- Defect annealing using RTA at ~900 ºC plus hydrogen plasma passivation
- Novel contact design but complex manufacturing using inkjet patterning
- Developed to pilot production stage by CSG Solar

M J Keevers et al, 22nd European PV Conf, Milan, 2007, p1783
Typical mini-module viewed from glass side, includes rows of test cells at top and bottom

- No of cells=20 cells
- Aperture area=94 cm$^2$
- Voc=492 mV/cell
- Jsc=29.5 mA/cm$^2$
- FF=72.1%
- EFF=10.4%

- Leading Poly-Si on glass thin film technology
- High density of grain boundaries and intra-grain defects limits Voc

M J Keevers et al, 22nd European PV Conf, Milan,2007, p1783
Alternative Crystallisation Techniques

• Zone-melting crystallisation (ZMC) using light sources and electron beams – requires high temperature substrates. Long history with most work on thick >20-30 µm films

• Laser crystallisation – will be discussed under seed layer approaches
Zone-Melting Crystallisation

- E-beam crystallised ~10 µm thick Si films on high temperature glass
- Grain sizes up to ~ 2000 µm in melt direction. Grain orientation [001] - [111]

Solar Cell Structure and Performance

<table>
<thead>
<tr>
<th>Voc (mV)</th>
<th>FF</th>
<th>Jsc (mA/cm²)</th>
<th>Eff (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>545</td>
<td>74.1</td>
<td>11.8</td>
<td>4.7</td>
</tr>
</tbody>
</table>

D Amkreutz et al, Prog. In PV (2011)
Poly Silicon Growth and Devices: Seed Layer Approaches on Glass

Main approaches for seed layer production:

• Aluminium induced crystallisation (AIC)

• Laser Crystallisation
Seed Layers by Aluminium Induced Crystallisation (AIC)

Normal Geometry

As-deposited: 
- a-Si
- Al
- glass

After annealing: 
- Al+Si
- Poly-Si
- glass

After surface treatment: 
- Poly-Si
- glass

Poly-Si thickness is ~100-300 nm; doped p+ with Al to ~10^{-18}-10^{19} cm^{-3}

Model:

1. Dissociation of a-Si and transport across the interface barrier
2. Diffusion of Si within the Al film
3. Nucleation of Si crystallites
4. Si grain growth – lateral growth when thickness of Al film reached
5. Al transport into the Si layer
FIB Images of Layer Exchange: Reverse-AIC

As deposited

Annealed for 5mins at 500°C

Annealed for 60mins at 500°C

Annealed for 15mins at 500°C

From Ekanayake et al, J Crystal Growth 293 (2006) 351
**Electron Backscatter Diffraction (EBSD) R-AIC**

Annealed at 500ºC for 3hrs, 2 weeks after Al deposition

EBSD orientation map in sample normal direction for ~200 nm thick poly-Si layer. Large grains are apparent. *

Mixed orientation and surface roughness can be an issue for epitaxial thickening

From Ekanayake et al, J Crystal Growth 293 (2006) 351

Inverse pole figure

AFM image. Ra=6.8 nm
Si Island Formation - Normal AIC

FIB micrograph of poly-Si film after AIC and removal of the Al matrix by a wet chemical etch

Cross-sectional TEM of a 400nm thick poly-Si film with a Si island.

- Removal of Si islands necessary prior to epitaxy. Methods include:
  - Chemical mechanical polishing (CMP)
  - Reactive ion etching

Direct Epitaxial Thickening of AlC Seed Layers on Glass

Electron Cyclotron Resonance CVD

1.7 µm thick epitaxial layer grown at ~550 °C (a) EBSD orientation map (b) inverse pole figure (c) SEM image (d) overlay of EBSD map on SEM image.

*Cross-sectional TEM micrographs showing epitaxy plus defects

Solar Cells on Seed Layers on Glass

Typical Design and Process Sequence

- Absorber thickness ~1.5 - 2 µm
- Growth temperature up to ~600 °C
- Hetero-junction emitters
- Defect annealing by RTA at ~900 °C
- Defect passivation by hydrogen discharges
- Small areas (up to ~ 1 cm²)
- No advanced light trapping

Rau et al, 21st European PV Conf. September 2006, Dresden, p1418
## Typical Solar Cells Results on Glass

<table>
<thead>
<tr>
<th>Method of epitaxial thickening</th>
<th>Cells on seed layers</th>
<th>Ref cells on Si wafers</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Voc (mV)</td>
<td>FF (%)</td>
</tr>
<tr>
<td>Solid Phase Epitaxy¹</td>
<td>437</td>
<td>55.9</td>
</tr>
<tr>
<td>Ion-assisted deposition²</td>
<td>420</td>
<td>45.9</td>
</tr>
<tr>
<td>ECR CVD³</td>
<td>397</td>
<td>57.0</td>
</tr>
<tr>
<td>E-beam evaporation⁴</td>
<td>407</td>
<td>67.0</td>
</tr>
</tbody>
</table>

- Performance limited by material quality and cell design
- Defect densities up to ~10¹⁰ cm⁻²
- E-beam deposited layers give better performance due to less defects

Seed Layers by Laser Crystallisation

- Laser crystallisation of thin a-Si layers has been an active field for many years driven by TFT/display market
- Excimer laser crystallisation (ELC) gives randomly oriented grains of up to ~1 µm in size
- Large grained material has been produced by scanning line focussed laser beams. Recent results include Andra et.al:
  - CW diode laser at 806 nm → grains exceeding 100 µm in 400 nm thick a-Si starting layers
  - Green pulsed laser at 515 nm → grains exceeding ~10 µm in 60 nm thick a-Si starting layers
- These approaches give mixed orientation grains
- **Device results** - SPE of e-beam deposited a-Si on seed layer, CSG Solar contacting technology → efficiency of 4.9% in a 12 cell minimodule.
Mixed Phase Solidification (MPS)

- Results for 130 nm a-Si film on SiO₂ processed by scanning a linear, 532 nm CW laser beam. Scan speed 1.5 cm/s

(a) SEM of heavily defect-etched sample
(b) EBSD map showing (100) texture
(c) TEM of lightly defect etched sample. High film quality can be seen

- Early cell results - 5.4% efficiency achieved using thermal CVD on a glass ceramic substrates. Highest Voc was 530 mV. Potential for improvement

J S Im et.al. J Crystal Growth 312 (2010) 2775
High Temperature Seed Layer Approaches

• Exemplified by work of IMEC group
• Poly-Si seed layers (250 nm thick) by AIC on high temperature substrates e.g. alumina coated with flowable oxide
• Epitaxial thickening by thermal CVD at ~1100 ºC (dep rate 1.4 µm/min)
• Inter-digitated structure with heterojunction emitter on a 2-3 µm thick p-type absorber layer
• Remote plasma hydrogen defect passivation
• Plasma texturing plus ITO ARC for improved light capture

Average grain size ~5 µm
Maximum grain size ~15 µm

Solar cell structure - surface texturing not shown

Aperture area = 1 cm$^2$
J$_{sc}$ = 21.6 mA/cm$^2$
V$_{oc}$ = 522 mV
FF = 75.8 %
Eff = 8.5%

- Voc of cells ~ independent of grain size varying from ~0.2 – 50 µm
- Performance limited by a high density (~10$^9$ cm$^{-2}$) of intra-grain defects in seed layer or interface with epitaxial layer

Monocrystalline Seed Layers + Thermal CVD

- Demonstrate potential of seed layer approach
- Exemplified by work of IMEC group.
- Seed layer creation by transfer of 300 nm thick, (100) monocrystalline layers onto transparent glass ceramic substrates using implant-induced separation and anodic bonding (Corning process)

Schematic of Corning’s Si on glass process (glass ceramic substrate)

Device Processing and Results

- Epitaxial thickening by thermal CVD followed by cell processing at IMEC
- 2 µm of \( p^+ \) (~5x10^{19} \text{ cm}^{-3} ) BSF layer followed by 2-8 µm of \( p \) Si \( (10^{16} \text{ cm}^{-3}) \)
- Typical defect density in epitaxial layers is \~10^5 \text{ cm}^{-2} \) compared to \~10^9 \text{ cm}^{-2} \) for AIC layers

<table>
<thead>
<tr>
<th>Initial thickness</th>
<th>8 µm</th>
<th>4µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voc (mV)</td>
<td>598</td>
<td>613</td>
</tr>
<tr>
<td>Jsc</td>
<td>24.3</td>
<td>19.9</td>
</tr>
<tr>
<td>FF (%)</td>
<td>74</td>
<td>73</td>
</tr>
<tr>
<td>EFF (%)</td>
<td>10.8</td>
<td>8.9</td>
</tr>
</tbody>
</table>

Results for 1cm\(^2\) cells for different starting absorber thicknesses. No advanced light trapping or back reflector used

From Gordon et. al. Solar Energy Mat Solar Cells 95 (2011)S2
Silicon Nanowire Cells

- Effective light trapping is essential to realise the full potential of thin film poly-Si solar cells
- Conventional methods based on µm scale texturing used in bulk Si solar cell technology cannot be used
- Advanced designs being researched for planar thin film solar cells include the use of nanotextured substrates, photonic crystals and plasmonic structures
- New designs based on radial junctions in micro and nano wires also being investigated for enhanced light trapping
Radial Junction Si Wire Array Cells

- Radial junction geometry decouples length scale of light absorption from that of charge collection.
- Reduced reflection, excellent light trapping
- Short minority carrier collection path → reduced requirements for material purity
- Increased defect tolerance
- Facile strain reduction
- Band-gap tuning in quantum wires
- Fabrication directly on low-cost substrates
- Maximum efficiency not expected to increase above standard limits but above 17% predicted with efficient surface passivation

Methods of Wire Formation – Top Down

- Various approaches – based on patterned or non-patterned etching
- One example:

  Dip coat *n-type* silicon in silica bead solution

  Deep reactive-ion etch (DRIE) to form nanowires

  Remove beads in HF and diffusion dope to form radial *p-n junction*

Bottom-up Growth: Vapour Liquid Solid (VLS) Process

- VLS requires a metal catalyst particle as a site from which to nucleate growth.
- Particles can be formed by self assembly and other techniques.
- A feedstock gas such as SiH$_4$ is used.
- The feedstock gas saturates the particle resulting in precipitation of Si at the liquid solid interface giving wire growth.
- Catalyst metals used include Au, Sn for growth at low temperatures (<600 ºC) and Cu which requires high temperatures (~1000 ºC).
- Vertically aligned single crystal wires can be grown with diameters up to few 100 nms.
Si Nanowire Array Growth At LSBU Using Bottom-Up Approach

- We are studying bottom-up growth using the VLS process.
- Au and Sn have been studied as the catalyst particles.
- Particles formed by self assembly – annealing and surface tension induced agglomeration.
- Wire growth is carried out using a variant of plasma CVD called ECRCVD.
- Silane is used as the precursor for Si growth with phosphine as n-type dopant.
Electron Cyclotron Resonance Chemical Vapour Deposition (ECRCVD)

- ECR is a variant on plasma CVD with the addition of a magnetic field of 875 gauss subjecting the remote 2.45 Ghz plasma to a self limiting electron resonance.

- The plasma stream cracks the feed stock gas allowing deposition at lower substrate temperatures than CVD.

- A DC self bias can be created across the substrate with the aid of an applied RF signal.
3 nm Au catalyst layer thickness showing vertical growth on Si (111) wafer substrate. Growth temperature ~520°C. Top with RF bias

- Wire diameter typically ~300 nm, length ~1200 nm
- Some tapering due to side wall deposition

Raman spectra of wires showing single crystalline growth. Confirmed by EBSD
SiNW Reflectance

- Higher wire densities exhibit a lower reflectance.
- Growth of SiNWs on Si (100) occurs at an angle of 32.5° to the substrate.
- Angled growth gives the lowest reflectance.
• SEM image of an initial 12nm thick Sn film annealed on Si (111) wafer.

• SiNW diameter has a dependency on catalyst particle diameter.

• Initial catalyst particle size varies with layer thickness and substrate orientation.
Sn Catalysed Growth on Si Wafers

- Sample grown from 6nm initial Sn layer on Si (111). Growth temperature ~380°C
- No catalyst particle remains on the tip
- Orientation variable, rough surfaces
- Wires show conical growth rather than parallel growth.

- Samples grown at ~380°C, 6sccm SiH₄, MW power 800W.
- Density of samples drop with increase in initial layer thickness.
SiNW Growth Versus Sn Layer Thickness

- Increasing Sn layer thickness from 6 to 12nm increases length and diameter

- Increasing initial layer thickness to 24nm decreases SiNW length

- No correlation between initial particle diameter and wire diameter.
Sn Catalysed SiNWs on glass

- Absorption taken as 1-T-R.
- Different initial catalyst thicknesses give differing absorption spectra.
- Significant increase in absorption compared to planar layer on its own

A Glass SiNW stack

B SiNW on glass substrate
Sn 6nm~380°C, 6 sccm SiH₄
Conical wires better absorption characteristics

Zhu et. a. Nano Lett,9 (2009), 279
Low Temperature Bottom-Up Wire Growth Solar Cell Status

- Substrates include Si, glass, metal foils
- Wire lengths up to ~ a few µm, diameters typically < 1 µm
- Work on fully crystalline wire cells is at an early stage with typical efficiencies:
  - ~1-2% using VLS growth on glass and other substrates
- Up to ~5% achieved using a hybrid a-Si/c-Si structure
Hybrid c-Si/a-Si Nanowire Cells on Glass

Over $10^6$ NWs/cell

JCho, B O'Donnell, L Yu, K Kim, I Ngo, P Roca i Cabarrocas, Prog. In PV in press
(a) VLS-growth of p-type Si microwire arrays using SiCl$_4$/BCl$_3$ at ~1000 °C; (b) catalyst removal and growth of thermal-oxide diffusion-barrier; (c) selective removal of the oxide barrier using a polymer-infill etch mask; (d) thermal diffusion of radial p–n junctions. (e) SEM images of a microwire array following step (d)

Si wire-array solar cell performance using long wires grown at high temperatures

- Growth temperature ~1000 ºC using a Cu catalyst
- Wire length ~50 µm, diameter 2-3 µm on a 7 µm pitch
- Champion cell: Voc=498 mV; Jsc=24.3 mA/cm²; FF=65.4%, Eff=7.9%

Top Down Wire Formation on Si Wafers

• Jia et. al. (Solmat, 96 (2012) 226)
• SiNW prepared by etching n-type Si wafer using AgNO$_3$ and HF solution
• Diameter tens of nm to 300 nm, length ~900 nm
• Deposition of intrinsic and p-type a-Si by PECVD followed by TCO for top contact

• Best efficiency ~7.9%
Conclusions

• Solid phase crystallisation of amorphous Si films is still the most successful thin film poly-Si on glass technology (up to ~10% efficiency in minimodules).
• Seed layer approaches on glass give large grain sizes but efficiencies are < 5% due to material quality issues and simple cell designs without light trapping.
• Efficiencies of up to 8.5% using AIC seed layers and 11% using monocrystalline seed layers have been achieved on foreign substrates.
• With the use of advanced light trapping schemes such as plasmonics and further developments in device engineering (e.g. tandem structures) it should be possible to progress towards efficiencies of 15% and beyond.
• Translating this to glass substrates will continue to provide significant research challenges and opportunities.
• Work on nano/micro wire solar cells is at an early stage but shows promise. Again, there are significant research challenges and opportunities.