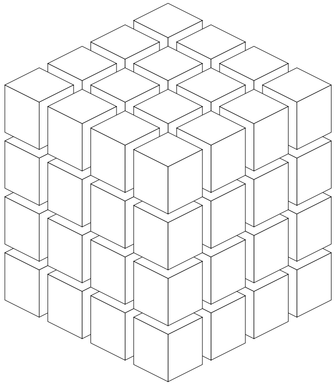
# Cray T3D & T3E

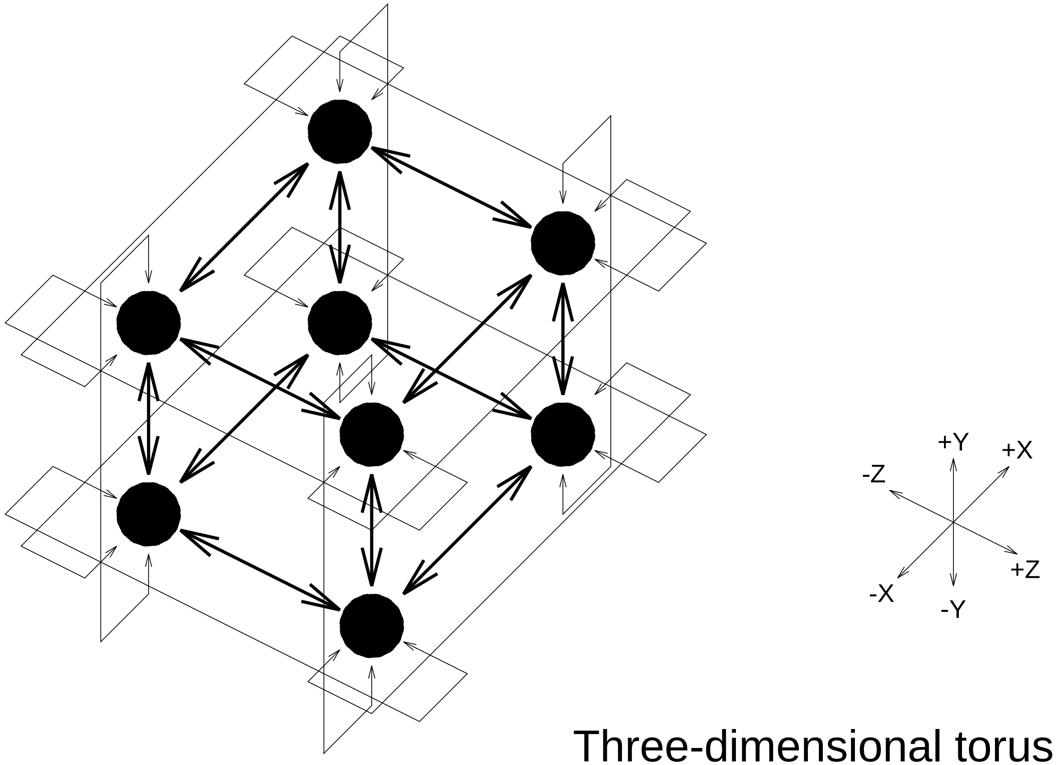
## Cray's Massively Parallel Processors



Up to 2048 PEs

| | | T3D | T3E | T3E-1200 | |
|---|---|---|---|---|---|
| Each PE is | DEC Alpha | 21064 | 21164 | 21164 | |
| | capable of | 150 | 600 | 1200 | MFlops |
| Total: | | 0.3 | 1.2 | 2.5 | TerraFlops |

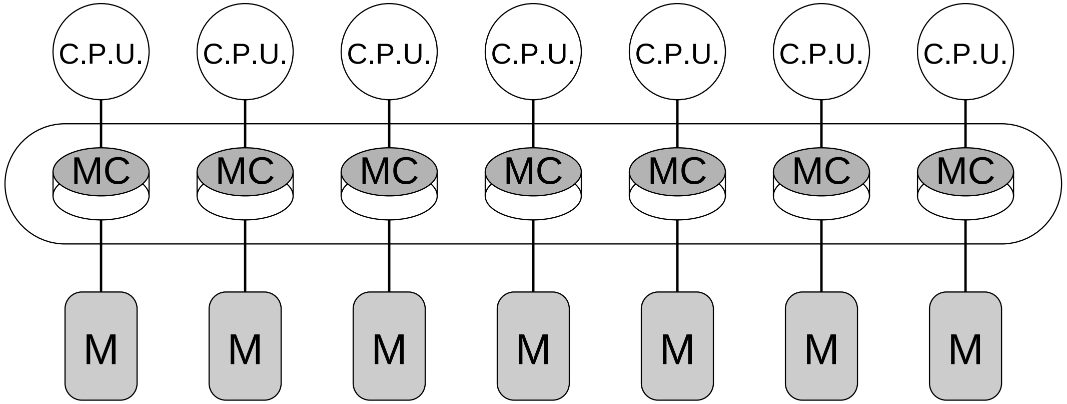
# Cray T3D & T3E - Network



Three-dimensional torus network

- Fixed Valency nodes ($v = 6$)
- Torus provides redundancy for fault-tolerance.
- Good geometric mapping for $3D$ finite element problems

# Cray T3D & T3E



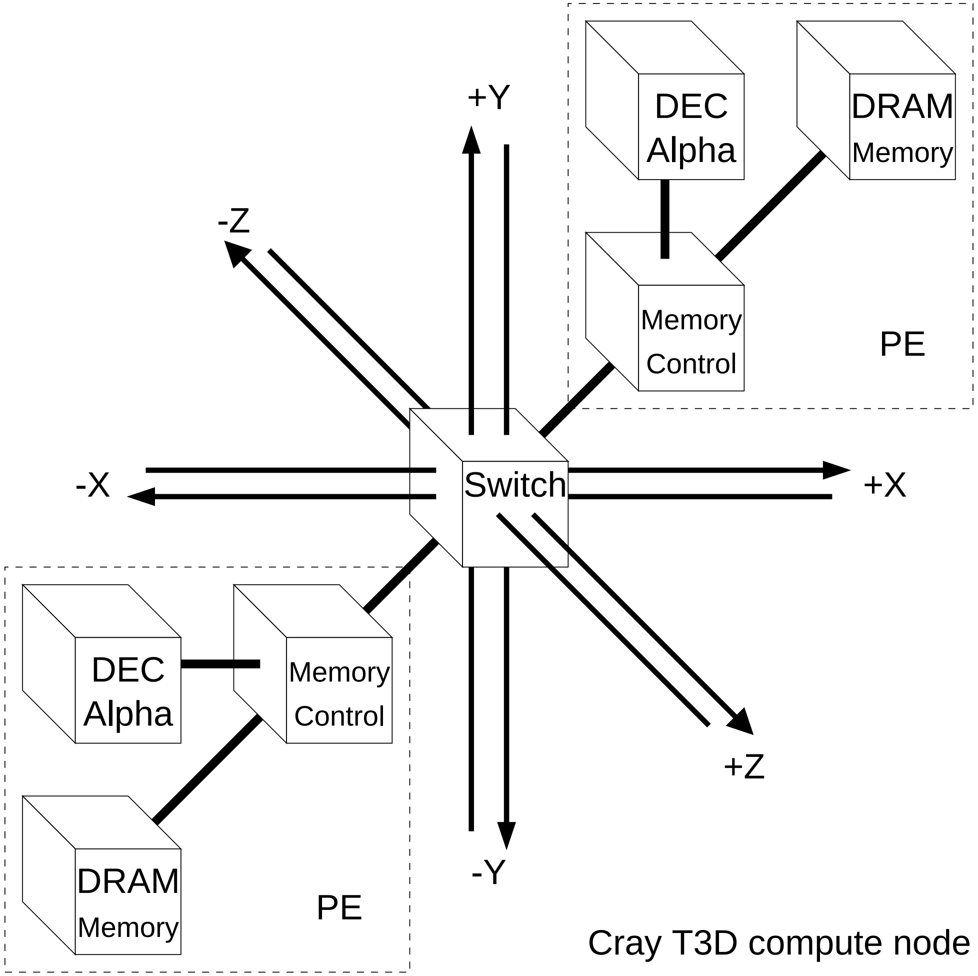
- Memory arrangement – *Shared Distributed Memory*
  - Physically Distributed

    Each processor has it's own local memory allowing for fast access without network delays.
  - Logically Shared

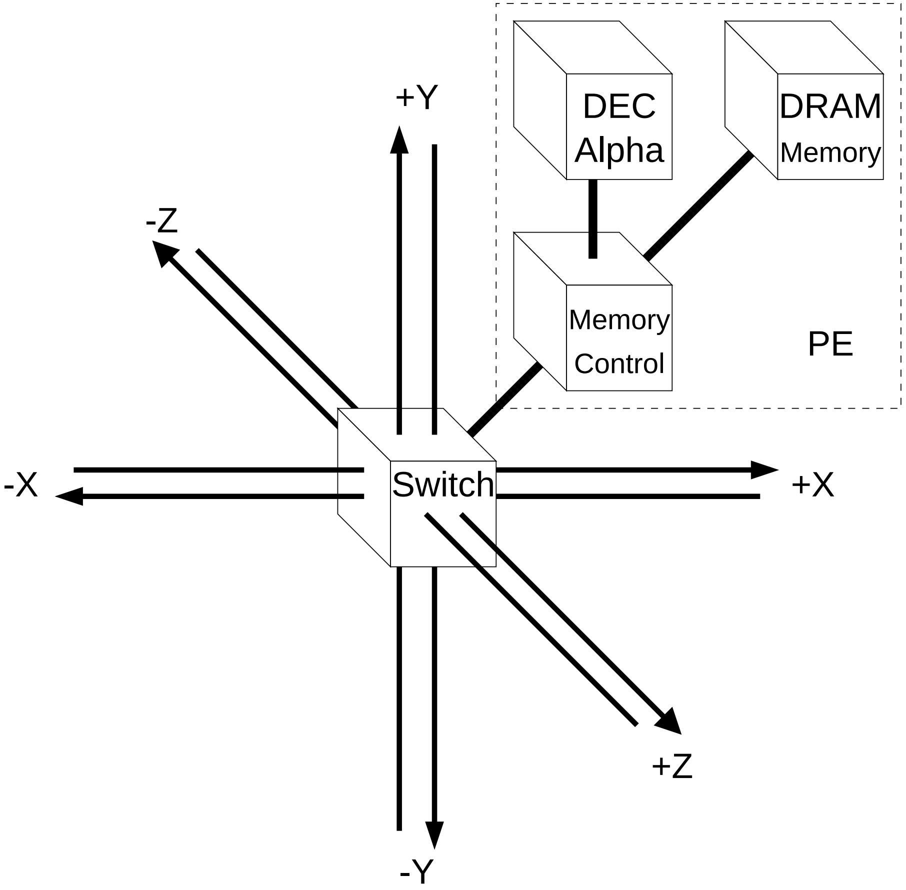
    Single global address space.

    A C.P.U. may access data from any block of memory. Non-local accesses are detected by the memory controller. Access is completed via the network which interconnects the memory controllers.

# Cray T3D & T3E



Cray T3D compute node



Cray T3E compute node

## Node Architecture

- DEC Alpha
  - Standard component.
  - Fastest available RISC microprocessor – 64 bit, Superscalar and Superpipelined.
  - For T3E – T3E-900 – T3E-1200 the only difference is the processor.

- Network
  - Direct network of nodes.
  - 1 or 2 PEs per node sharing a packet routing switch.
  - Data Channels are 16 bit parallel.

Cray T3E

## Scalability

- Bisection Bandwidth

  Increases as $p^{2/3}$

  Slightly less than linear but doesn't suffer from the problems of building large machines with truely scalable bisection bandwidth

  - Hypercube – increased node cost
  - Fat Tree – increased proportion of routing nodes

- Actual Machines

  - Machines have been built with between 6 and 1324 PEs although at $630,000 the 6 processor T3E-1200 may not represent good value for money.

| | T3D | T3E | T3E-900 | T3E-1200 | |
|---|---|---|---|---|---|
| No of PEs | 1024 | 1084 | 1324 | 1084 | |
| Theoretical Peak | 152.0 | 650.4 | 1191.6 | 1300.8 | GigaFlops |
| Measured (Linpack-MP) | 100.5 | 448.6 | 815.1 | 891.5 | GigaFlops |
| Year | 1994 | 1998 | 1997 | 1998 | |

## Programming Paradigms

- *Shared Memory Model*

  *Shared distributed memory* allows for shared memory code to be written.

  In order to gain maximum performance data must be carefully placed.

- *Communicating Processes Model*

  The network may be used for explicit message passing.

  Cray supports message passing versions of both C and Fortran

- *Data Parallel Model*

  The network supports synchronization to help with SIMD style computation.

  Cray's CRAFT Fortran includes Fortran 90 array syntax.