I3T25 (0.35 um) Design Rules

1000115 Rev: E

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I3T25 (0.35 um) Design Rules

Owner: Technology Research & Development

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Revision History

Revision	Requestor	Release Date	Description
E	IS	03-May-2010	• Updated Layout Rules ○ Exceptions for specific components (Schottky diode, pipc and DMOS') page modified to reference DES-0005 ○ Deleted HVROUTE rules: The layout concept never developed ○ DSEDN rule change Description - 1, 10 Min space – 7 Deleted – 11 ○ DSNDN rule change Description – 1, 2, 3, 4, 5, 6, 7, 8, 10, 11, 13 New rule – 15, 16, 17, 18 ○ SSEDN rule change Min space – 13 Deleted – 8, 10 ○ SSEDP rule change New rule – 15 ○ SSNDN rule change Description – 13 Min space – 11 Deleted – 10, 15, 16 ○ SSNDP rule change New rule – 18, 22 ○ DSEDP rule change Description – 1, 16, 20 Min spacing- 11 Deleted – 12, 13 New rule – 16 ○ DSNDP rule change Description – 16, 20 ○ DSEDPTN rule change New rule – 1 through 13 ○ Poly2 rule change Description – 11.3, 11.8, 11.9, 11.10, 11.11, 11.13 • Updated Process Info ○ Updated technology features including think gate option ○ Added dual gate process description • Updated Electrical Design ○ Added HV DMOS transistors overview ○ Added DMOS electrical parameters ○ Added schottky information ○ Added pipc information • Updated Safe Oper Area ○ Added thick gate DMOS SOA information
D	SS	02-Oct-2008	• Added 9 new DG devices: 1. POLY2 (11)

			2. NDMOS Thick-Gate Single-Sided Extended-Drain (LFNDM25T) 3. PDMOS Thick-Gate Single-Sided Extended-Drain (LFPDM25T) 4. NDMOS Thick-Gate Double-Sided Extended-Drain (LFNDM25DT) 5. PDMOS Thick-Gate Double-Sided Extended-Drain (LFPDM25DT) 6. NDMOS Thick-Gate Single-Sided Nested-Drain (LFNDM20NT) 7. PDMOS Thick-Gate Single-Sided Nested-Drain (LFPDM20NT) 8. NDMOS Thick-Gate Double-Sided Nested-Drain (LFNDM20DNT) 9. PDMOS Thick-Gate Double-Sided Nested-Drain (LFPDM20DNT) • Added 3 new I3T25 Specific rules 8.2, 19.7, 99.15 • Documented exceptions of new I3T25 DG rules from 1000115 and DES-0005 • Deleted duplicate rule 50.14 • PTN25.8 description wording updated to add 'if abutted with source active' • Rule Name number change made to rules to avoid confusion with I3T80 1. PWIMP: a. 50.5 changed to 50.17 b. 50.8 changed to 50.19 c. 50.9 changed to 50.20 d. 50.10 changed to 50.23 e. 50.15 changed to 50.24 2. PFIELD: a. 49.7 changed to 49.16 b. 49.8 changed to 49.17 c. 49.9 changed to 49.18 3. N-WELL Resistor: a. NWR.2 changed to NWR.6 4. POLY2: a. 11.1 changed to 11.13 • Update to I3T25SG Exceptions 1.3, 1.6, 13.7, 17.9
C	BG	17-Apr-2008	• Document name change from 'I3T25/C035U Specific (0.35 um) Design Rules' to 'I3T25 (0.35 um) Design Rules' • Mask Information section updated to reflect consolidation of I3T25 and C035U process • Deep pwell (layer 99) updates ○ Change notes to reflect consolidation of I3T25 and C035U processes ○ Clarify requirements for pocket separation • DRC Thick ox (layer 21) updates ○ Change notes to reflect consolidation of I3T25 and C035U processes • Pfield (layer 49) updates ○ Change notes to reflect consolidation of I3T25 and C035U processes ○ Pfield only allowed in HV pockets • Nfield (layer 20) updates ○ Change notes to reflect consolidation of I3T25 and C035U

			processes • Not pwell (layer 8) updates ○ Change notes to reflect consolidation of I3T25 and C035U processes ○ Use standardized wording (enclose v cover) for rule • LPDM12 device specific (LPDE) updates ○ lfpdm 12 device violates nwell spacing ○ OTP passes all latchup tests ○ push rule to allow n-active to nwell spacing increase (special case, see below) ○ Add note on matching of devices ■ For LPDM12, LFNDM, LFPDM LNNDM15 and LFNDM14 DMOS devices, the electrical characteristics are strongly orientation dependent. Whenever matching between these DMOS devices is important, they should be oriented in the same direction. Use of dual finger devices is recommended. ■ LFNDM device specific (NTN25) updates ■ LFPDM device specific (PTN25) updates ○ Used standardized wording 'intersecting' instead of 'overlapping' ○ Clarified rule superseded by device specific rule allowing poly over active corners ○ Add note on matching of devices ■ For LPDM12, LFNDM, LFPDM LNNDM15 and LFNDM14 DMOS devices, the electrical characteristics are strongly orientation dependent. Whenever matching between these DMOS devices is important, they should be oriented in the same direction. Use of dual finger devices is recommended. • LNNDM15 AND LFNDM14 Layout Rules Update ○ Add note on matching of devices ■ For LPDM12, LFNDM, LFPDM LNNDM15 and LFNDM14 DMOS devices, the electrical characteristics are strongly orientation dependent. Whenever matching between these DMOS devices is important, they should be oriented in the same direction. Use of dual finger devices is recommended.
B	MD	22-May-2007	C035U Specific (1000115) and I3T25 (DES-0078) Design Rule Manuals are being combined. No rules changed.
A	BG	07-Jun-2006	added LPDM12, updated GDS to CAD view (Initial release. Unreleased version was referred to as DES-0001.)

The following reflect revisions to Draft Document# DES-0001 C035U Design Rules Manual

Revision	Requestor	Request Number Date	Request Number	Pages	Description
2.2	HDV, MA	13-Dec-05		All	Aligned to DES-0005
2.1	MN				Modified or removed well resistors to put appropriate ones In DES-0005. Moved Schottky diode to DES-0005 (except isolation rule). Fixed typos and corrected the convention of overlap and extension definitions.

1.1	MN	28-Dec-2004			Added Well Resistors; specific support high voltage devices; and IO rules (including LV IO transistor, ESD, and latch up rules)
1.0	MN	24-Sept-2004			Added Schottky Diode, added Seal Ring rules for Deep P-well & N-well, updated the TOC, and corrected typos.
0.1	MT	09-Jan-2004	029372	All	New document

The following reflect revisions to Draft Document# DES-0078 I3T25 Design Rules Manual

Revision	Requestor	Date	Request Number	Pages	Description
2.1	HDV MT	08-11-2005 2/7/2005		All	Adapt manual to version 3.6 of DES0005 and new guidelines.
2.0	MT	03-14-2005		21-38	Added thingate SOA, metal-metal specific rules, updated DMOS layout & electrical rules
1.6	MT	01-20-2004		21-26	Added thingate device specific rules
1.5	MT	12-08-2004		3-19	Added rules 21.5, 20.2, 20.3
1.4	MT	10-18-2004		3-19	Added rules 50.9, 50.10, 49.9. Updated layers table.
1.3	MT	10-17-2004		3-30	Added layout rules for NFIELD and THOX layer. Added thingate electrical rules. Added thingate and thickgate SOA rules.
1.2	MT	10-01-2004		16-18	Added rules 99.15, 49.7, 50.7, and assigned document number, 0078
1.1	MT	9-22-2004		16-18	Adjustments to pwimp-n+act spacing, deep_pwell-n+act spacing, nwell to deep_pwell spacing, pfield-n+act spacing, and rules added for the not_pwell layer.
1.0	MT	9-16-2004		1-18	New document

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Scope and Introduction

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I3T25 INTRODUCTION

SCOPE

This document applies to Design Engineers, Technology Engineers, CAD Engineers, Process Engineers, Quality Assurance Engineers, Reliability Engineers, and Product Engineers.

It is an addendum reference to be applied for the design and layout of any logic and mixed-signal I3T25 product to be fabricated in the AMIS production lines Fab 2 and Fab 10.

Updates of this document are possible. It is the user's responsibility to consult the document control center on the availability of updated revisions of this specification.

PURPOSE

This I3T25 manual provides the layout rules for the 3.3V, C035U-based LV-MS technology, built on n-epi with deep p-well isolation and provides layout rules and electrical parameters for the HV devices targeting applications up to 18 Volt maximum.

This manual is to be treated as an addendum to document DES-0005 C035U (0.35 Micron) Core CMOS Design Rules. DES-0005 contains the base design rules for the 0.35 µm C035U platform that is common for I3T & LV/LP technologies processed in Fab 2 and Fab 10.

Please refer to the section entitled “I3T25 Technology Features and Isolation Concept “ for a simplified cross-section of how n-epi is isolated by using a deep p-well.

REFERENCE DOCUMENTS

DES-0005: C035U (0.35 Micron) Core CMOS Design Rules
1000033: Assembly/Probe Related Layout Rules

As described in specification DES-0005, the CMOS process within the I3T25U technology is a single level poly, twin-tub CMOS process using an n-type epitaxial layer on top of a p-type substrate.
I3T25 as basis CMOS technology offers: silicided source and drains and polysilicon, and resistors on unsilicided active area and unsilicided polysilicon.
To this core digital process extra process modules have been added mixed signal applications: MIM-capacitors and high ohmic polysilicon resistors.
C035U-based technologies offer flexible metallization schemes. Minimum number of metal layers is 3, maximum number of metal layers is 5. The top layer metal can be either thin or thick. The table below gives an overview of the qualified metallization modules available for product design.

Level	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
Metal 1	72 mΩ/sq	72 mΩ/sq	72 mΩ/sq	72 mΩ/sq	72 mΩ/sq	72 mΩ/sq
Metal 2	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq
Metal 3	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq	34 mΩ/sq	55 mΩ/sq	55 mΩ/sq
Metal 4	-	55 mΩ/sq	55 mΩ/sq	-	34 mΩ/sq	55 mΩ/sq
Metal 5	-	-	55 mΩ/sq	-	-	34 mΩ/sq

In addition, a thick top metal layer could be made available as an option for Power Metal applications.
The CMOS technology I3T25 is developed for the design of circuits operating at a power supply voltage of 3.3 volt (+0.3/-0.6 volt).
As opposed to standard CMOS technologies built on p/p+ epitaxial material the following should carefully be taken into account:

- Devices are built into an n-type epi. As a consequence the Pwell will be floating and the Nwell will be common inside a single N-EPI pocket. All Pwell's need to be contacted, whereas the Nwell should be at Vdd, or otherwise an I3T25U isolation should be added to make them floating.
- The Nwell resistors are (if no precautions are taken versus the current layout) in an n-type epi environment can not be processed and have to be replaced by other resistors.

The I3T25 high voltage technology uses a deep_pwell as an isolation feature. As such this feature makes n-epi pockets fully floating towards the p-type substrate. In section 2 of this document the isolation scheme is described in more detail.

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Mask Information

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I3T25 MASK INFORMATION

Deep P-well Layers Table

The table hereafter gives the list of GDS layers that will contain data to be translated into processing masks. The complete layers table is given in the next section.

DIGITIZED AREA	GDS NUMBER	GDS LAYER NAME	DRAWN/ GENERATED	LAYOUT GRID	NOTES
LIGHT	99	deep_pwell	D	0.05 µm	-

Streamed Layers Table

The following gives a listing of the streamout layers used for the I3T25 technology including the deep p-well module process.

 # digital drawing layers

```
nwell          drawing      1      0
active         drawing      2      0
poly           drawing     13      0
poly2          drawing     11      0
pplus          drawing     17      0
siprot         drawing     18      0
contact        drawing     19      0
metal1         drawing     23      0
v1             drawing     25      0
metal2         drawing     27      0
v2             drawing     32      0
metal3         drawing     34      0
v3             drawing     35      0
metal4         drawing     36      0
v4             drawing     52      0
metal5         drawing     53      0
nitride        drawing     31      0
rnwell         drawing    112      0
mexclude       drawing     62      4
y9             drawing      0     63
noring         drawing     51      0
metdis         drawing     63      0
nlddprot       drawing     38      0
nplusprot      drawing     66      0
metal1     positivePS      23      1
metal1     negativePS      23      2
metal2     positivePS      27      1
metal2     negativePS      27      2
metal3     positivePS       4      1
metal3     negativePS      34      2
metal4     positivePS      36      1
metal4     negativePS      36      2
```

metal5	positivePS	53	1
metal5	negativePS	53	2

 # digital drawing layers (Other)

dractxt	drawing	15	0
c4	drawing	39	0

 # digital mask making layers

not_pwell	drawing	8	0
nldd	drawing	14	0
nplus	drawing	16	0
nogen	drawing	61	0
nwell	hd	1	30
active	hd	2	30
poly	hd	13	30
pplus	hd	17	30
siprot	hd	18	30
contact	hd	19	30
metal1	hd	23	30
v1	hd	25	30
metal2	hd	27	30
v2	hd	32	30
metal3	hd	34	30
v3	hd	35	30
metal4	hd	36	30
v4	hd	52	30
metal5	hd	53	30
mcapa	drawing	3	0
mdiode	drawing	4	0
mnpn	drawing	5	0
mpnp	drawing	6	0
mres	drawing	7	0
msub	drawing	9	0
nogate	drawing	10	0
nondrc	drawing	62	47
mfuse	drawing	62	48
mio	drawing	62	56
mshield	drawing	62	49
mfgpp	drawing	46	0
poly	markerR	13	17
metal1	markerR	23	17
metal2	markerR	27	17
metal3	markerR	34	17
metal4	markerR	36	17
metal5	markerR	53	17

 # CAD texting layers (Other)

text	drawing	0	0
poly	pintext	13	21
metal1	lpetext	23	22

metal1	pintext	23	21
metal1	flatext	23	20
metal2	lpetext	27	22
metal2	pintext	27	21
metal2	flatext	27	20
metal3	lpetext	34	22
metal3	pintext	34	21
metal3	flatext	34	20
metal4	lpetext	36	22
metal4	pintext	36	21
metal4	flatext	36	20
metal5	lpetext	53	22
metal5	pintext	53	21
metal5	flatext	53	20

 # CAD P&R layers

prBoundary	drawing	60	0
flatext	drawing	60	20
lpetext	drawing	60	21
pintext	drawing	60	22
metal1	boundary	37	0
metal2	boundary	40	0
metal3	boundary	41	0
metal4	boundary	54	0
metal5	boundary	55	0
v1	boundary	56	0
v2	boundary	57	0
v3	boundary	58	0
v4	boundary	59	0
metal1	pin	23	10
metal2	pin	27	10
metal3	pin	34	10
metal4	pin	36	10
metal5	pin	53	10

 # CAD layers

notusedlayers	drawing	70	0
dracula	drawing	45	0
DREC	drawing	113	0
LREC	drawing	114	0
stext	drawing	116	0
NREC	drawing	118	0

 # Extra layers for i3t25

hipo	drawing	26	0
pwmtl	drawing	33	0
plddprot	drawing	47	0
pwimp	drawing	50	0
polyimp	drawing	76	0
mimc	drawing	78	0
plddonly	drawing	90	0

deep_pwell	drawing	99	0
tenkplyr	drawing	100	0
noviagen	drawing	106	0

 # Extra layers for lfpdm25 / lfndm25

pfield	drawing	49	0
hvroute	drawing	101	0
hvkout	drawing	107	0

 # Extra layers for dual gate

poly2	drawing	11	0
thox	drawing	21	0
nfield	drawing	20	0

Layout data GDS numbering

The table hereafter gives the list of GDS layers that will contain data to be translated into processing masks (marker layers, special layers for e.g. LVS checking, etc… are excluded from this table).

For the GDS numbers in the table below, data type 0 (normal layout – dg) and data type 30 (high density – hd) are assumed; in case other data types are involved, this is indicated by xx_yy, where xx refers to the GDS number and yy refers to the data type.

MASK NAME	DIGITIZED AREA	GDS NUMBER	GDS LAYER NAME	DRAWN/ GENERATED	LAYOUT GRID
DEEP_PWELL	CLEAR	99	deep_pwell	D	0.05 µm
ACTIVE	DARK	2	active	D	0.05 µm
THKGATE	CLEAR	21	thox	D	0.05 µm
PFIELD	CLEAR	49	pfield	D	0.05 µm
NFIELD	CLEAR	20	nfield	D	0.05 µm
NWELL	CLEAR	1	nwell	D	0.05 µm
PWELL	DARK	8 1 50	not_pwell nwell pwimp	G	0.05 µm
THKGATE2	DARK	21	thox	G	0.05 µm
POLY	DARK	13	poly	D	0.025 µm (*)
POLY2	DARK	11	poly2	D	0.025 µm (*)
HIPO	CLEAR	26	hipo	D	0.05 µm
NLDD	DARK	14 17 38 26	nldd pplus nlddprotect hipo	G	0.05 µm
N+IMPLANT	DARK	16 17 66 26	nplus pplus nplusprotect hipo	G	0.05 µm
P+IMPLANT	CLEAR	17	pplus	D	0.05 µm
SALPROTECT	DARK	18	siprot	D	0.05 µm
CONTACT	CLEAR	19	contact	D	0.025 µm (*)
METAL1	DARK	23 23_1 23_2	metal1 metal1_pS metal1_nS	D	0.05 µm
VIA1	CLEAR	25	v1	D	0.05 µm
METAL2	DARK	27 27_1 27_2	metal2 metal2_pS metal2_nS	D	0.05 µm
MIMC	DARK	78	mimc	D	0.05 µm
VIA2	CLEAR	32 78 106	v2 mimc noviagen	D	0.05 µm
METAL3	DARK	34 34_1 34_2	metal3 metal3_pS metal3_nS	D	0.05 µm
VIA3	CLEAR	35	v3	D	0.05 µm

METAL4	DARK	36 36_1 36_2	metal4 metal4_pS metal4_nS	D	0.05 µm
VIA4	CLEAR	52	v4	D	0.05 µm
METAL5	DARK	53 53_1 53_2	metal5 metal5_pS metal5_nS	D	0.05 µm
PASSIVATION	CLEAR	31	nitride	D	0.05 µm
-	-	61	nogen	D	0.05 µm
-	-	62_4	mexclude	D	0.05 µm
-	-	63	metdis	D	0.05 µm
-	-	15	dractxt	D	0.05 µm

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Marking Layers

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I3T25 Marking Layers

The marking layers used in I3T25 base cmos are discussed in C035U Core CMOS. This document only discusses the I3T25 specific marking layers.

They are utilized to distinguish three classes of objects:

a. voltage ranges;
b. specific type of devices;
c. special frozen layouts.
d. High voltage n-epi pockets

GDS NAME	GDS NR.	Data Type	Purpose	Description
HVKOUT	107	0	[dg]	to avoid routing in metal1 or metal2 where there is a risk for parasitic field transistor (HV check): its use should be limited, eg. at the edges of poly gates or on special areas
LREC	114	0	[dg]	Marks high voltage devices and isolated high voltage nepi pockets where especial I3T25 DRC/LVS rules are applied.

Some specific layout rules are defined for their drawing.

In general, a special device is recognized by means of one or more marking layers when the marking layer overlaps, even partially, the “pattern” used for the LVS recognition of that device.

Once a device is recognised by means of a dedicated marking layers (or by means of a combination of more of them), special layout rules can be exclusively checked on it.

Different voltage ranges:

The voltage rating system of I3T25 foresees only two classes of voltages :

1. Low Voltage (LV, up to maximum 3.6 Volt)
2. High Voltage (HV, up to the maximum allowable voltage).

Each of the High Voltage Devices has his own Pcell that is having a deep_pwell in its boundary. As such the HV devices are by default isolated from one another through the deep_pwell. They are also isolated as such from the low voltage part of the circuitry. Furthermore, we will need to make sure there are no pockets made that are having HV and LV parts together.

Indeed if we want to put two isolated nwell regions in the same pocket, they will always be shorted via the underlying n-epi layer. In theory two isolated pwell regions could be located in the same pocket, but there is no way to obtain a high enough voltage range between the two independent pwell regions to allow up to 25 Volt difference in potential. The use of Pfield in the Pwell periphery could be usefull to overcome the voltage problem, but will never be ideal in terms of area consumption. If the wells are always used in CMOS configurations (i.e.

NMOS and PMOS together) there is no way to make it work anyhow.

High Voltage Routing:

The rules discussed here detect possible dangerous situations when routing a connection to a terminal over another pocket. All metal connections coming from terminals placed inside a pocket are considered operating at the max allowed voltage. The maximal voltage difference can therefore exist between any track passing above a pocket and all doping levels present in the pockets.

HVKOUT layer:

The rules discussed here detect possible dangerous situations when routing inside a pocket. The layer HVKOUT (IGS 107) is used to define an area in the layout where any routing of Metal1 and/or Metal2 is forbidden. It is already implemented in few Pcells where the standard DRC verification could not be very effective.

HVKOUT layer can be placed wherever, according to the detected risk of parasitic field MOS transistors, but it is advised to cover the minimal area needed to prevent this occurrence. If a metal connection intersect HVKOUT, the designer must evaluate whether its bias is harmful to invert the crossed implanted layer underneath and move it away accordingly.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
KOUT.1	No METAL1 can intersect HVKOUT area: risk of parasitic field MOS			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

LREC marker:

The LREC marker layer is mandatory for identifying isolated high voltage n-epi pockets and high voltage devices within this pocket.

To apply high voltage only design rules to a HV pockets the drawing layer LREC must be applied anywhere within an n-epi pocket that is isolated with a DEEP_PWELL ring. Once a polygon of LREC is drawn, the text "HVPOCKET" must be added to identify the pocket for high voltage applications and special design rules. Also, see section Layout Rules & Device Specific, "Guidelines and Suggestions for Pcell layout" for additional information on using HV pockets in conjunction with LV pockets and HV pcells.

To apply high voltage only design rules to HV specific devices the LREC marker layer must be present within the given device with a text message of the devices' model name. For I3T25 HV pcells this marker and text is already in place.

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Process Information

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PROCESS INFORMATION

I3T25 technology features:

I3T25 is the ON Semiconductor 0.35 um low-voltage CMOS technology developed for the design of circuits operating at a power supply voltage of 3.3 volt (+0.3/-0.6 volt). The technology is built on n-/p- epitaxial silicon. The I3T25 thingate HV (see below) extends the voltage range to 18V. Also with 290A dual gate option, gate voltage range to 12V.

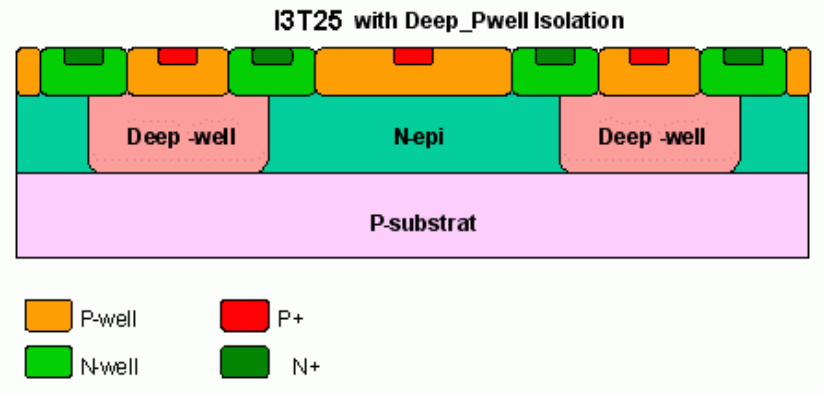
- I3T25 is a 0.35um CMOS based technology that contains a number of integrated mixed-signal modules including:
  - Low Voltage CMOS transistors
  - Medium-High Voltage Smart Power MOS transistors
  - Linear capacitors (MIMC & Poly)
  - High precision resistors
  - Schottky diodes
  - Bipolar transistors
  - ESD primitive cell library
  - Dual gate module (12V gates)
  - HV pocket isolation
  - Freeprom E^2

I3T25 (3.3V) N-epi isolation utilizing Deep_Pwell

The I3T25 process flow starts with silicon consisting of 2.8um of n- epi on top of a p- substrate. The I3T25 deep_pwell module is formed before the core CMOS and has no impact on electrical characteristics. The simplified cross-section below illustrates the concept of electrically isolating one adjacent n-epi pocket from another n-epi pocket. This isolation method is includes an nwell ring adjacent to the deep_pwell layer and is engineered to guarantee 3.3 volts of isolation within a given n-epi pocket.

The following outlines the process flow for the deep p-well module.

- Deep pwell module
    - pad oxide
    - deep_pwell patterning
    - deep_pwell implant
    - deep_pwell anneal drive



I3T25 Thingate module:

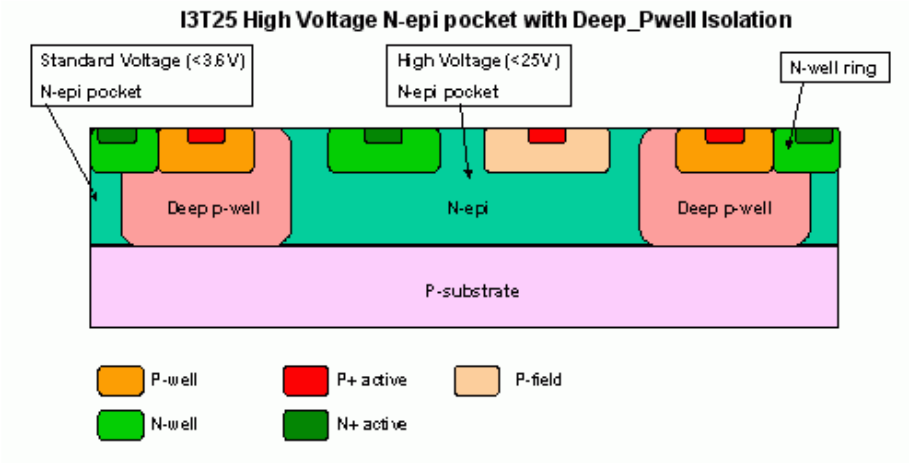
The following outlines the I3T25 thingate module for the I3T25 that is part of the base process flow of the I3T25 technology described in above. (I3T25 is also available without the ‘thingate HV’ module at a savings of 1 mask step)

The PFIELD implant is only required for the thingate PDMOS device. The NDMOS device requires no extra processing in the C035U process flow.

- High Voltage Thingate DMOS module
    - sacrificial oxidation
    - **pfield implant patterning**
    - **pfield implant**
    - **resist removal**
    - tub patterning

I3T25 (25V) N-epi isolation utilizing Deep_Pwell:

The I3T25 technology makes use of high voltage n-epi pockets (<25V) that are electrically isolated from adjacent nepi pockets. The cross-section below illustrates the basic approach. The not_pwell layer is used in a high voltage pocket that suppresses the automatic generation of pwell. This allows 'free' n-epi to exist allowing a high breakdown voltage between n-epi and deep_pwell, and pfield (or pwell) to n-epi.



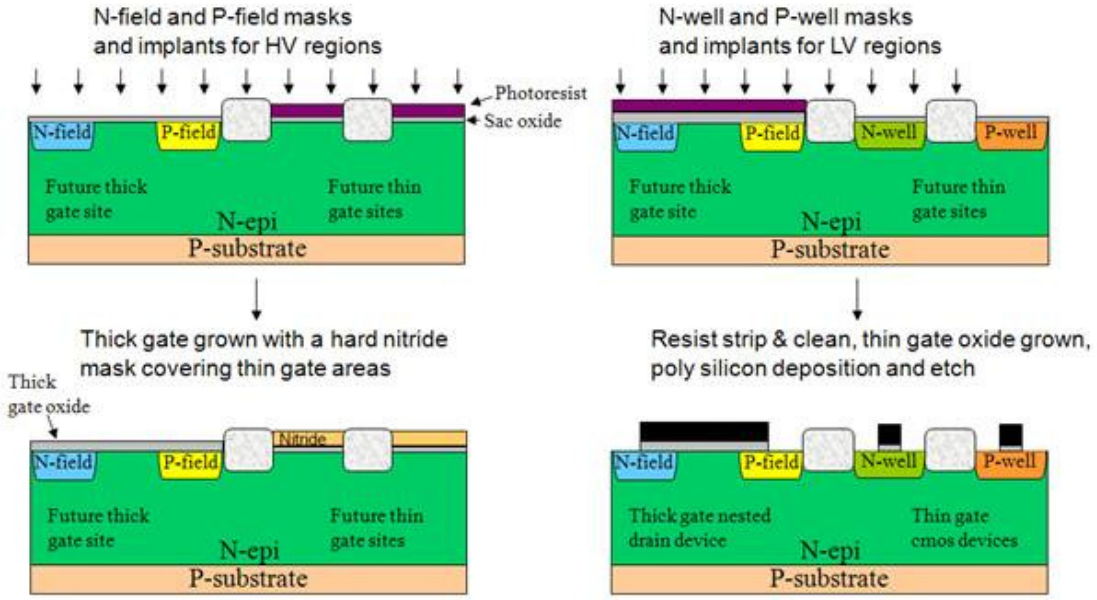
I3T25 Dual Gate Process module:

Advantages for this Dual Gate approach:

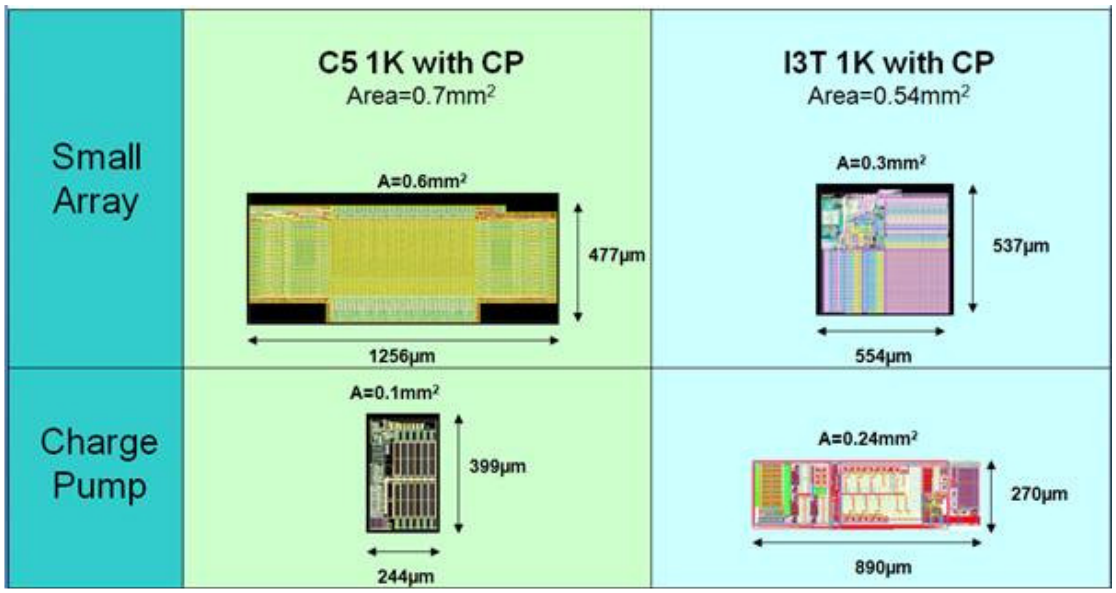
- No implants through Thickgate oxide
- Thickgate processing is nearly ~100% modular with thingate base devices
  - Thermal oxide processing is done prior to implants
    - No significant shifts in Vt and Gamma
  - Field oxide budget is similar to single gate processing
    - Little effect on narrow width CMOS
    - Little effect on base techno active isolations
    - Little effect on FOX BB, no SG DMOS shifts

What's the added manufacturing cost?

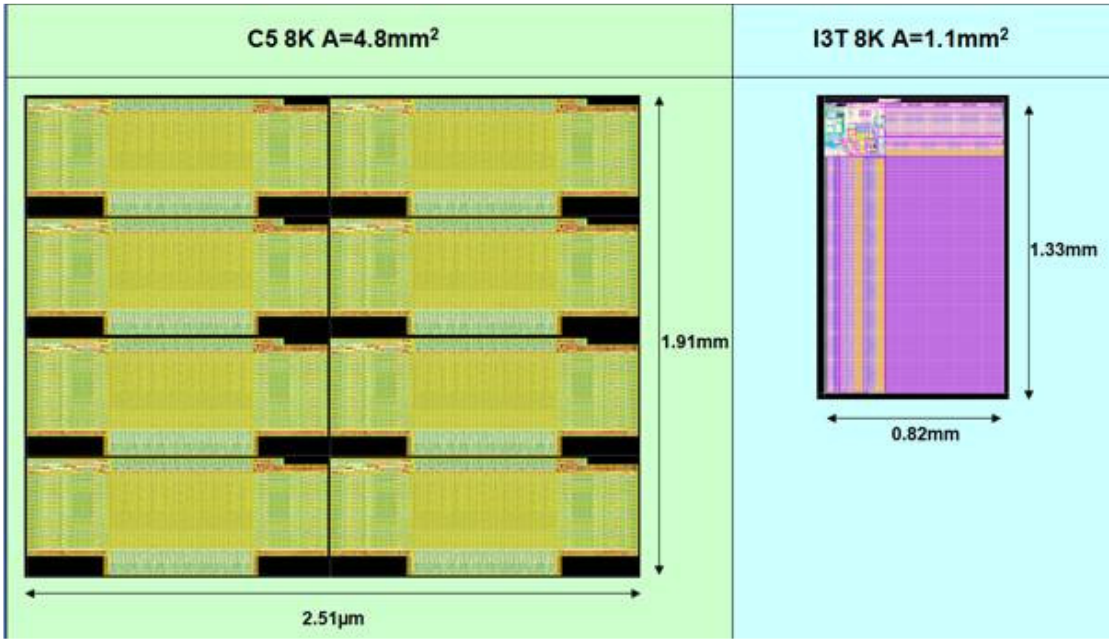
- >+5 added mask steps to I3T25 SG process
  - 31 total masking steps for 5 Metal layers including 1K HIPO



EEPROM in I3T25:



Charge Storage:



I3T25 (0.35 um) Design Rules

Layout Rules and Device Specific Rules

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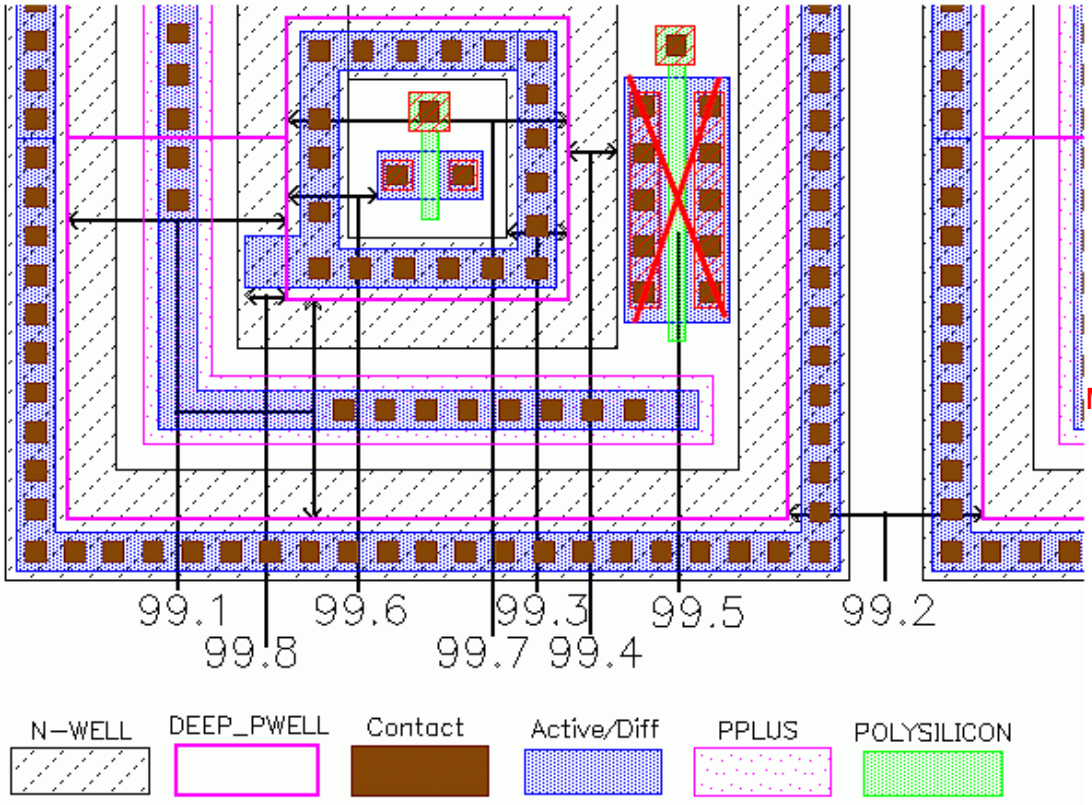
I3T25 (0.35 Micron) DEEP_PWELL Layout Rules

Layer/level #99



NOTE --->
More graphics to view!
See following page
for graphic # 2

Note 1: DEEP_PWELL (GDS layer 99) is used to define DEEP_PWELL isolation. By using DEEP_PWELL rings it is possible to electrically isolate N-EPI pockets. A silicon wafer is N-EPI unless DEEP_PWELL is drawn.

DEEP_PWELL is used by PNP bipolars as a collector (PNP bipolar is built in a polygon of DEEP_PWELL). POLYSILICON resistors, ACTIVE resistors and MIM capacitors are allowed in DEEP_PWELL and related N-WELL ring without restrictions.

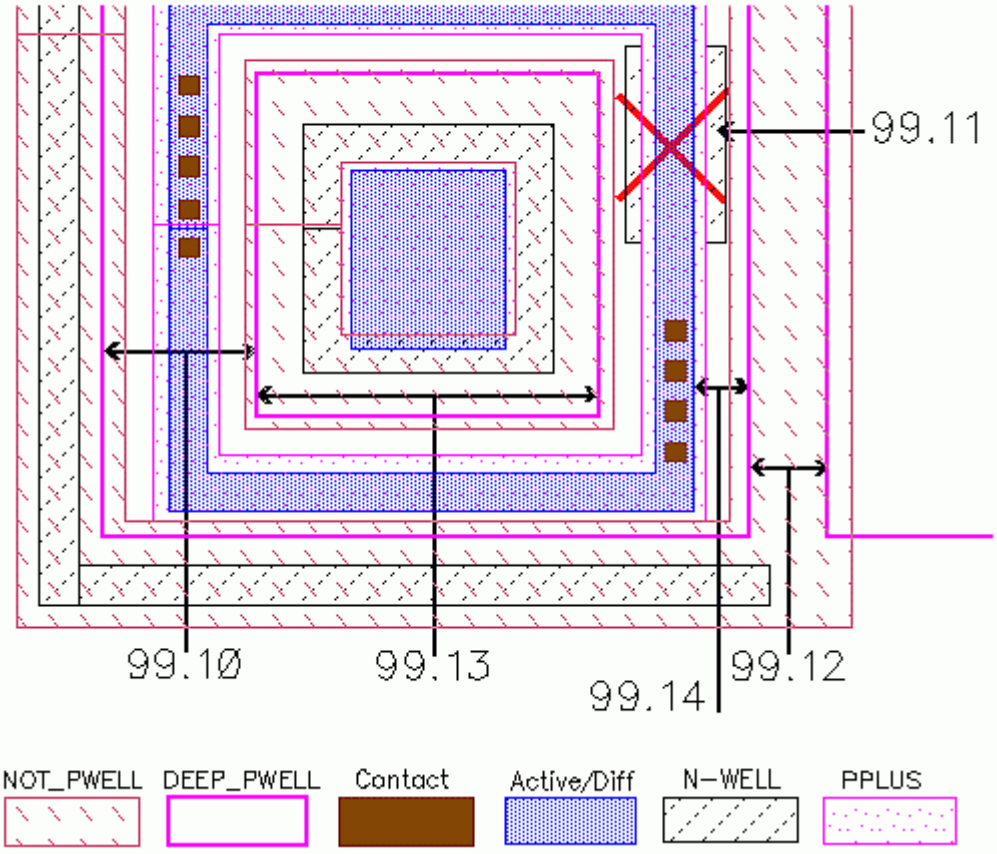
DEEP_PWELL provides electrical connectivity for all P-WELL regions that occur inside DEEP_PWELL. To avoid potential gradients it is advised to connect these P-WELL regions using metal straps, which also ensures better LVS coverage.

Note 2: DEEP_PWELL rules with the note “HV pocket” are defined for high voltage (<25V) operation within an n-epi pocket. A high voltage n-epi pocket is defined when a DEEP_PWELL ring completely encloses an n-epi region and marker layer LREC is drawn within the pocket with the text “HVPOCKET” added. DEEP_PWELL rules 99.1, 99.2, 99.3, 99.4, 99.6, 99.7, 99.8 are for low voltage (<3.6V) n-epi pockets and are all void for high voltage pockets.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
99.1	Minimum deep_pwell width	4.50	µm	*	
99.2	Minimum deep_pwell spacing -if less than 2.50um then merge deep_pwells	2.50	µm	*	If HV pocket is near LV pocket, HV rule 99.12 applies.
99.3	Minimum nwell enclosure of n-epi pocket.	1.25	µm	*	Nwell ring enveloping deep_pwell & n-epi edge is required for proper pwell inside n-epi to deep_pwell isolation.
99.4	Mandatory Nwell intersection with deep_pwell. This is a FIXED intersection value	1.00	µm	*	
99.5	NO CMOS allowed in deep_pwell			*	Except for lfndm25dt, lfndm20dnt
99.6	Minimum CMOS spacing to deep_pwell edge	1.25	µm	*	
99.7	Minimum n-epi pocket width	2.50	µm	*	
99.8	Maximum extension of active layer in deep_pwell	0.75	µm	*	Except for lfndm25dt
99.10	Minimum DEEP_PWELL width (for 25V breakdown with adjacent Nepi pocket)	6.00	µm	*	(Rule is specific to the HV pocket) HV pocket to LV pocket DPW must be min 7um due to requirement of nwell intersection with DPW (1.0um) plus DPW (without any nwell in it) around HV pockets of 6.0um.
99.11	No NWELL or NFIELD is allowed in or coincident with DEEP_PWELL (for 25V breakdown with adjacent Nepi pocket)			*	(Rule is specific to the HV pocket) The check identifies deep pwell which is within 6 um of a HV pocket and determines the presence of nwell and nfield in this zone.
99.12	Minimum deep_pwell spacing - if less than 3.00um then merge deep_pwells	3.00	µm	*	(Rule is specific to the HV pocket)
99.13	Minimum n-epi pocket width	3.00	µm	*	(Rule is specific to the HV pocket)
99.14	Minimum DEEP_PWELL enclosure ACTIVE AREA	2.00	µm	*	(Rule is specific to the HV pocket) Except for lfndm25dt
99.15	deep_pwell ring requires full p+ active ring			*	(Rule is specific to HV pocket containing thox)

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

HV Pocket rules:



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I3T25 (0.35 Micron) THOX Layout Rules

Layer/level #21

Note 1: Thox is not presently used in the released devices of the technology.: These THOX rules are defined for high voltage (<25V) gate operation of thickgate DMOS devices. This layer is only allowed in the high voltage n-epi pockets. The presence of a THOX layer in a HV pocket results in a thick gate oxide under poly gates.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
21.1	Minimum THOX spacing	0.70	µm	*	
21.2	Minimum THOX width	2.00	µm	*	
21.3	Minimum THOX to active spacing	0.30	µm	*	
21.4	Minimum THOX enclosure of active	0.30	µm	*	
21.5	THOX only allowed in high voltage n-epi pocket			*	Except for lfndm20dnt

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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I3T25 (0.35 Micron) PFIELD Layout Rules

Layer/level #49

Note 1: Specific to the I3T25 process: It defines drawn lightly p-doped areas, inside free n-epi regions. Therefore, it can be used only where no deep n-doped layers are used, i.e. it can be drawn only where there is no NWELL.

It is used to form the drain drift region of the thin and thick gate PDMOS25 and the body of the thick gate NDMOS25.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
49.1	Minimum PFIELD width	1.40	µm	*	(Rule is specific to HV pocket)
49.2	Minimum PFIELD spacing (if less then merge)	1.70	µm	*	(Rule is specific to HV pocket) Except for lfpdm25dt
49.3	Minimum PFIELD spacing to DEEP_PWELL (for 25V breakdown)	2.00	µm	*	(Rule is specific to HV pocket)
49.4	Minimum PFIELD spacing to NWELL (for 25V breakdown)	0.00	µm	*	(Rule is specific to HV pocket)
49.5	Minimum PFIELD enclosure of free P+ ACTIVE (for 25V junction termination), the active area must not cross PFIELD edges.	1.00	µm	*	(Rule is specific to HV pocket) Free ACTIVE is an active area not covered by POLY gate. Except for lfpdm20nt
49.6	Minimum PFIELD spacing to N+ ACTIVE (guard ring in PDMOS)	1.00	µm	*	(Rule is specific to HV pocket)
49.15	Pfield is only valid in HV pocket			*	(Rule is specific to HV pocket)
49.16	Minimum PFIELD enclosure N+ ACTIVE	1.00	µm	*	(Rule is specific to HV pocket) Except for lfndm25t, lfndm20nt
49.17	Minimum PFIELD spacing to NFIELD (for 25V breakdown)	0.00	µm	*	(Rule is specific to HV pocket)
49.18	Minimum PFIELD spacing to P+ ACTIVE (if at different potential)	2.00	µm	*	(Rule is specific to HV pocket)

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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I3T25 (0.35 Micron) NFIELD Layout Rules

Layer/level #20

Note 1: Nfield is not presently used in the released devices of the technology.: The NFIELD layer is only used in a high voltage n-epi pocket.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
20.1	Minimum NFIELD spacing to DEEP_PWELL (for 25V breakdown)	1.00	µm	*	
20.2	Minimum NFIELD width	1.70	µm	*	Except for lfpdm25dt, lfpdm20dnt
20.3	NFIELD only allowed in high voltage n-epi pocket			*	Except for lfndm20dnt

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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I3T25 (0.35 Micron) N-WELL Layout Rules

Layer/level #1

Note 1: Specific to the I3T25 process: All low voltage rules for NWELL are defined in DES-0005. The following NWELL rule(s) apply to applications within a high voltage n-epi pocket.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
1.9	Minimum NWELL spacing to DEEP_PWELL (for 25V breakdown)	1.00	µm	*	(Rule is specific to the I3T25 process)

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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I3T25 (0.35 Micron) PWIMP Layout Rules

Layer/level #50

Note 1: Specific to the I3T25 process: In standard Low Voltage, Mixed Signal CMOS, the p-well implanted areas are generated as a copy of the drawn nwell data, since the pwell mask is actually protecting the nwell areas from the pwell implant, the corresponding GDS layer is referred to as NOT_PWELL.

Note 2: The I3T25 technology offers the possibility of having N-epitaxial regions, not implanted either by nwell nor pwell. In this case, the NOT_PWELL layer has to be explicitly drawn.

Note 3: For convenience, the layer PWIMP (GDS layer 50) has been introduced, allowing the definition of a floating pwell, inside a drawn NOT_PWELL area.

Note 4: As a consequence of the description the PWIMP layer will only be used in the high voltage areas.

Note 5: IMPORTANT REMARK: The PWIMP rules listed below are ONLY to be used in high voltage pockets. They do NOT apply to general low voltage CMOS pockets. In LV pockets PWIMP rules are defined in DES-0005.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
50.6	Minimum PWIMP spacing to N+ ACTIVE (guard ring in NDMOS, at 25V)	1.00	µm	*	(Rule is specific to the I3T25 process)
50.13	Minimum PWIMP spacing to NWELL (for 25V breakdown)	1.00	µm	*	(Rule is specific to the I3T25 process)
50.17	Minimum PWIMP enclosure of free P+ ACTIVE (for 25V PFIELD breakdown), the active area must not cross PWIMP edges.	1.00	µm	*	(Rule is specific to the I3T25 process) Free ACTIVE is an active area not covered by POLY gate.
50.19	Minimum PWIMP spacing to NFIELD (for 25V breakdown)	1.00	µm	*	(Rule is specific to the I3T25 process)
50.20	Minimum PWIMP spacing to P+ ACTIVE (if at different potential)	2.00	µm	*	(Rule is specific to the I3T25 process)
50.23	Minimum PWIMP spacing to PFIELD (pfield should NOT share common area with pwimp)	2.00	µm	*	(Rule is specific to the I3T25 process)
50.24	Minimum PWIMP spacing to DEEP_PWELL (for 25V breakdown)	2.00	µm	*	(Rule is specific to the I3T25 process)

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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I3T25 (0.35 Micron) NOT_PWELL Layout Rules

Layer/level #8

Note 1: Specific to the HV pockets: Defines all areas that are not pwell implanted outside the nwells. This layer should not be drawn in LV pockets except for a few special devices that require within the pcell.

Note 2: In the case of HV pockets pwell implants should be explicitly stopped in certain regions to allow for higher voltages, that pocket must be covered by drawn NOT_PWELL. PWIMP can be used to force a hole in this light field mask. In high voltage pockets, PWIMP should be used. The NOGEN layer has no influence on the generation of the final PWELL mask, therefore any n-doped regions inside NOGEN for which the pwell implant should be stopped need to be covered by NOT_PWELL.

Note 3: The layout rules for all pwell implanted regions are defined for any drawn PWIMP region as well as for the complementary areas of the generated NOT_PWELL, unless explicitly mentioned.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
8.2	Maximum NOT_PWELL intersection with DEEP_PWELL	1.00	µm	*	(Rule is specific to the I3T25 process) Except for lfndm25dt, lfndm20dnt
8.3	NOT_PWELL intersection with DEEP_PWELL for a high voltage pocket -this is a fixed value – NOT_PWELL must enclose the entire HV n-epi pocket	1.00	µm	*	(Rule is specific to the I3T25 process) Except for lfndm25dt, lfndm20dnt

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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I3T25 (0.35 Micron) ACTIVE Layout Rules

Layer/level #2

Note 1: Specific to the I3T25 process: Defines all MOS source and drain areas, diffused areas for inter-connect, resistors and n-well straps.
Unless otherwise specified, these rules must be applied to drawn ACTIVE areas.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
2.8	Minimum N+ ACTIVE area spacing to DEEP_PWELL within a high voltage pocket	1.00	µm	*	(Rule is specific to the I3T25 process) Except for lfndm25dt

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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I3T25 (0.35 Micron) CONTACT Layout Rules

Layer/level #19

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
19.7	Minimum polysilicon contact spacing to active area on thox	0.70	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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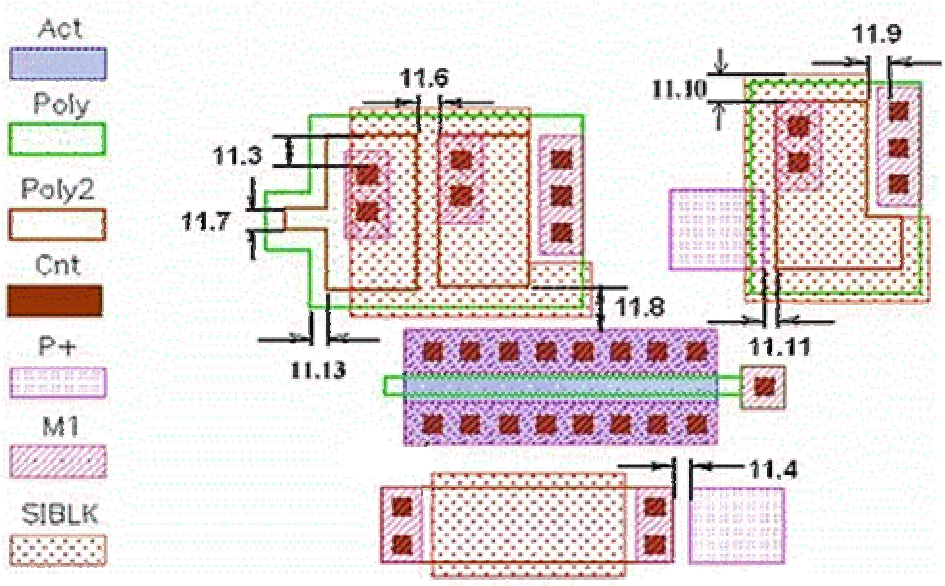
I3T25 (0.35 Micron) POLY2 Layout Rules

Layer/level #11



Note 1: Poly2 (aka: P2, PY2 or Cap Poly in some processes) layer is used to define top capacitor

Note 2: TopCap is Poly2 on Poly1 used for capacitor.
Note 3: BotCap is Poly1 used for a capacitor

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
11.2	Min Poly2 to Active Spacing	0.20	µm	*	
11.3	Min POLY2 Enclosure of Contact	0.30	µm	*	
11.4	POLY2 is Outside P+			*	Poly2 must be outside of P+
11.5	Min Poly2 to P+ Spacing	0.50	µm	*	
11.6	Min POLY2 Spacing	0.80	µm	*	
11.7	Min POLY2 Width	2.00	µm	*	
11.8	Min POLY2 to Active Space	2.00	µm	*	
11.9	Min POLY2 to Contact Spacing	0.60	µm	*	
11.10	Min required siprot enclosure of POLY2	0.50	µm	*	Poly2 top plate must be totally covered by SIBLK layer.
11.11	Min POLY2 to P+ Space	2.00	µm	*	
11.12	Poly 2 is not allowed below M2.5			*	
11.13	Min POLY1 Enclosure Of POLY2	1.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

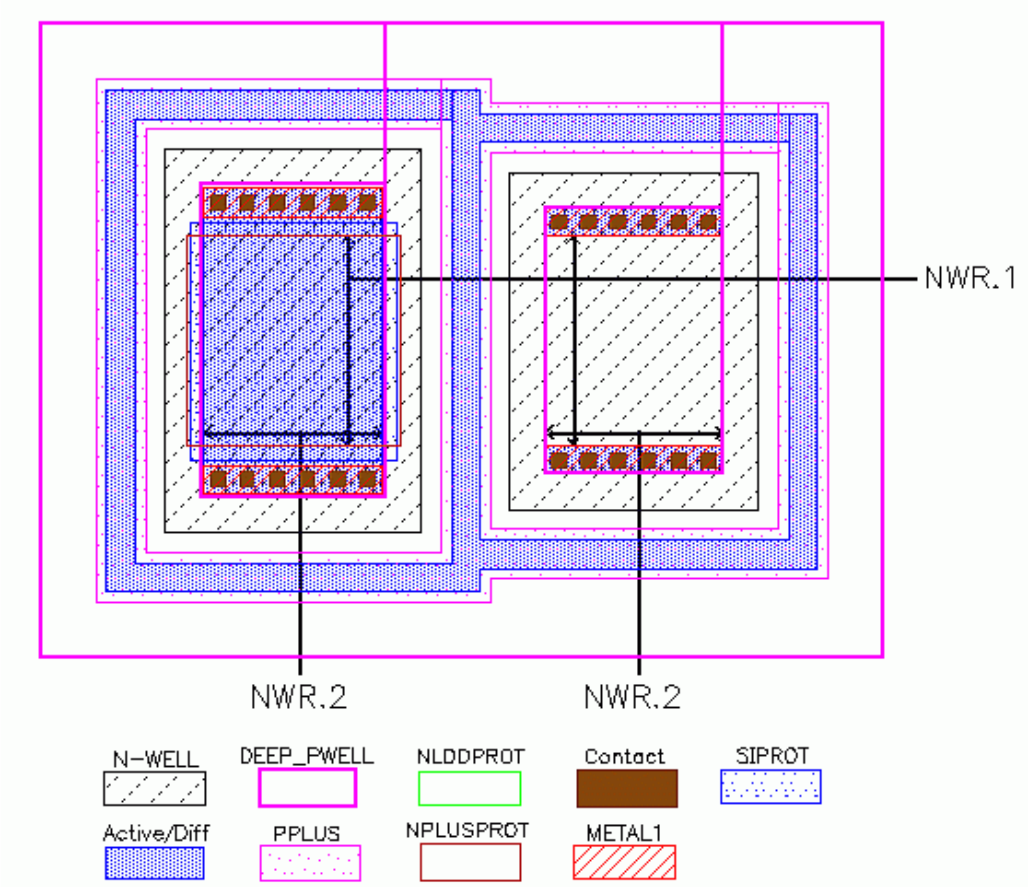
I3T25U (0.35 Micron) EXCEPTIONS FOR SPECIFIC COMPONENTS Layout Rules

Note 1: Some of the devices do not respect certain C035U rules. For these cases, exceptions have been made and are given in the list below.

Exceptions related to the DES-0005 C035U (0.35 Micron) Core CMOS Design Rules document:

Rule Name	Rule Description	Rule Value	Notes
1.3	See DES-0005	See DES-0005	Exceptions for lfndm25, lfpdm25
1.6	See DES-0005	See DES-0005	Exceptions for lfpdm25
13.7	See DES-0005	See DES-0005	Exceptions for lfndm25
17.9	See DES-0005	See DES-0005	Exception for lfpdm25, lfpdm25t, lfpdm20nt
18.6	See DES-0005	See DES-0005	Exception for lfndm20nt, lfpdm20nt, lfpdm20dnt, lfndm20dnt
18.15	See DES-0005	See DES-0005	Exception for lfpdm20nt, lfpdm20dnt
18.18	See DES-0005	See DES-0005	Exception for lfpdm20nt, lfpdm20dnt
18.21	See DES-0005	See DES-0005	Exception for lfndm20nt, lfpdm20nt, lfpdm20dnt, lfndm20dnt
18.22	See DES-0005	See DES-0005	Except for lfpdm20nt, lfpdm20dnt
18.24	See DES-0005	See DES-0005	Except for lfndm20nt, lfpdm20nt, lfpdm20dnt , lfndm20dnt
19.10	See DES-0005	See DES-0005	Exception for pipc Poly2
38.5	See DES-0005	See DES-0005	Except for lfndm20nt, lfpdm20nt, lfpdm20dnt, lfndm20dnt
50.4	See DES-0005	See DES-0005	Exception for SCHD, lfndm20dnt
66.3	See DES-0005	See DES-0005	Except for lfndm20nt, lfpdm20nt, lfpdm20dnt, lfndm20dnt
66.9	See DES-0005	See DES-0005	Exception for SCHD, lfndm20nt,
66.10	See DES-0005	See DES-0005	Except for lfndm20nt, lfpdm20nt, lfpdm20dnt, lfndm20dnt
66.14	See DES-0005	See DES-0005	Except for lfndm20nt, lfpdm20nt, lfpdm20dnt, lfndm20dnt,

I3T25 (0.35 Micron) N-WELL RESISTORS Layout Rules



Note 1: N-WELL resistors in C035U with DEEP_PWELL isolation technology are available in two types. These types are: nwarsb and nwrsb. nwarsb is an N-WELL resistor under ACTIVE, whereas nwrsb is an N-WELL resistor under Field Oxide.

The width and length of these resistors is defined as follows:

- · Width is defined perpendicular to the direction of current flow. It is the width of the active area for nwarsb and the width of the DEEP_PWELL opening for nwrsb.
- · Length is defined parallel to the direction of current flow. It is the length of the NPLUSPROT and NLDDPROT layers (which are copies of each other) for nwarsb and the distance between the two active areas for nwrsb.

Since all N-WELL resistors inside a pocket are at the same potential, each N-WELL resistor needs its own pocket for electrical isolation.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
NWR.1	Minimum N-Well Resistor Width	5.00	µm	*	
NWR.6	Minimum N-Well Resistor Length	5.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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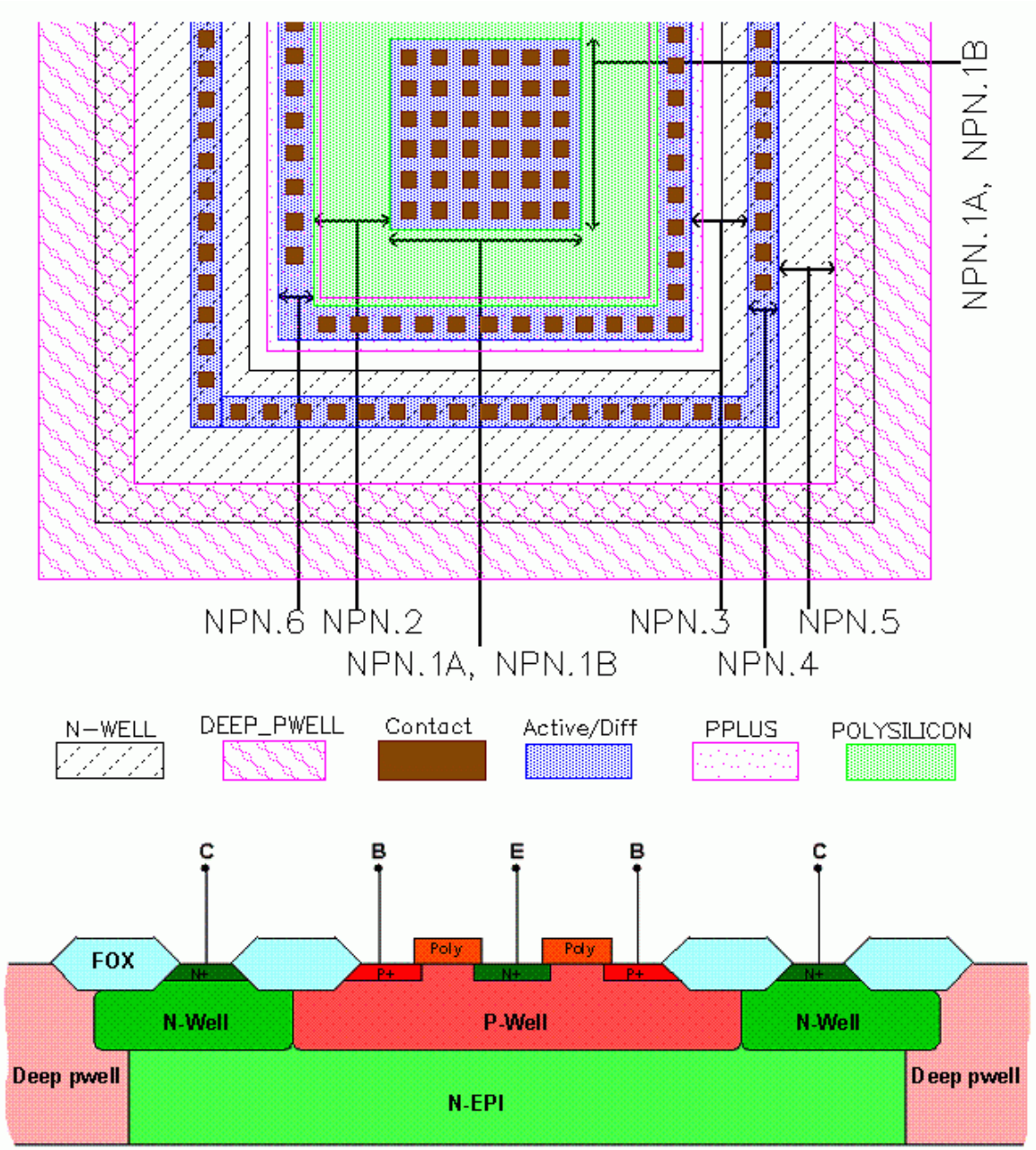
I3T25 (0.35 Micron) VERTICAL NPN TRANSISTOR Layout Rules



Note 1: Vertical NPN bipolar transistor is formed using NPLUS ACTIVE as emitter, P-WELL as the base and N-EPI as the collector. PPLUS ACTIVE area is used for base contact. NPLUS ACTIVE area together with N-WELL is used for collector contact. The emitter is self aligned by using POLYSILICON ring.

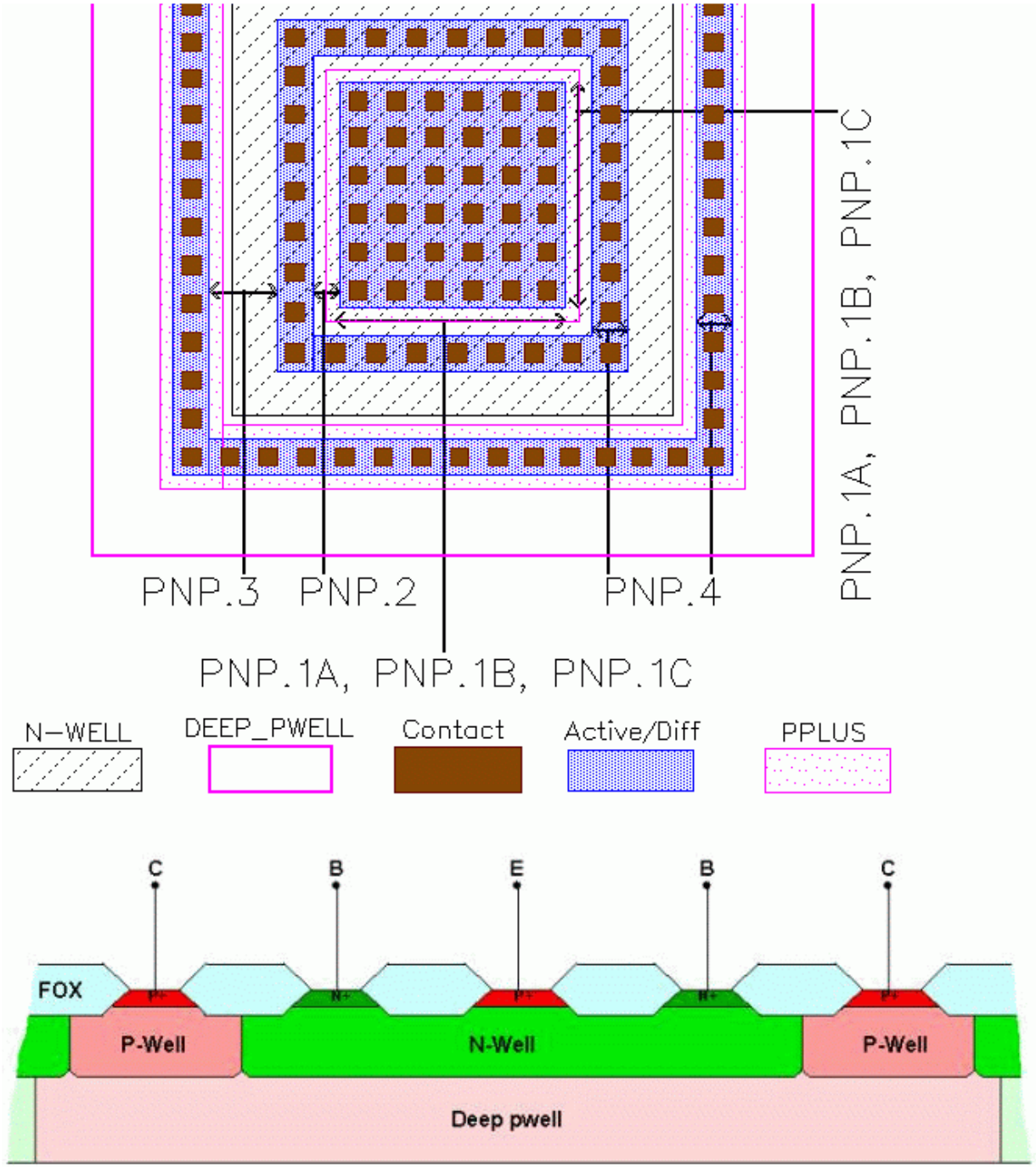
Model performance can only be guaranteed if the following set of rules are obeyed in layout.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
NPN.1A	Mandatory emitter length & width - only two different fixed sizes available	5.00	µm	*	

NPN.1B	Mandatory emitter length & width - only two different fixed sizes available	10.00	µm	*	
NPN.2	Mandatory poly width -emitter to base distance	2.00	µm	*	
NPN.3	Mandatory base active to collector active spacing -base to collector distance	1.50	µm	*	
NPN.4	Mandatory collector active width	0.80	µm	*	
NPN.5	Mandatory collector active to deep_pwell	1.50	µm	*	
NPN.6	Mandatory base active width	0.90	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

I3T25 (0.35 Micron) VERTICAL PNP TRANSISTOR Layout Rules



Note 1: Vertical PNP bipolar transistor is formed using PPLUS ACTIVE as emitter, N-WELL as the base and DEEP_PWELL as the collector. NPLUS ACTIVE area is used for base contact. PPLUS ACTIVE area together with P-WELL is used for collector contact.

Model performance can only be guaranteed if the following set of rules are obeyed in layout.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
PNP.1A	Mandatory emitter length & width - three different fixed sizes modelled	0.80	µm	*	
PNP.1B	Mandatory emitter length & width - three different fixed sizes modelled	5.00	µm	*	
PNP.1C	Mandatory emitter length & width - three different fixed sizes modelled	10.00	µm	*	
PNP.2	Mandatory emitter active to Base active spacing -emitter to base distance	0.60	µm	*	
PNP.3	Mandatory base active to Collector active spacing -base to collector distance	1.50	µm	*	
PNP.4	Mandatory Base and Collector active width	0.80	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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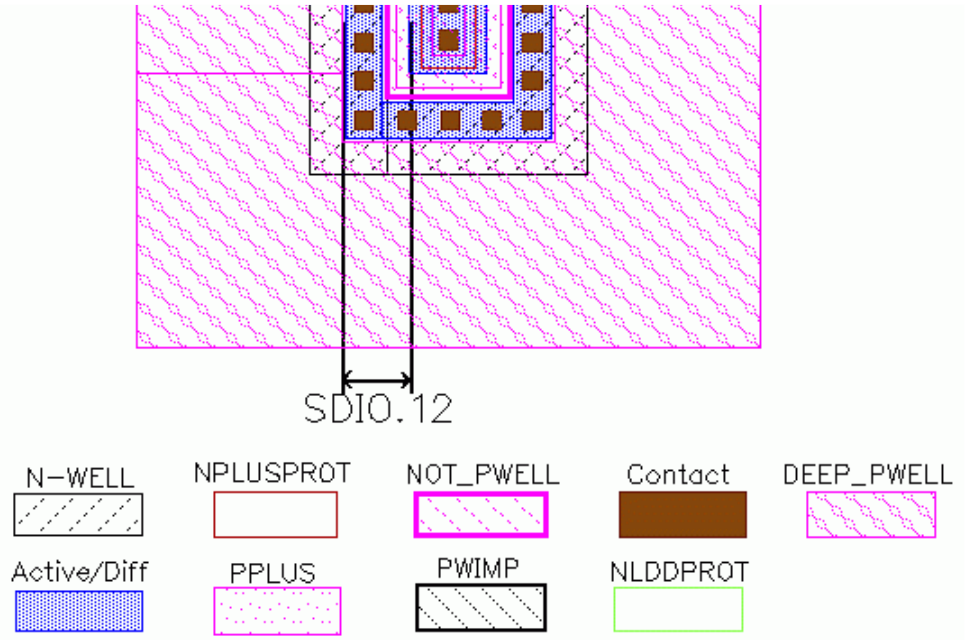
I3T25 (0.35 Micron) SCHOTTKY DIODE Layout Rules



Note 1: The description and set of rules applicable to the core of this device can be found in C035U (0.35 Micron) Core CMOS Design Rules. Additional rule applicable to isolation is given below.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
SDIO.12	Minimum Deep_P-well Space to Schottky Active	1.50	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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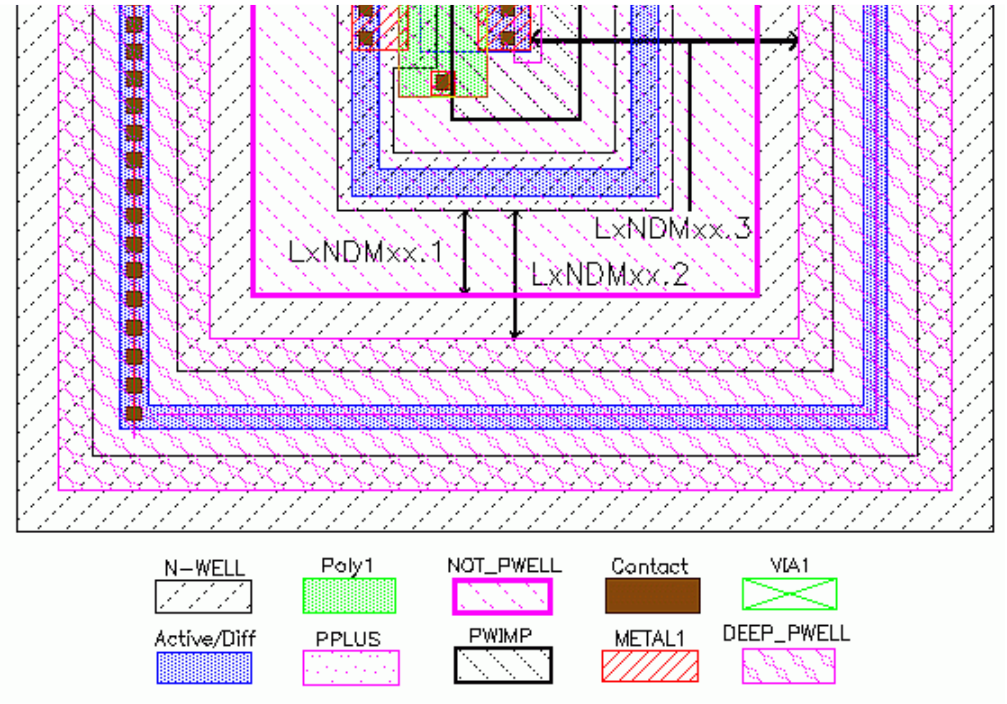
I3T25 (0.35 Micron) LNNDM15 AND LFNDM14 Layout Rules



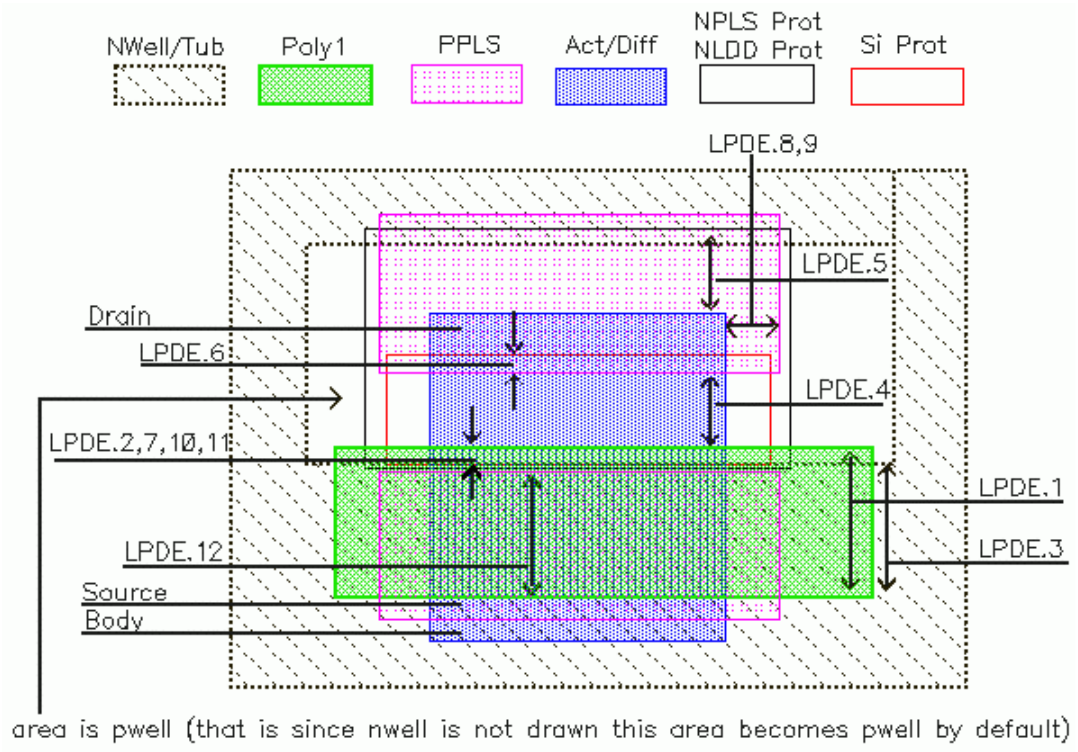
Note 1: The description and set of rules applicable to the core of these devices can be found in C035U (0.35 Micron) Core CMOS Design Rules. Additional rules applicable to isolation of these devices are given below.

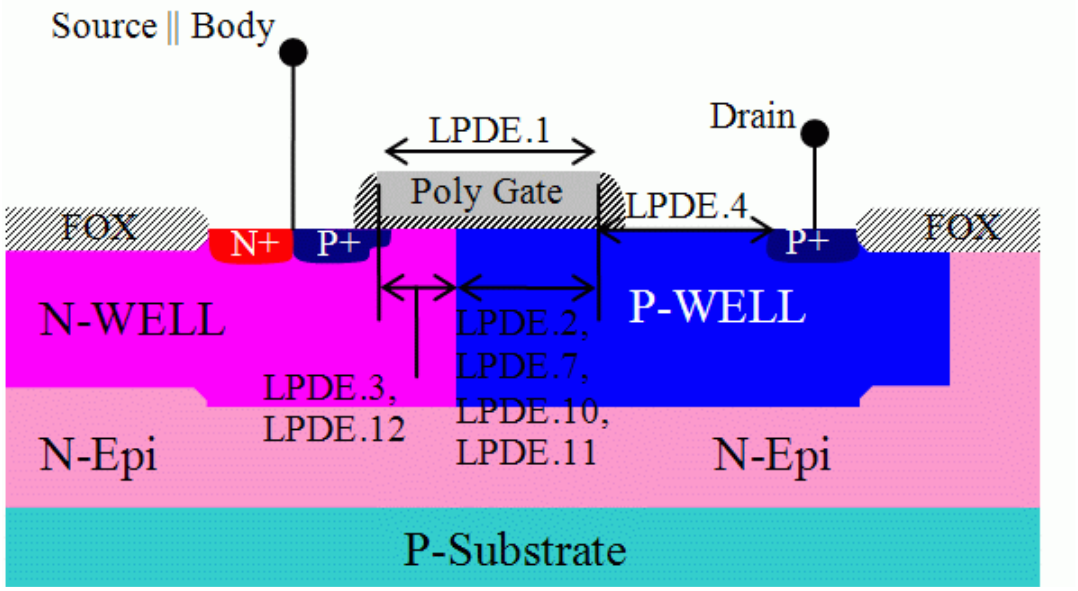
Note 2: For LPDM12, LFNDM, LFPDM LNNDM15 and LFNDM14 DMOS devices, the electrical characteristics are strongly orientation dependent. Whenever matching between these DMOS devices is important, they should be oriented in the same direction. Use of dual finger devices is recommended.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
LxNDMxx.1	Minimum Space N-well Drain to N-Well Isolation (protected by not_pwell)	6.00	µm	*	
LxNDMxx.2	Minimum Space N-Well Drain to Deep P-Well	7.25	µm	*	
LxNDMxx.3	Minimum Space P+ Active to Deep P-Well	6.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

I3T25 (0.35 Micron) LPDM12 Layout Rules





Note 1: This section covers the Lateral P-type Drain extended MOS (lpdm12, lpdm12op30, ldpm12op3m)

Note 2: lpdm12, lpdm12op30, ldpm12op3m are not checked by DRC release 3.4 or earlier

Note 3: The layout rules of the variable width (W=3.5um for EE, W = 30, 3000 for OTP) lateral 12V PDMOS used

in the control circuit of the FREEPROM based EEPROM and OTP are described in the table below. There valid width are described below. Design rule LPDE.13a-c will call out invalid widths, use of the wrong width to schematic will be found by LVS.

Device	Width
lpdm12	3.5
lpdm12op30	30
ldpm12op3m	30 fingers 100um width

Note 4: LPDM12 is ONLY qualified for use in OTP and Freeprom.
Note 5: For LPDM12, LFNDM, LFPDM LNNDM15 and LFNDM14 DMOS devices, the electrical characteristics are strongly orientation dependent. Whenever matching between these DMOS devices is important, they should be oriented in the same direction. Use of dual finger devices is recommended.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
LPDE.1	Fixed poly length	1.40	µm	*	
LPDE.2	Fixed Pwell implanted (Pwell/Pwimp) intersection with poly on drain side (PW_ext)	0.30	µm	*	Pwimp is only drawn when the LPDM12 is placed alone in its own Nepi pocket in combination with the layer “not_pwell”. In all the other cases, the Pwell drain extension is generated.
LPDE.3	Fixed Nwell intersection with poly on source side (channel length)	1.10	µm	*	
LPDE.4	Fixed spacing pplus to poly gate at the drain side (Lpsd)	0.70	µm	*	
LPDE.5	Minimum spacing drain active to Nwell ring	1.10	µm	*	
LPDE.6	Fixed siprot intersection with pplus at the drain side	0.40	µm	*	
LPDE.7	Fixed siprot intersection with poly	0.30	µm	*	
LPDE.8	Minimum enclosure by nplusprot of active at the drain side (except active under poly)	0.50	µm	*	
LPDE.9	Minimum enclosure by nlddprot of active at the drain side (except active under poly)	0.50	µm	*	
LPDE.10	Fixed intersection nplusprot with poly	0.30	µm	*	
LPDE.11	Fixed intersection nlddprot with poly	0.30	µm	*	
LPDE.12	Fixed intersection Pplus (source) with poly gate	1.10	µm	*	
LPDE.13a	Fixed lpdm12 gate width.	3.50	µm	*	
LPDE.13b	Fixed lpdm12op30 gate width.	30.00	µm	*	
LPDE.13c	Fixed ldpm12op3m gate finger width.	100.00	µm	*	
LPDE.14	For lpmd12 devices: maximum spacing of n-active in n-wells (when the n-well contains p-active).	120.00	µm	*	Exception to XN.5 Must be checked independent of high density memory rules XN.5mem.

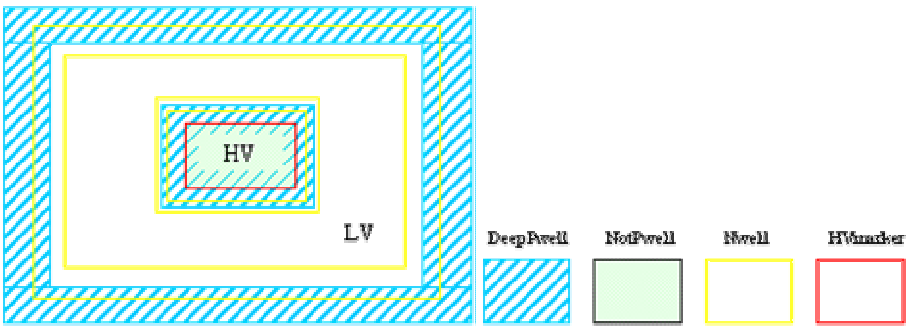
(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

Guidelines and Suggestions for Pcell layout:

The following section describes scenarios where a DMOS pcell can be used in conjunction with high voltage and low voltage n-epi pockets.

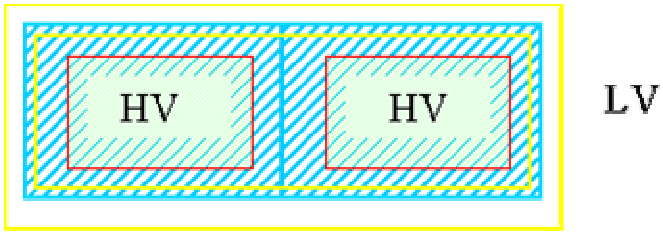
1) HV pocket inside a single LV pocket, or stand alone device.

-Pcell deep pwell isolation option = ON
-Pcell outer Nwell ring optioin = ON



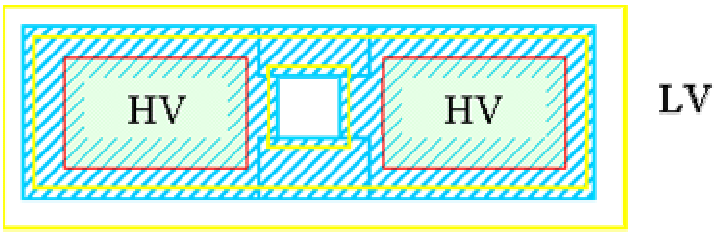
2) Two or more HV pockets merged together.

-Pcell deep pwell isolation option = ON
-Pcell outer Nwell ring option = OFF: Draw Nwell ring manually
-No Nwell ring in between HV pockets
-DPW overlap can be anything from 0 to 6 um



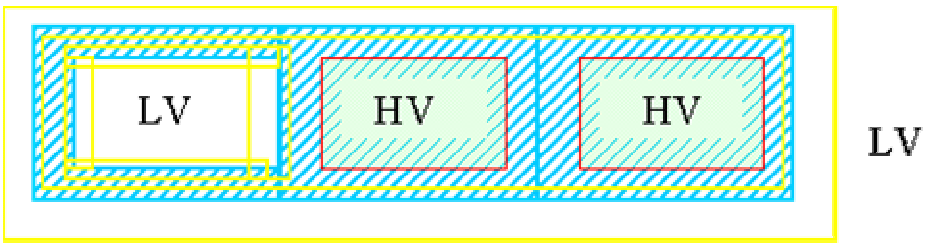
3) Two HV pockets with double guard rings in between for increased latch-up immunity

-Pcell Deep Pwell isolation option = ON
-Pcell outer Nwell ring option = OFF
-Spacing between Pcells = 2.5um min. spacing (outer DPW to DPW, rule 99.2)
-Isolate middle with 2 DPW blocks (min. DPW width LV = 4.5um, rule 99.1)
-Put Nwell in between with 1 um overlap (rule 99.4)
-Put Nwell ring manually around whole structure



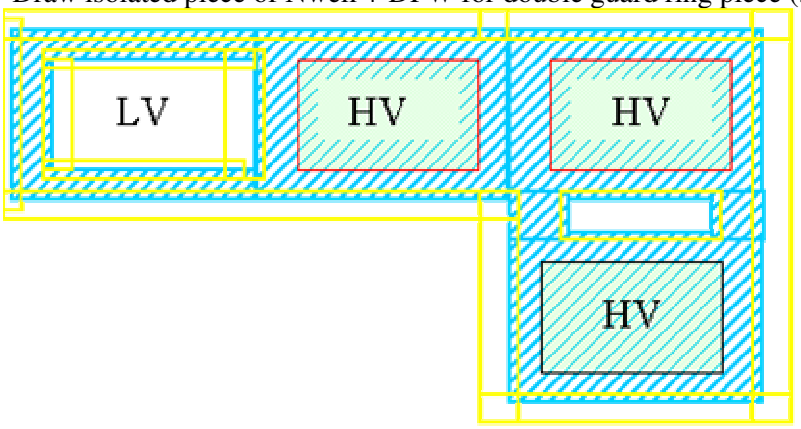
4) HV pocket with LV and merged HV pockets

-Pcell Deep Pwell isolation option = ON
-Pcell outer Nwell ring option = OFF
-Draw Nwell manually around total pocket; 1 um inside DPW (rule 99.4)
-Draw Nwell manually inside LV pocket; 1 um inside DPW (rule 99.4)



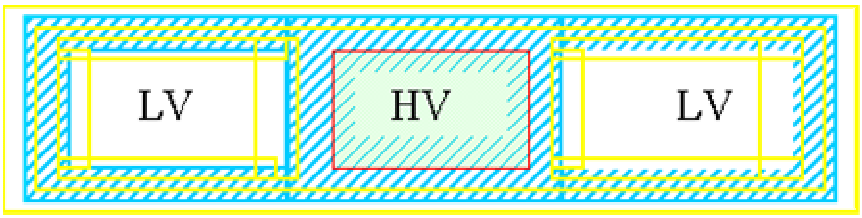
5) HV pocket with LV pocket, merged HV pockets with double guard ring

-Pcell Deep Pwell isolation option = ON
-Pcell outer Nwell ring option = OFF
-Draw different Nwell parts manually around total pocket; 1 um inside DPW (rule 99.4)
-Draw Nwell manually inside LV pocket; 1 um inside DPW (rule 99.4)
-Draw isolated piece of Nwell + DPW for double guard ring piece (see 3 above)



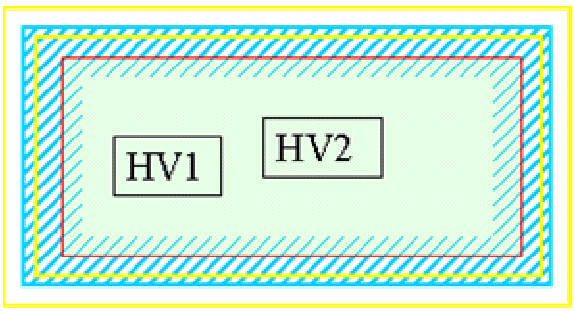
6) HV pocket with two or more LV pockets

-Pcell Deep Pwell isolation option = ON
-Pcell outer Nwell ring option = OFF
-Draw Nwell ring manually around total pocket; 1 um inside DPW (rule 99.4)
-Draw Nwell ring manually inside LV pockets; 1 um inside DPW (rule 99.4)
***Note: if Pcell outer Nwell ring option would be ON, then LV pockets would be shorted!



7) HV pocket with two or more devices inside

-Pcell Deep Pwell isolation option = OFF
-Pcell outer Nwell ring option = Not Applicible
-Draw DPW ring manually around area; minimum 6um wide (rule 99.10).
-Draw Not_Pwell layer within entire HV nepi pocket, 1um inside DPW (rule 8.3)
-Draw Nwell ring manually around total pocket; 1 um inside DPW (rule 99.4)



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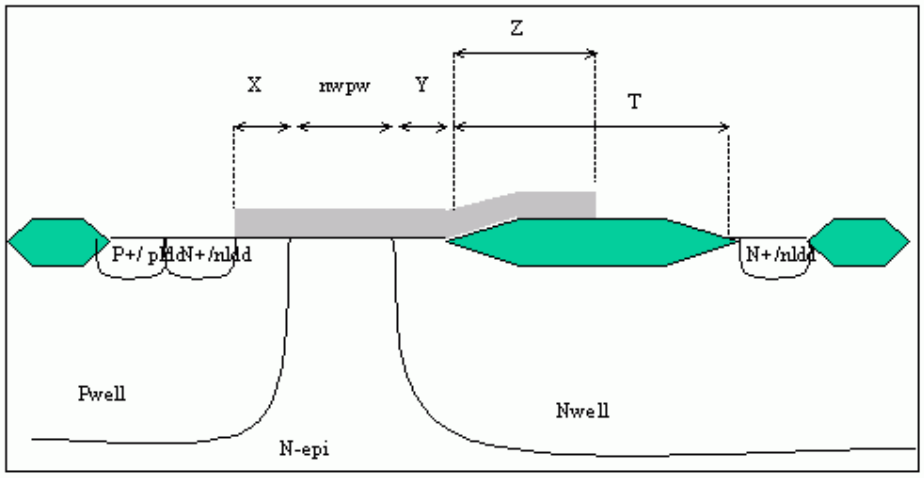
I3T25 (0.35 Micron) NDMOS THINGATE TRANSISTOR Layout Rules

Cross-section:



Note 1: lfndm25
Note 2: For LPDM12, LFNDM, LFPDM LNNDM15 and LFNDM14 DMOS devices, the electrical characteristics are strongly orientation dependent. Whenever matching between these DMOS devices is important, they should be oriented in the same direction. Use of dual finger devices is recommended.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
NTN25.1	Fixed POLY gate spacing to N+ ACTIVE drain (T-Z). *Only for the POLY side intersecting the NWELL	0.50	µm	*	
NTN25.2	Fixed POLY gate intersection with PWIMP, in active area (X)	0.80	µm	*	
NTN25.3	Fixed POLY gate intersection with NWELL at drain side (Y+Z)	0.00	µm	*	
NTN25.4	Fixed POLY gate length (X+PWNW+Y+Z)	2.20	µm	*	
NTN25.5	Fixed spacing between NWELL drain and PWIMP	1.40	µm	*	
NTN25.6	Fixed POLY gate intersection with N+ ACTIVE source (X+PWNW+Y)	1.70	µm	*	
NTN25.7	Fixed spacing between N+ ACTIVE source and drain (T)	1.00	µm	*	
NTN25.8	Fixed spacing between PPLUS bulk to POLY gate edge	0.80	µm	*	
NTN25.9	Fixed POLY edge to source contact spacing	0.40	µm	*	
NTN25.10	Minimum poly gate width	5.00	µm	*	
NTN25.11	Minimum PWIMP enclosure of N+active, except side overlapped by poly gate (NDMOS channel)	0.80	µm	*	

NTN25.12	Poly silicon gate running ACTIVE AREA corners are allowed			*	This is an exception to Rule 13.5 of the core CMOS set.

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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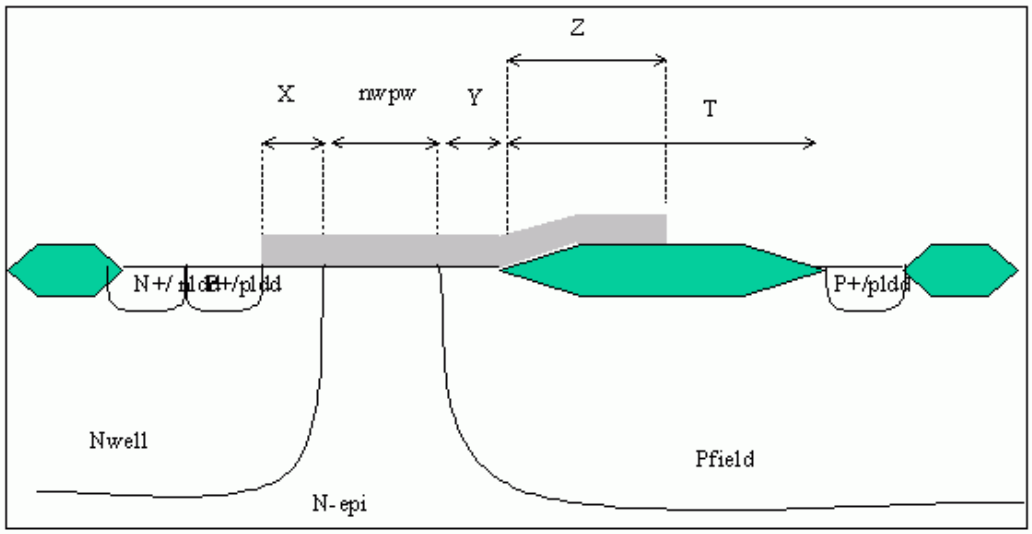
I3T25 (0.35 Micron) PDMOS THINGATE TRANSISTOR Layout Rules

Cross-section:



Note 1: lfpdm25
Note 2: For LPDM12, LFNDM, LFPDM LNNDM15 and LFNDM14 DMOS devices, the electrical characteristics are strongly orientation dependent. Whenever matching between these DMOS devices is important, they should be oriented in the same direction. Use of dual finger devices is recommended.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
PTN25.1	Fixed POLY gate spacing to P+ ACTIVE drain (T-Z). *Only for the POLY side overlapping the PFIELD	0.45	µm	*	
PTN25.2	Fixed POLY gate intersection with NWELL, in active area (X)	0.80	µm	*	
PTN25.3	Fixed POLY gate intersection with PFIELD at drain side (Y+Z)	0.85	µm	*	
PTN25.4	Fixed POLY gate length (X+PWNW+Y+Z)	1.65	µm	*	
PTN25.5	Fixed spacing between PFIELD drain and NWELL	0.00	µm	*	
PTN25.6	Fixed POLY gate intersection with P+ ACTIVE source (X+PWNW+Y)	1.20	µm	*	
PTN25.7	Fixed spacing between P+ ACTIVE source and drain (T)	0.90	µm	*	
PTN25.8	Fixed spacing between POLY gate edge and N+ active bulk, if abutted with source active	1.00	µm	*	
PTN25.9	Fixed POLY edge to source contact spacing	0.30	µm	*	
PTN25.10	Minimum poly gate width	5.00	µm	*	
PTN25.11	Minimum PFIELD spacing to P+active	1.50	µm	*	

PTN25.12	Minimum NWELL enclosure of free P+ active area, except side overlapped by poly gate (PDMOS channel)	0.80	µm	*	
PTN25.13	Poly silicon gate running ACTIVE AREA corners are allowed			*	This is an exception to Rule 13.5 of the core CMOS set.

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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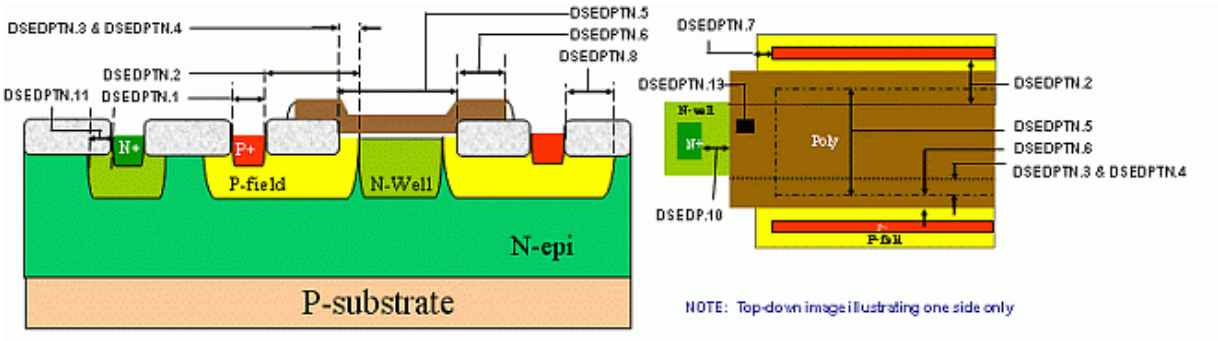
I3T25 (0.35 Micron) PDMOS THIN-GATE DOUBLE-SIDED EXTENDED-DRAIN Layout Rules



Note 1: (LFPDM25D)

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
DSEDPTN.1	Minimum width of p+ active	0.80	µm	*	
DSEDPTN.2	Fixed p+ active spacing to nwell under poly	1.30	µm	*	
DSEDPTN.3	Fixed pfield intersection with active (under poly)	0.40	µm	*	
DSEDPTN.4	Fixed active (under poly) extension beyond nwell	0.40	µm	*	
DSEDPTN.5	Minimum active (under poly) width	3.00	µm	*	
DSEDPTN.6	Minimum poly enclosure of active	0.45	µm	*	
DSEDPTN.7	Minimum pfield enclosure of p+ active (not under poly)	1.30	µm	*	
DSEDPTN.8	Minimum pfield enclosure of p+ active (side opposite gate)	2.10	µm	*	
DSEDPTN.9	Minimum gate width	5.00	µm	*	
DSEDPTN.10	Minimum poly spacing to n+ active	1.00	µm	*	
DSEDPTN.11	Minimum nwell enclosure of N+ active (Bulk)	0.40	µm	*	
DSEDPTN.12	N+ active (bulk) ring must enclose the device			*	
DSEDPTN.13	Poly contacts must be placed on both sides of gate			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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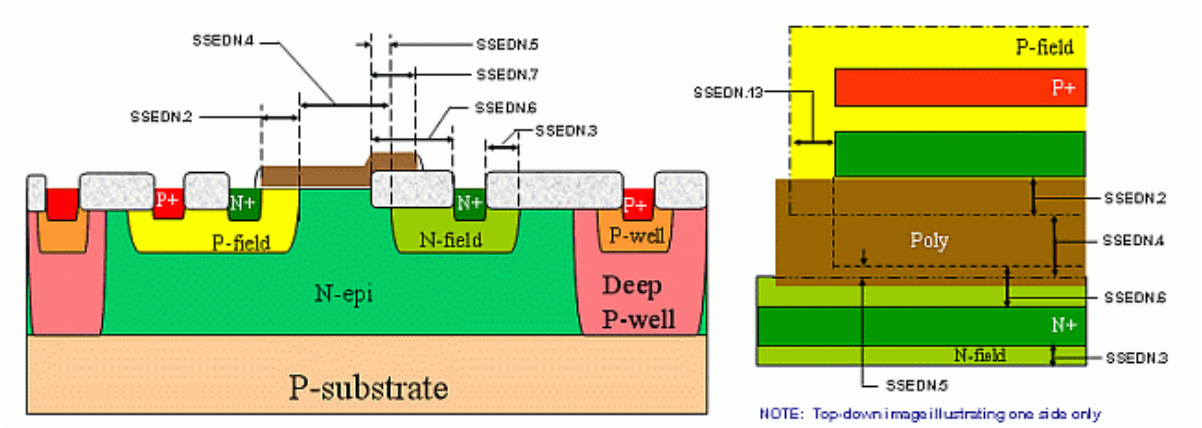
I3T25 (0.35 Micron) NDMOS THICK-GATE SINGLE-SIDED EXTENDED-DRAIN Layout Rules



Note 1: (LFNDM25T)

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
SSEDN.1	Fixed width of n+ active (source), if abutted with p+ active (bulk)	0.80	µm	*	
SSEDN.2	Fixed pfield intersection with poly gate	0.80	µm	*	
SSEDN.3	Minimum nfield enclosure of n+ active (drain)	0.45	µm	*	
SSEDN.4	Fixed nfield (drain extension) spacing to pfield	1.40	µm	*	
SSEDN.5	Minimum nfield (drain extension) spacing to active (under poly)	0.30	µm	*	
SSEDN.6	Fixed active (under poly) spacing to n+ active (drain)	0.90	µm	*	
SSEDN.7	Fixed poly gate extension beyond active	0.45	µm	*	
SSEDN.9	Minimum gate width	5.00	µm	*	
SSEDN.11	Active/Nfield (drain) ring must enclose device			*	
SSEDN.12	thox must be coincident with not_pwell			*	
SSEDN.13	Minimum pfield extension beyond n+ active (source), NOT under poly gate	1.50	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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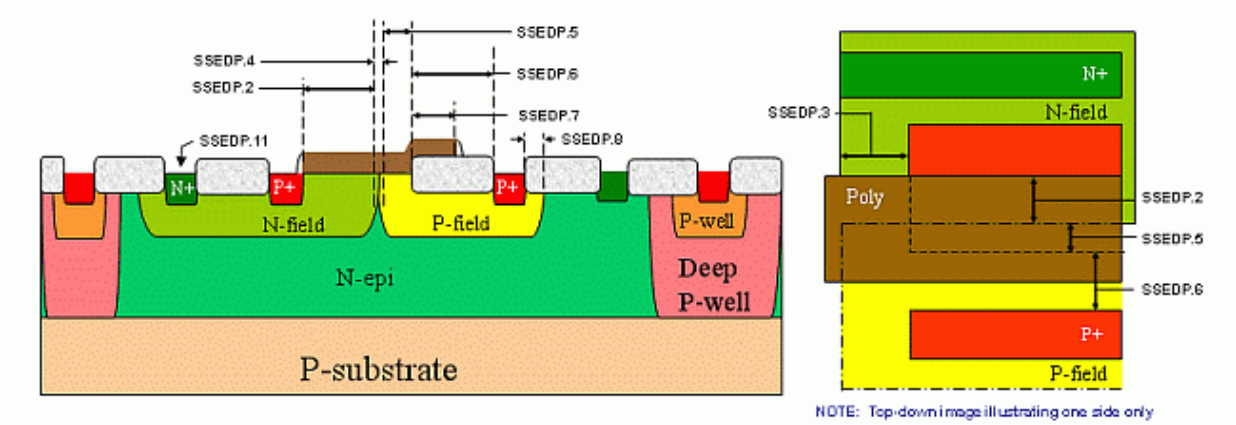
I3T25 (0.35 Micron) PDMOS THICK-GATE SINGLE-SIDED EXTENDED-DRAIN Layout Rules



Note 1: (LFPDM25T)
Note 2: HV keep out mark required in the area adjacent to both source and gate connection to prevent parasitic MOS

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
SSEDP.1	Fixed width of p+ active (source), if abutted with n+ active (bulk)	1.00	µm	*	
SSEDP.2	Fixed nfield intersection with poly gate	0.80	µm	*	
SSEDP.3	Minimum nfield extension beyond p+ active (source), NOT under poly gate	2.00	µm	*	
SSEDP.4	Fixed pfield (drain extension) spacing to nfield under poly gate	0.00	µm	*	
SSEDP.5	Minimum pfield (drain extension) intersection with active (under poly)	0.40	µm	*	
SSEDP.6	Fixed active (under poly) spacing to p+ active (drain)	0.90	µm	*	
SSEDP.7	Fixed poly gate extension beyond active	0.45	µm	*	
SSEDP.8	Minimum pfield enclosure of p+ active (drain)	1.00	µm	*	
SSEDP.9	Minimum p+ active (source) contact spacing to poly gate	0.40	µm	*	
SSEDP.10	Minimum gate width	5.00	µm	*	
SSEDP.11	N+ active (bulk) ring must enclose the device			*	
SSEDP.12	Minimum nfield spacing to deep_pwell	5.00	µm	*	
SSEDP.13	Minimum active spacing to deep_pwell	5.00	µm	*	

SSEDP.14	thox must be coincident with not_pwell			*	
SSEDP.15	This device does not allow multi-finger layout. Multi-finger layout LFPDM25T on silicon will not match simulation result from the model.			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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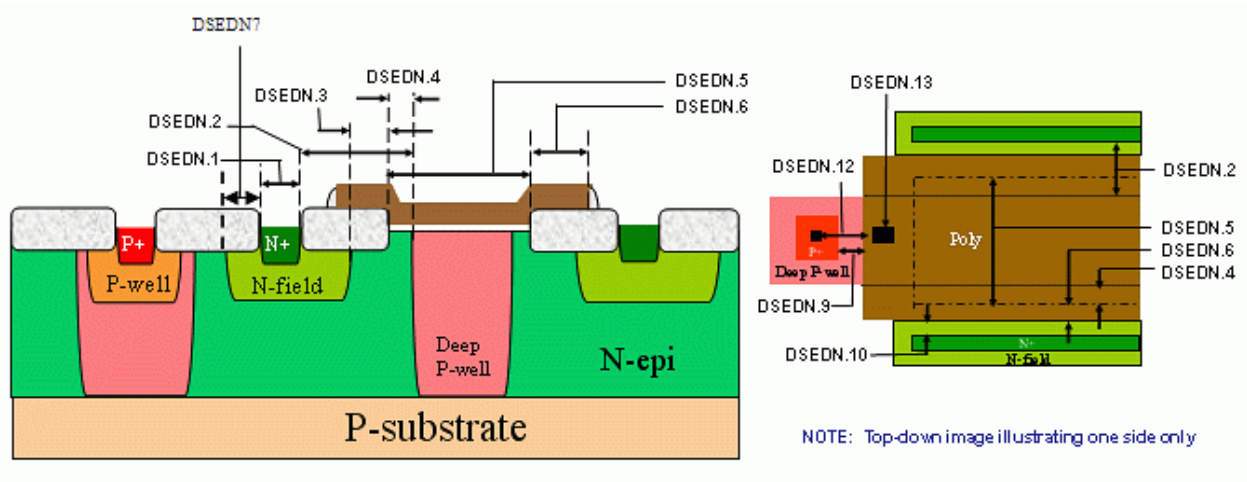
I3T25 (0.35 Micron) NDMOS THICK-GATE DOUBLE-SIDED EXTENDED-DRAIN Layout Rules



Note 1: (LFNDM25DT)

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
DSEDN.1	Minimum width of n+ active (source/drain)	0.80	µm	*	
DSEDN.2	Fixed n+ active spacing to deep pwell under poly	1.80	µm	*	
DSEDN.3	Fixed nfield spacing to active (under poly)	0.50	µm	*	
DSEDN.4	Fixed active (under poly) extension beyond deep pwell	0.90	µm	*	
DSEDN.5	Minimum active (under poly) width	7.80	µm	*	
DSEDN.6	Minimum poly enclosure of active	0.45	µm	*	
DSEDN.7	Minimum nfield enclosure of n+ active (not under poly)	0.50	µm	*	
DSEDN.8	Minimum gate width	5.00	µm	*	
DSEDN.9	Minimum poly spacing to p+ active	0.50	µm	*	
DSEDN.10	Minimum nfield enclosure of n+ active	0.40	µm	*	
DSEDN.12	Maximum deep_pwell contact spacing to each end of gate	1.30	µm	*	
DSEDN.13	Poly contacts must be placed on both sides of gate			*	
DSEDN.14	thox must be coincident with not_pwell			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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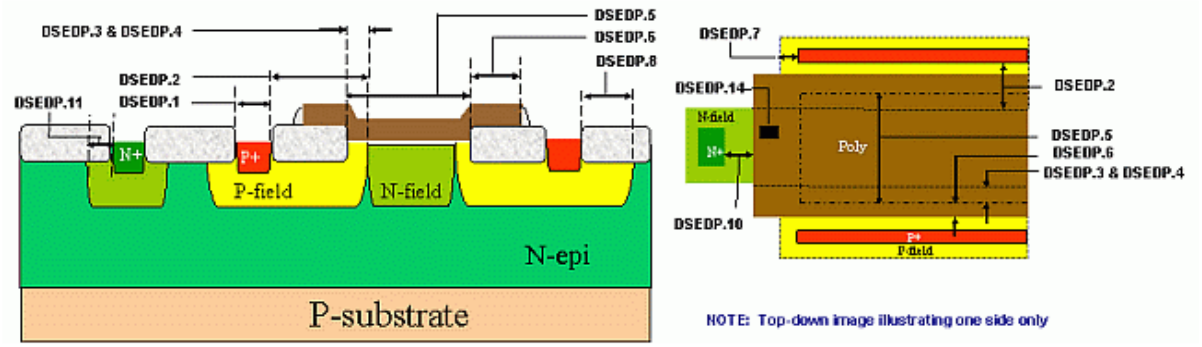
I3T25 (0.35 Micron) PDMOS THICK-GATE DOUBLE-SIDED EXTENDED-DRAIN Layout Rules



Note 1: (LFPDM25DT)

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
DSEDP.1	Minimum width of p+ active	0.80	µm	*	
DSEDP.2	Fixed p+ active spacing to nfield under poly	1.40	µm	*	
DSEDP.3	Fixed pfield intersection with active (under poly)	0.50	µm	*	
DSEDP.4	Fixed active (under poly) extension beyond nfield	0.50	µm	*	
DSEDP.5	Minimum active (under poly) width	2.40	µm	*	
DSEDP.6	Minimum poly enclosure of active	0.45	µm	*	
DSEDP.7	Minimum pfield enclosure of p+ active (not under poly)	1.30	µm	*	
DSEDP.8	Minimum pfield enclosure of p+ active (side opposite gate)	2.10	µm	*	
DSEDP.9	Minimum gate width	5.00	µm	*	
DSEDP.10	Minimum poly spacing to n+ active	1.00	µm	*	
DSEDP.11	Minimum nfield enclosure of N+ active (Bulk)	0.40	µm	*	
DSEDP.14	Poly contacts must be placed on both sides of gate			*	
DSEDP.15	thox must be coincident with not_pwell			*	
DSEDP.16	N+ active (bulk) ring must enclose the device			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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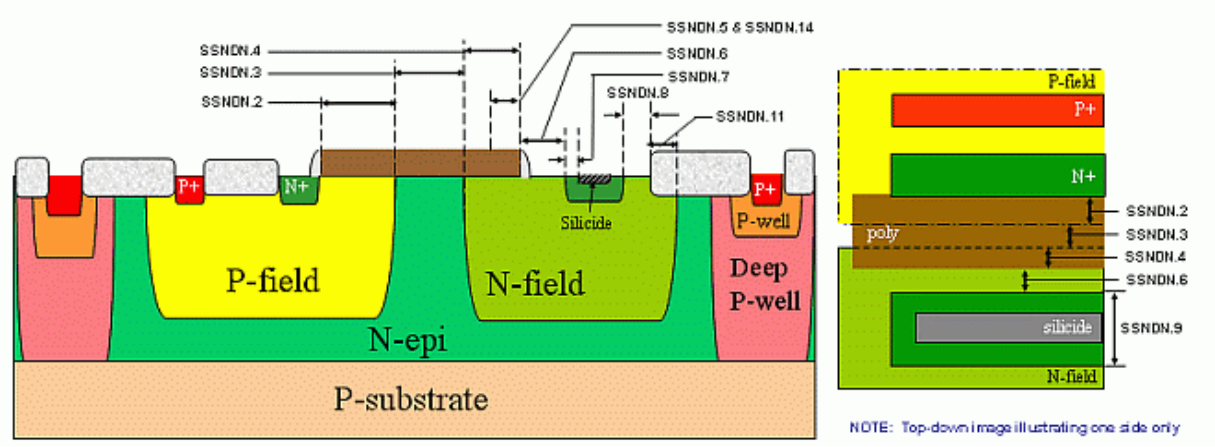
I3T25 (0.35 Micron) NDMOS THICK-GATE SINGLE-SIDED NESTED-DRAIN Layout Rules



Note 1: (LFNDM20NT)
Note 2: NBLK combined layers include nlddprot and nplusprot

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
SSNDN.1	Fixed width of n+ active (source), if abutted with p+ active (bulk)	0.80	µm	*	
SSNDN.2	Fixed pfield intersection with poly gate	0.80	µm	*	
SSNDN.3	Fixed pfield spacing to nfield (drain) under poly gate	0.40	µm	*	
SSNDN.4	Fixed nfield intersection with poly gate	0.40	µm	*	
SSNDN.5	Minimum siprot intersection with poly gate (drain side)	0.20	µm	*	
SSNDN.6	Fixed Nldd spacing to poly gate	0.40	µm	*	
SSNDN.7	Fixed siprot intersection with all edges of nldd	0.40	µm	*	
SSNDN.8	Minimum active enclosure of nldd (not next to gate)	0.30	µm	*	
SSNDN.9	Minimum width of nldd	1.90	µm	*	
SSNDN.11	Minimum nfield extension beyond active (drain), NOT under poly gate	1.00	µm	*	
SSNDN.12	Minimum gate width	5.00	µm	*	
SSNDN.13	Minimum NBLK extension beyond n+ active (drain - not next to gate).	0.90	µm	*	
SSNDN.14	Fixed NBLK intersection with poly gate	0.20	µm	*	
SSNDN.17	thox must be coincident with not_pwell			*	
SSNDN.18	N+ Active drain ring must enclose device			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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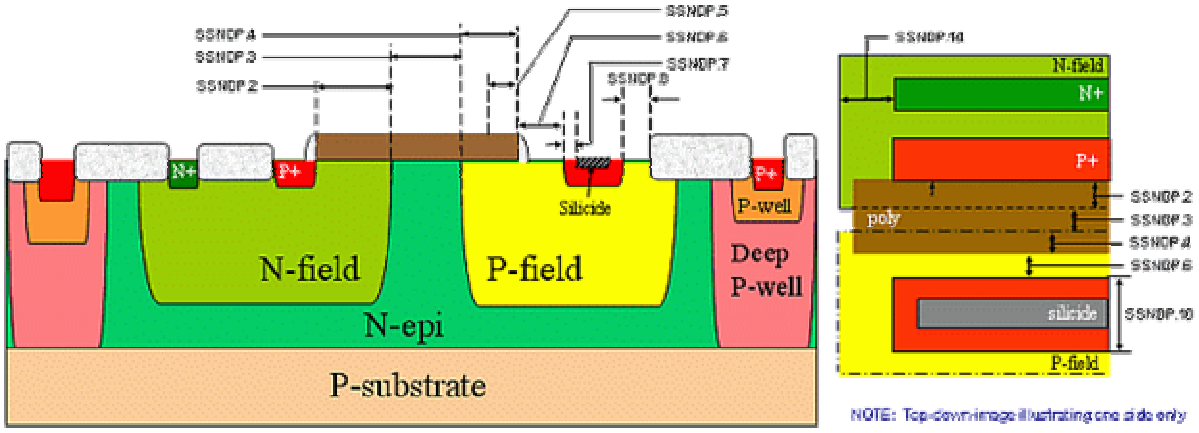
I3T25 (0.35 Micron) PDMOS THICK-GATE SINGLE-SIDED NESTED-DRAIN Layout Rules



Note 1: (LFPDM20NT)
Note 2: NBLK combined layers include nlddprot and nplusprot

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
SSNDP.1	Fixed width of p+ active (source), if abutted with n+ active (bulk)	0.70	µm	*	
SSNDP.2	Fixed nfield intersection with poly gate	0.80	µm	*	
SSNDP.3	Fixed nfield spacing to pfield (drain) under poly gate	0.20	µm	*	
SSNDP.4	Fixed pfield intersection with poly gate	0.30	µm	*	
SSNDP.5	Minimum siprot intersection with poly gate (drain side)	0.20	µm	*	
SSNDP.6	Fixed poly gate spacing to pplus (drain)	0.40	µm	*	
SSNDP.7	Fixed siprot intersection with all edges of pplus of drain	0.40	µm	*	
SSNDP.8	Fixed active enclosure of pplus (drain (not next to gate))	0.30	µm	*	
SSNDP.9	Minimum p+ active (source) contact spacing to poly gate	0.50	µm	*	
SSNDP.10	Minimum width of pplus (drain)	1.90	µm	*	
SSNDP.11	Minimum pplus intersection with poly gate (source side)	1.10	µm	*	
SSNDP.12	Minimum pfield extension beyond active (drain), NOT under poly gate	1.10	µm	*	
SSNDP.13	Minimum gate width	5.00	µm	*	
SSNDP.14	Minimum nfield enclosure of n+ active (bulk)	1.10	µm	*	
SSNDP.15	Minimum NBLK extension beyond active (drain) (not next to gate)	0.90	µm	*	
SSNDP.16	Fixed NBLK intersection with active (drain) (not next to gate)	0.30	µm	*	

SSNDP.17	Minimum NBLK intersection with poly gate (drain side)	0.20	µm	*	
SSNDP.18	Minimum NBLK intersection with siprot	0.60	µm	*	
SSNDP.19	Minimum nfield spacing to deep_pwell	5.00	µm	*	
SSNDP.20	Minimum pfield spacing to deep_pwell	5.00	µm	*	
SSNDP.21	thox must be coincident with not_pwell			*	
SSNDP.22	This device does not allow multi-finger layout. Multi-finger layout LFPDM20NT on silicon will not match simulation result from the model.			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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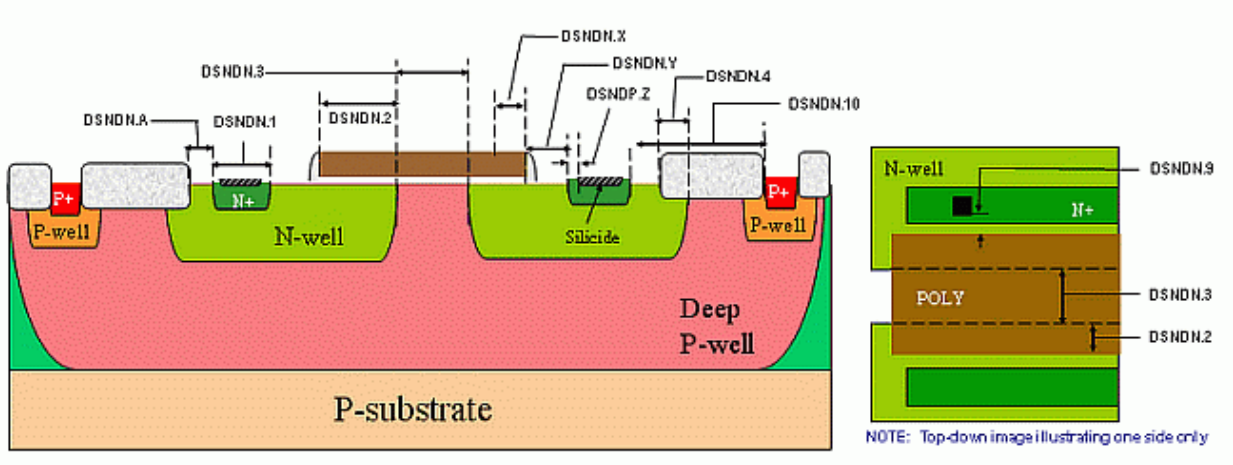
I3T25 (0.35 Micron) NDMOS THICK-GATE DOUBLE-SIDED NESTED-DRAIN Layout Rules



Note 1: (LFNDM20DNT)
Note 2: NBLK combined layers include nlddprot, nogen, and nplusprot

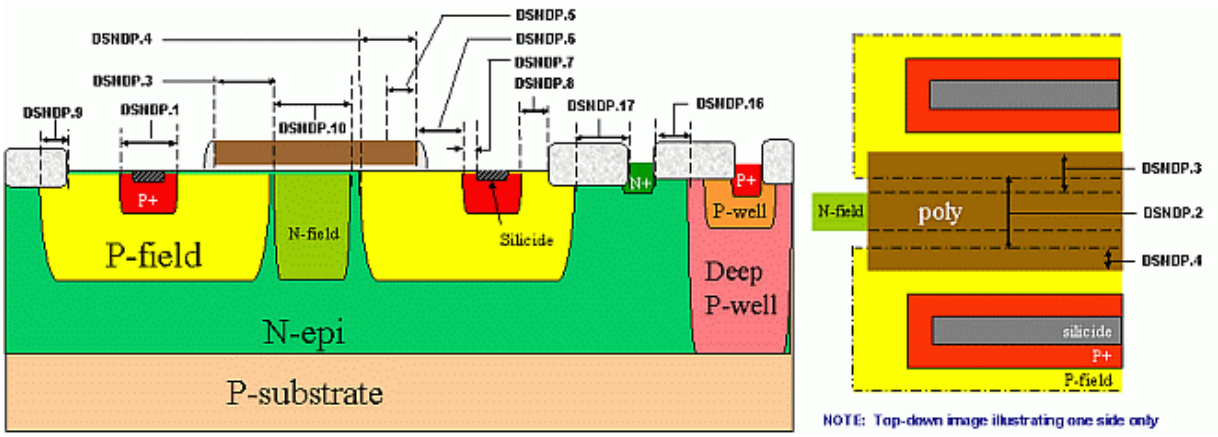
Rule Name	Rule Description	Rule	Units	Rule Type	Notes
DSNDN.1	Minimum width of N+ (source/drain)	1.90	µm	*	
DSNDN.2	Minimum nwell intersection with poly gate	1.40	µm	*	
DSNDN.3	Fixed nwell spacing to nwell under poly gate	2.40	µm	*	
DSNDN.4	Minimum nwell extension beyond active (source/drain), NOT under poly gate	1.10	µm	*	
DSNDN.5	Minimum siprot intersection with poly gate (source/drain side)	0.20	µm	*	
DSNDN.6	Fixed poly gate spacing to Nplus	0.40	µm	*	
DSNDN.7	Fixed siprot intersection with all edges of nplus (source/drain)	0.40	µm	*	
DSNDN.8	Fixed active enclosure of nplus (source/drain), NOT next to gate	0.30	µm	*	
DSNDN.9	Minimum active contact spacing to poly gate	1.15	µm	*	
DSNDN.10	Minimum active to p+ active (bulk) spacing	2.40	µm	*	
DSNDN.11	Minimum deep_pwell enclosure of active	5.80	µm	*	
DSNDN.12	Minimum gate width	5.00	µm	*	
DSNDN.13	Minimum not_pwell enclosure of active	0.80	µm	*	

DSNDN.14	thox must be coincident with not_pwell			*	
DSNDN.15	Minimum NBLK intersection with poly gate (source/drain sides)	0.20	µm	*	
DSNDN.16	Minimum NBLK intersection with siprot (gate sides)	0.60	µm	*	
DSNDN.17	Minimum NBLK intersection with active (not next to gate)	0.30	µm	*	
DSNDN.18	Minimum NBLK extension beyond active (not next to gate)	0.90	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

(Confidential)
1000115 Rev: E, 03-May-2010

I3T25 (0.35 Micron) PDMOS THICK-GATE DOUBLE-SIDED NESTED-DRAIN Layout Rules



Note 1: (LFPDM20DNT)
Note 2: NBLK combined layers include nlddprot and nplusprot

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
DSNDP.1	Minimum width of pplus (source/drain)	1.90	µm	*	
DSNDP.2	Minimum pfield spacing	2.00	µm	*	
DSNDP.3	Fixed poly extension beyond nfield	0.80	µm	*	
DSNDP.4	Fixed pfield intersection with poly gate	0.60	µm	*	
DSNDP.5	Minimum siprot intersection with poly gate (source/drain side)	0.20	µm	*	
DSNDP.6	Fixed poly gate spacing to pplus	0.40	µm	*	
DSNDP.7	Fixed siprot intersection with all edges of pplus (source/drain)	0.40	µm	*	
DSNDP.8	Fixed active enclosure of pplus (source/drain), NOT next to gate	0.30	µm	*	
DSNDP.9	Minimum pfield extension beyond active, NOT under poly gate	1.10	µm	*	
DSNDP.10	Minimum nfield width	1.60	µm	*	
DSNDP.11	Minimum NBLK intersection with poly gate (source/drain sides)	0.20	µm	*	
DSNDP.12	Minimum NBLK intersection with siprot (gate sides)	0.60	µm	*	
DSNDP.13	Minimum NBLK intersection with active (not next to gate)	0.30	µm	*	
DSNDP.14	Minimum NBLK extension beyond active (not next to gate)	0.90	µm	*	
DSNDP.15	Minimum nfield extension beyond active under poly	3.60	µm	*	
DSNDP.16	Minimum n+ active (bulk) spacing to deep_pwell	2.00	µm	*	

DSNDP.17	Minimum n+ active (bulk) to pfield spacing	1.60	µm	*	
DSNDP.18	Minimum n+ active (bulk) to nfield spacing	0.55	µm	*	
DSNDP.19	Minimum gate width	5.00	µm	*	
DSNDP.20	Fixed poly enclosure of pplus	0.20	µm	*	
DSNDP.21	An n+ active bulk ring must surround the device			*	
DSNDP.22	thox must be coincident with not_pwell			*	
DSNDP.23	Nfield bulk must be contacted on both sides of gate			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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I3T25 (0.35 Micron) METAL2-METAL2.5 CAPACITOR Layout Rules

Note 1: (Pcell PC_MIMC and PC_MIMCXW)

Note 2: Refer to DES-0005

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I3T25 (0.35 Micron) METAL-METAL FINGER CAPACITOR Layout Rules

Note 1: (Pcells PC_MMCHB and PC_MMCHBXW)

Note 2: Refer to DES-0005

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I3T25 (0.35 Micron) METAL-METAL SANDWICH CAPACITOR Layout Rules

Note 1: (Pcells PC_ MMCHP and PC_MMCHPXW)

Note 2: Refer to DES-0005

I3T25 (0.35 um) Design Rules

Die Seal Ring Rules

1000115 Rev: E

Confidential

I3T25 Die Seal Ring Rules

Introduction

This section covers the process layout rules for the scribe lane and the edge of die. The introduction covers definitions and general requirements.

Purpose

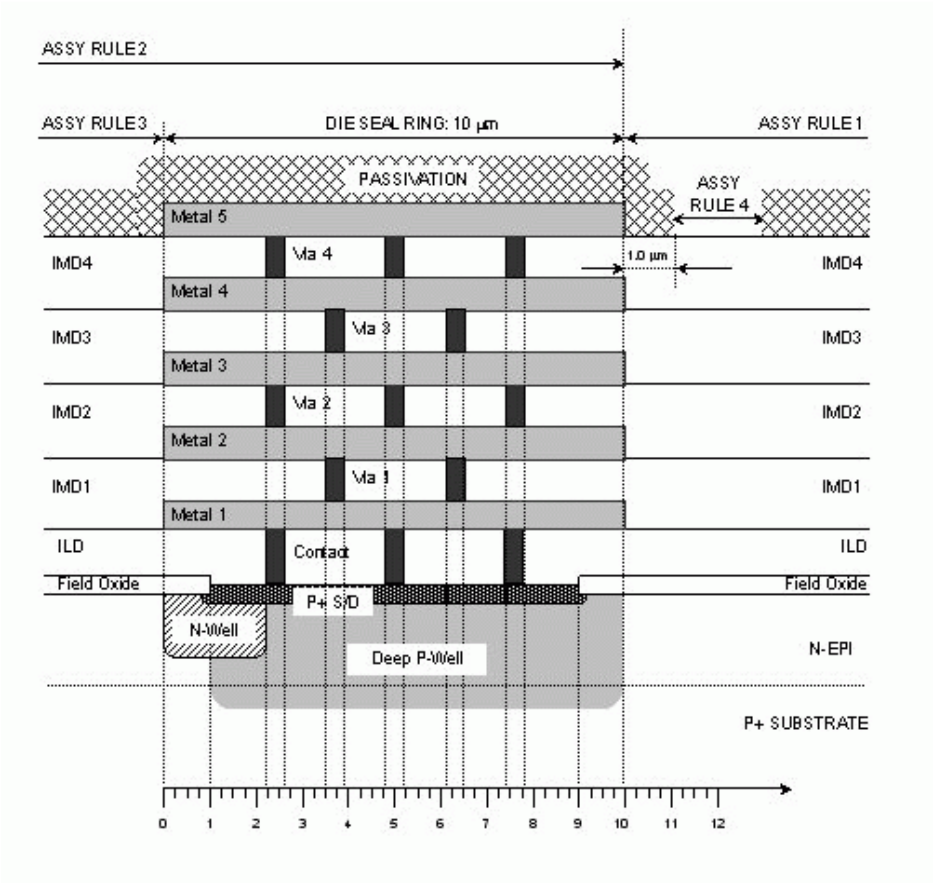
The purpose of this section is to define a scribe lane and an edge of die, which will give a moisture resistant die, without the possibility that cracks generated during sawing can propagate into the die.

Guidelines

For the basic die seal ring rules, refer to the C035U Base Design Rules (DES-0005.) In addition to those rules, we require that the substrate isolation be added with a Deep P-well and an N-well (see figure below.) For the following rules, all dimensions are in microns and refer to the inner edge of the die seal ring.

Edge Seal Layout Rules

	Layer	Drawn ?	From	To
8.2.1	deep pwell	yes	1.0	10.0
8.2.2	nwell	yes	0	2.2



I3T25 (0.35 um) Design Rules

Electrical Design Rules

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I3T25 Electrical Design Rules

HV DMOS Transistors Overview:

Technology	Device	GOX A
I3T25 SG	SSED NDMOS (thin-gate)	71
I3T25 SG	SSED PDMOS (thin-gate)	71
I3T25 DG	SSED NDMOS LFNDM25T	290
I3T25 DG	SSED PDMOS LFNDM25T	290
I3T25 DG	DSED NDMOS LFNDM25DT	290
I3T25 DG	DSED PDMOS LFPDM25DT	290
I3T25 DG	SSND NDMOS LFNDM20NT	290
I3T25 DG	SSND PDMOS LFPDM20NT	290
I3T25 DG	DSND NDMOS LFNDM20DNT	290
I3T25 DG	DSND PDMOS LFPDM20DNT	290

I3T25 Electrical Design Rules

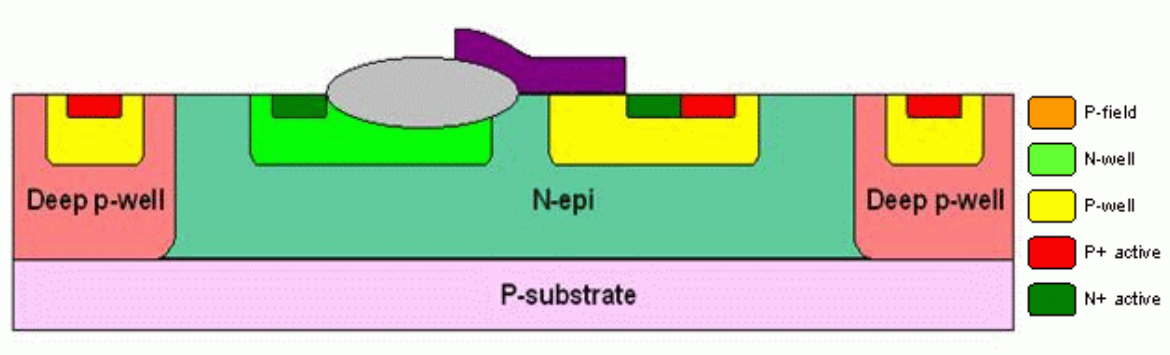
NDMOS Thingate Transistor: lfndm25

The information/rules are for I3T25 only.

Application: Medium voltage switch where drain terminal can raise up to 18 V with respect to the p-substrate.

This device is not self-aligned since the channel is defined by the PWELL overlap under the POLY gate, hence the effective length of the channel is susceptible to misalignment and the characteristics might be orientation dependent. The device source-drain breakdown is sensitive to the length of the free epi extension in active area that is determined by the alignment of the PWELL mask relative to FOX.

Cross-section:

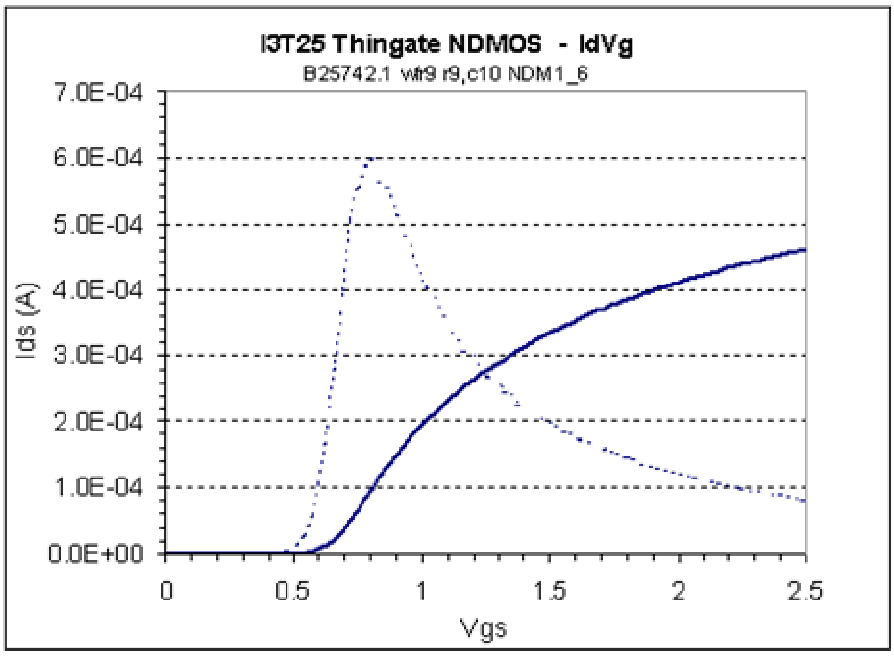


Main electrical features*: for a device of 40 µm width
(*only of indicative value)

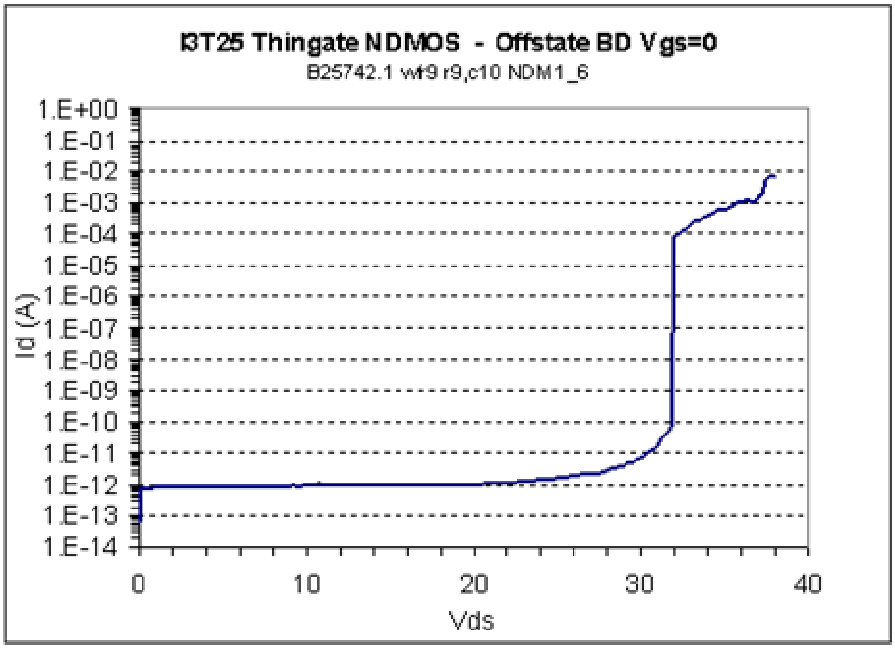
Parameters	Min	Typ	Max	Units
Vt(0)	0.51	0.58	0.643	V
ß(lin) at V_D=0.1	4148	5215	6550	µA/V^2
Slin				mV/dec
Ron @ Vgs=3.3V, Vds=0.5V	174	224	280	Ω
|Vbdl (=Vmax=Vdsmax)	25	31		V
Vgsmax		3.3	3.6	V
Vdsmax		18	19.8	V
Idsat/W at Vgs=3.3V, Vds=18V	230	279	362	µA/µm
TCvt0				mV/K
TCRon				%/K

Electrical characteristics:

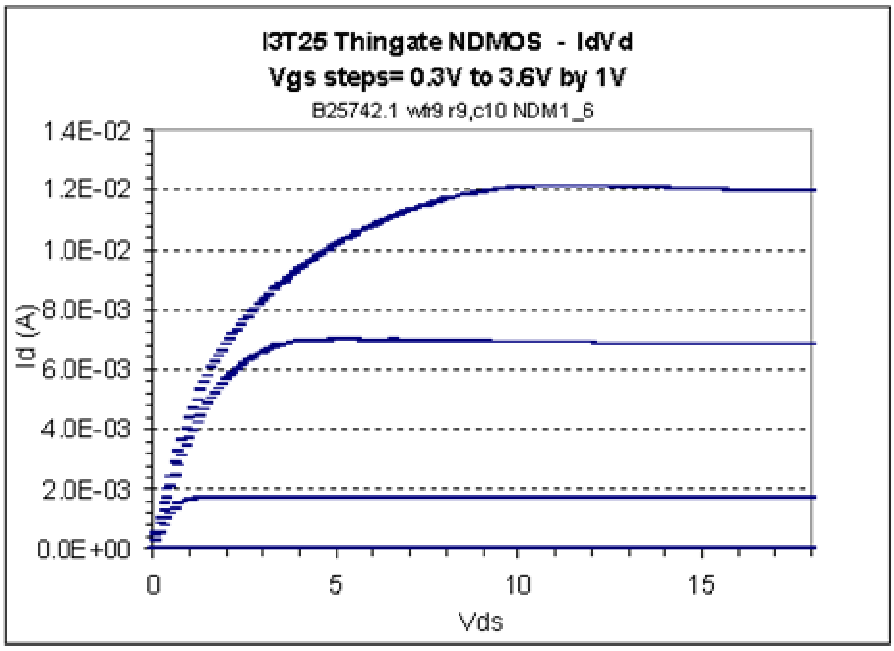
Ids-Vgs at Vds=0.1V (transfer characteristic)



Ids-Vds at Vgs=0V (off state leakage current)



Ids-Vds for different Vgs (output characteristic). Vg going from 0.3 to 3.6 in 1V steps



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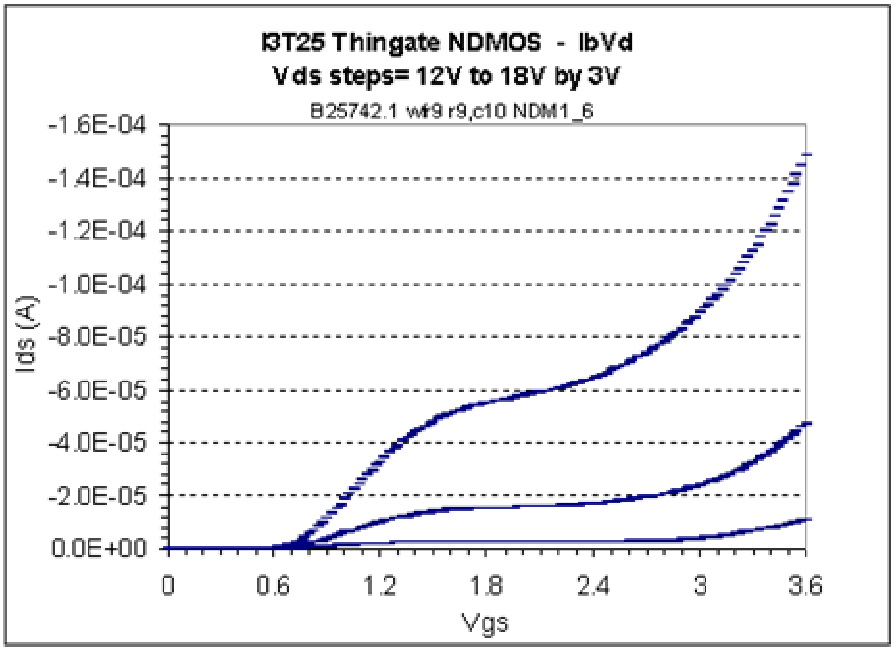
Ibs-Vds for different Vds (bulk current check). Vds going from 12 to 18V in 3V steps.



I3T25 Electrical Design Rules

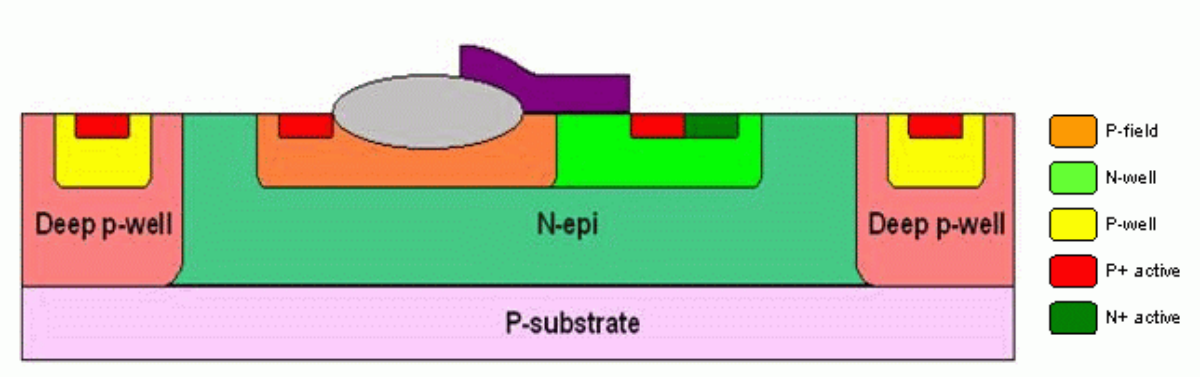
PDMOS Thingate Transistor: lfpdm25

The information/rules are for I3T25 only.

Application: Medium voltage switch where the body terminal can raise up to 18 V with respect to the p-substrate.

This device is not self-aligned since the channel is defined by the NWELL overlap under the POLY gate, hence the effective length of the channel is susceptible to misalignment and the characteristics might be orientation dependent. The device source-drain breakdown is sensitive to the length of the drain extension in active area that is determined by the alignment of the PFIELD mask relative to FOX.

Cross-section:

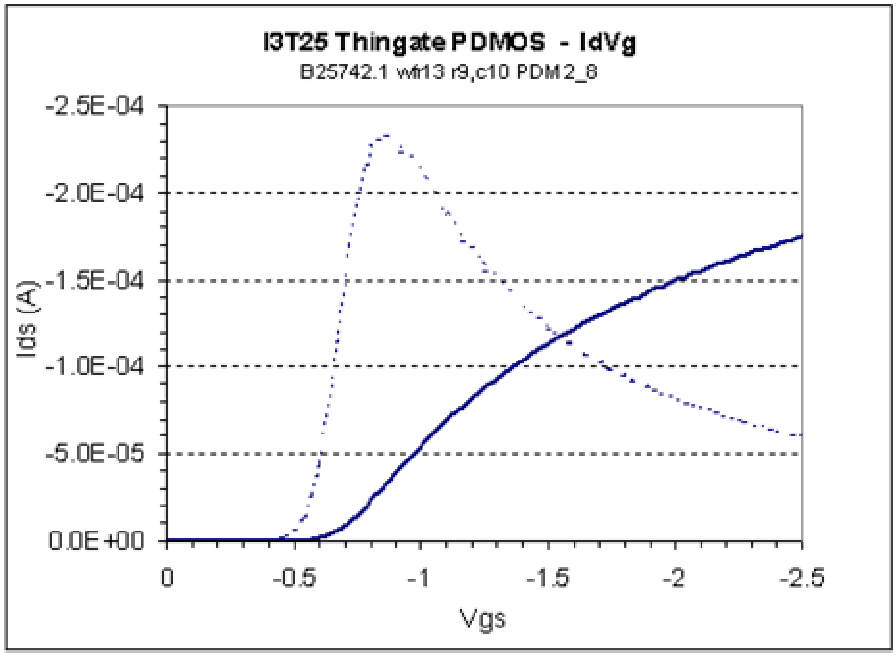


Main electrical features*: for a device of 40 µm width
(*only of indicative value)

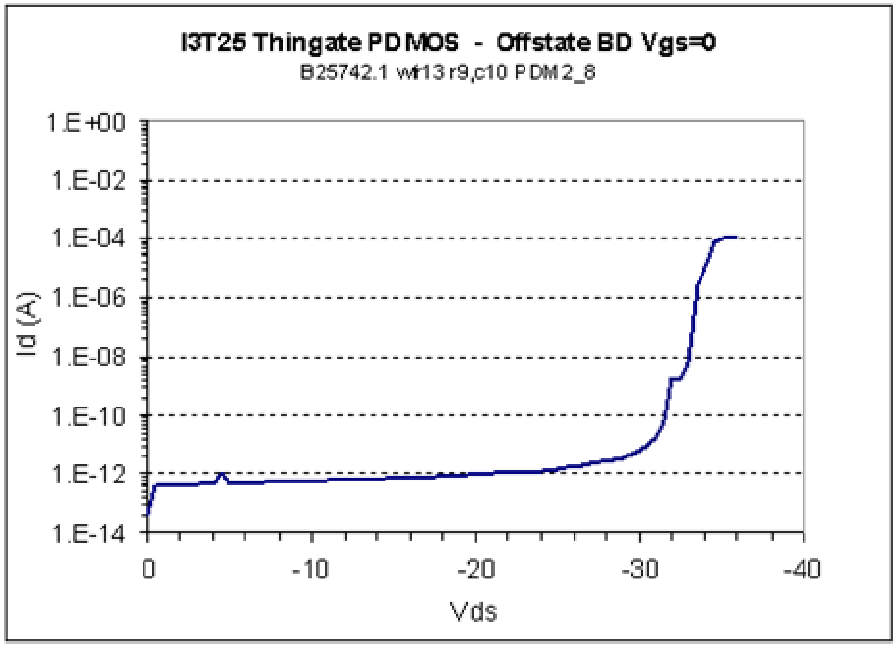
Parameters	Min	Typ	Max	Units
Vt(0)	-0.541	-0.604	-0.702	V
ß(lin)	1241	1811	2380	$\mu A/V^2$
Slin				mV/dec
Ron @ Vgs=3.3V, Vds=0.5V	331	537	767	Ω
|Vbdl (=Vmax=Vdsmax)	25	28.5		V
Vgsmax		3.3	3.6	V
Vdsmax		18	19.8	V
Idsat/W at Vgs=3.3V, Vds=18V	-76	-121.5	-167	µA/µm
TCvt0				mV/K
TCRon				%/K

Electrical characteristics:

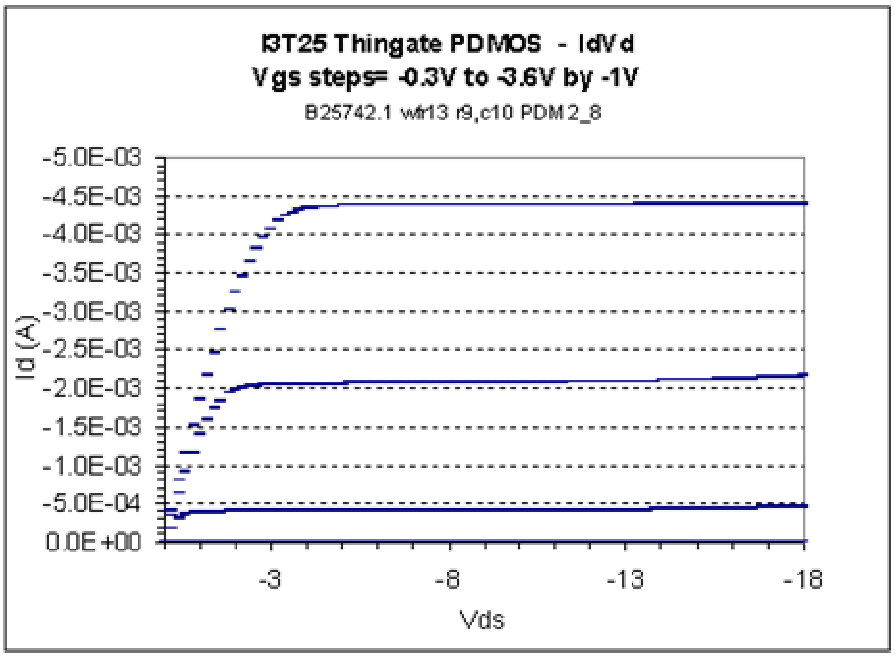
Ids-Vgs at Vds=-0.1V (transfer characteristic)



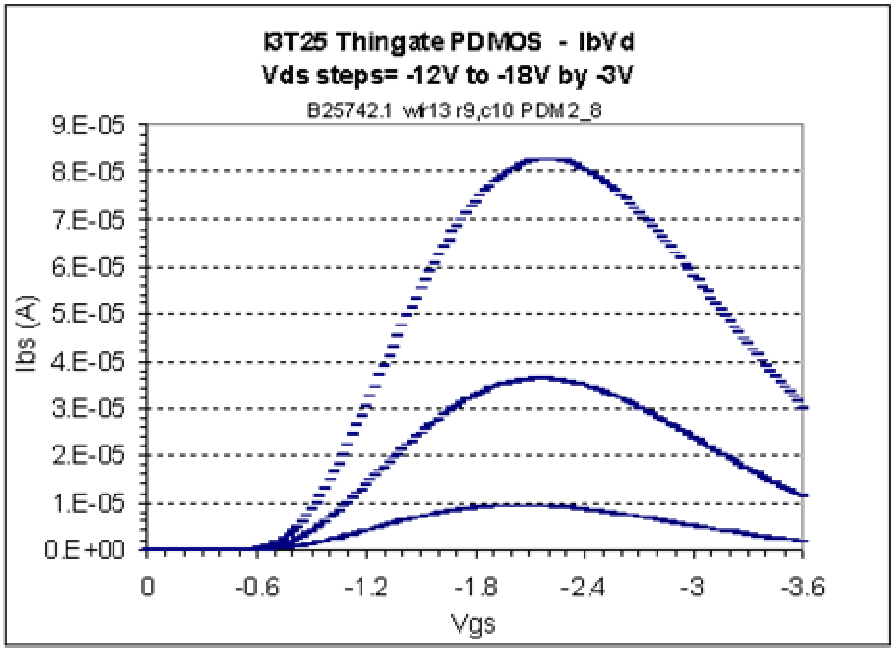
Ids-Vds at Vgs=0V (off state leakage current)



Ids-Vds for different Vgs (output characteristic). Vg going from 0.3 to 3.6 in 1V steps.



Ibs-Vds for different Vds (bulk current check). Vds going from 12 to 18V in 3V steps



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I3T25 DMOS Electrical Parameters: Thin-gate & Thick-gate Devices

Note: The information listed below is for reference only and may not be current (04/29/2010). Current data is located in the ON Semiconductor's Modeling reports, which are located in the PDK at '/lib/amis350uc/tech/spectre/amis350ucakxx/current/doc/'.

Thin-gate DMOS devices:

LFNDM25

Measurement information

To obtain Vt0 for simulations, we run an IdVg simulation, where Vg is biased at 0.1V and Vg is swept from 0 to 2V. We then find the intercepting Vg axis crossing. This is Vt0.
Idsat bias conditions are 18V for Vd and 3.3V for Vg.
Ron bias conditions are 0.5V for Vd and 3.3V for Vg.

Model-silicon verification

Temp = 27C				Simulation				
Device_w		ETEST	Automatic_data	awcs		typ	awcp	
NDMOS_40	Vt0	n/a	0.575			6.22E-01		
	Ron_0.1_3.3	n/a	2.136E+02	2.841E+02	24.00%	2.23E+02	1.754E+02	23.97%
	Idsat_3.3	n/a	1.148E-02	9.130E-03	27.82%	1.21E-02	1.445E-02	17.87%
NDMOS_20	Vt0	n/a	0.576			6.22E-01		
	Ron_0.1_3.3	n/a	4.370E+02	5.668E+02	23.76%	4.46E+02	3.497E+02	24.31%
	Idsat_3.3	n/a	5.872E-03	4.560E-03	27.92%	6.04E-03	7.230E-03	17.94%
NDMOS_10	Vt0	n/a	0.578			6.22E-01		
	Ron_0.1_3.3	n/a	8.530E+02	1.134E+03	23.67%	8.94E+02	7.010E+02	24.17%
	Idsat_3.3	n/a	3.001E-03	2.280E-03	27.92%	3.02E-03	3.610E-03	17.80%
NDMOS_7	Vt0	n/a	0.576			6.22E-01		
	Ron_0.1_3.3	n/a	1.194E+03	1.619E+03	23.67%	1.28E+03	1.001E+03	24.17%
	Idsat_3.3	n/a	2.122E-03	1.600E-03	27.49%	2.11E-03	2.530E-03	18.10%
NDMOS_5	Vt0	n/a	0.582			6.21E-01		
	Ron_0.1_3.3	n/a	1.638E+03	2.267E+03	23.67%	1.79E+03	1.402E+03	24.17%
	Idsat_3.3	n/a	1.519E-03	1.140E-03	27.92%	1.51E-03	1.810E-03	18.07%
NDMOS_3	Vt0	n/a	0.583			6.24E-01		
	Ron_0.1_3.3	n/a	2.642E+03	3.779E+03	23.67%	2.98E+03	2.337E+03	24.17%
	Idsat_3.3	n/a	9.040E-04	6.846E-04	27.84%	9.06E-04	1.080E-03	17.52%
NDMOS_2	Vt0	n/a	0.577			6.21E-01		
	Ron_0.1_3.3	n/a	3.828E+03	5.668E+03	23.68%	4.47E+03	3.505E+03	24.17%
	Idsat_3.3	n/a	5.958E-04	4.564E-04	27.84%	6.04E-04	7.227E-04	17.89%
NDMOS_1	Vt0	n/a	0.578			6.21E-01		
	Ron_0.1_3.3	n/a	7.214E+03	1.134E+04	23.67%	8.94E+03	7.010E+03	24.17%
	Idsat_3.3	n/a	2.863E-04	2.282E-04	27.84%	3.02E-04	3.613E-04	17.89%
NDMOS_0.8	Vt0	n/a	0.578			6.28E-01		
	Ron_0.1_3.3	n/a	8.974E+03	1.417E+04	23.66%	1.12E+04	8.763E+03	24.16%
	Idsat_3.3	n/a	2.227E-04	1.826E-04	27.84%	2.42E-04	2.891E-04	17.89%

Table LFNDM25 Measured vs. Simulation Data Comparison at 27C

LFPDM25

Measurement information

To obtain Vt0 for simulations, we run an IdVg simulation, where Vg is biased at -0.1V and Vg is swept from 0 to -2V. We then find the intercepting Vg axis crossing. This is Vt0.
Idsat bias conditions are -18V for Vd and -3.3V for Vg.
Ron bias conditions are -0.5V for Vd and -3.3V for Vg.

Model-silicon verification

Temp = 27C				Simulation				
Device_w		ETEST	Automatic_data	awcs		typ	awcp	
PDMOS_40	Vt0	n/a	0.639			6.56E-01		
	Ron_0.1_3.3	n/a	5.507E+02	7.736E+02	35.45%	5.41E+02	3.311E+02	48.07%
	Idsat_3.3	n/a	4.867E-03	3.010E-03	48.17%	4.92E-03	6.650E-03	29.90%
PDMOS_20	Vt0	n/a	0.643			6.60E-01		
	Ron_0.1_3.3	n/a	1.111E+03	1.551E+03	35.45%	1.08E+03	6.664E+02	47.69%
	Idsat_3.3	n/a	2.444E-03	1.500E-03	47.72%	2.44E-03	3.300E-03	29.97%
PDMOS_10	Vt0	n/a	0.647			6.66E-01		
	Ron_0.1_3.3	n/a	2.289E+03	3.113E+03	35.45%	2.18E+03	1.340E+03	47.55%
	Idsat_3.3	n/a	1.211E-03	7.381E-04	47.67%	1.20E-03	1.630E-03	30.39%
PDMOS_7	Vt0	n/a	0.642			6.68E-01		
	Ron_0.1_3.3	n/a	3.337E+03	4.460E+03	35.44%	3.12E+03	1.921E+03	47.46%
	Idsat_3.3	n/a	8.396E-04	5.118E-04	47.96%	8.35E-04	1.130E-03	30.07%
PDMOS_5	Vt0	n/a	0.645			6.71E-01		
	Ron_0.1_3.3	n/a	4.778E+03	6.263E+03	35.45%	4.38E+03	2.701E+03	47.34%
	Idsat_3.3	n/a	5.918E-04	3.617E-04	47.95%	5.90E-04	7.989E-04	30.10%
PDMOS_3	Vt0	n/a	0.644			6.75E-01		
	Ron_0.1_3.3	n/a	8.239E+03	1.049E+04	35.45%	7.33E+03	4.536E+03	47.15%
	Idsat_3.3	n/a	3.464E-04	2.131E-04	47.93%	3.47E-04	4.708E-04	30.15%
PDMOS_2	Vt0	n/a	0.639			6.78E-01		
	Ron_0.1_3.3	n/a	1.291E+04	1.581E+04	35.41%	1.11E+04	6.846E+03	47.01%
	Idsat_3.3	n/a	2.202E-04	1.399E-04	47.92%	2.28E-04	3.092E-04	30.19%
PDMOS_1	Vt0	n/a	0.628			6.80E-01		
	Ron_0.1_3.3	n/a	2.819E+04	3.185E+04	35.43%	2.23E+04	1.383E+04	46.74%
	Idsat_3.3	n/a	9.997E-05	6.825E-05	47.92%	1.11E-04	1.509E-04	30.25%
PDMOS_0.8	Vt0	n/a	0.632			6.81E-01		
	Ron_0.1_3.3	n/a	3.651E+04	3.990E+04	35.46%	2.79E+04	1.733E+04	46.69%
	Idsat_3.3	n/a	7.694E-05	5.423E-05	47.91%	8.84E-05	1.200E-04	30.29%

Table LFPDM25 Measured vs. Simulation Data Comparison at 27C

LFPDM25D

Measurement information

Measurement condition of *id-vg*: VDS=-0.1V; VGS is swept from 0V to -3.3V at a step of -0.033V while VBS is biased at 0V, 1.65V and 3.3V respectively.
Measurement condition of *id-vd*: VBS=0V; VDS is swept from 0V to -18V at a step of -0.25V while VGS is biased at -0.9V, -1.7V, -2.5V and -3.3V respectively.

Model-silicon verification

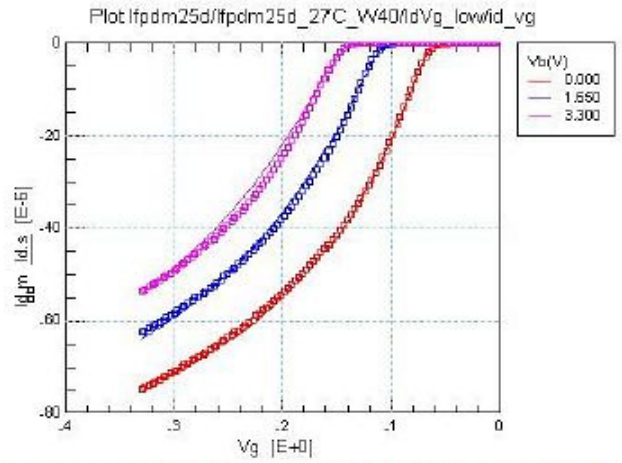

Figure 1 LFPDM25D comparison of measured and simulated id-vg curves at 27C (W=40um)

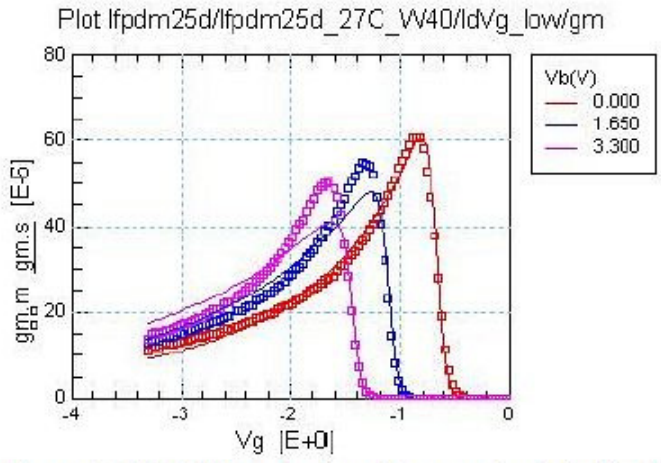

Figure 2 LFPDM25D comparison of measured and simulated gm-vg curves at 27C (W=40um)

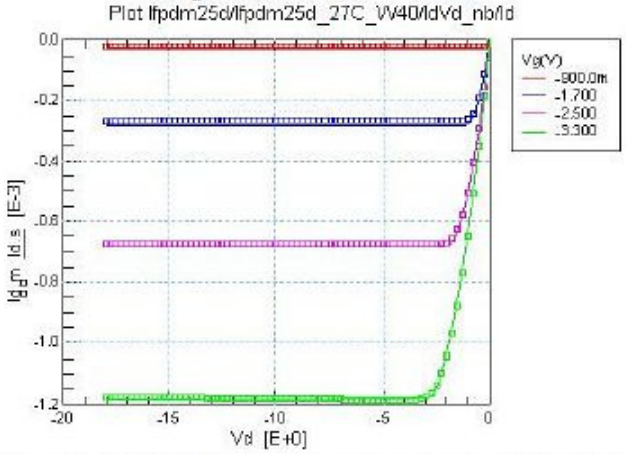

Figure 3 LFPDM25D comparison of measured and simulated id-vd curves at 27C (W=40um)

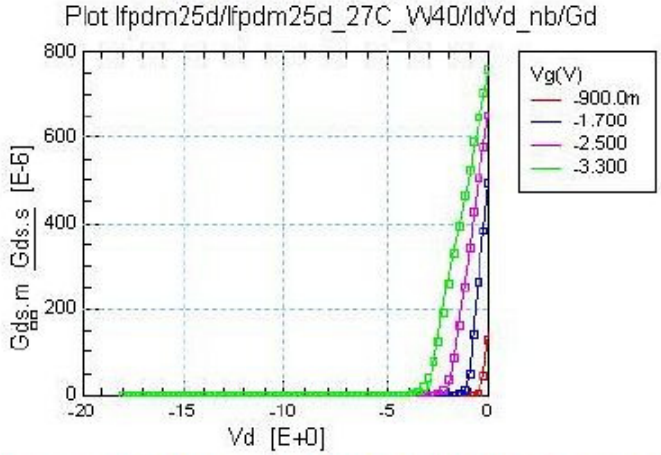

Figure 4 LFPDM25D comparison of measured and simulated gd-vd curves at 27C (W=40um)

Bench test results

Parameters		TRD Targets		Simulation				
	Lower	Mean	Upper	typ	awcp(awc0)	awcp offset	awcs(awc1)	awcs offset
Vt_gm	-0.492	-0.615	-0.738	-0.614347	-0.492101	-19.90%	-0.73798	20.12%
Idsat_3.3_18	-9.28E-04	-1.16E-03	-1.39E-03	-1.1624E-03	-1.3935E-03	19.88%	-9.2783E-04	-20.18%
Ron_0.5_3.3	1160	1450	1740	1447.9	1162.63	-19.70%	1742.3	20.33%
Beta_lin	N/A	N/A	N/A	15.1714	16.9395	11.65%	13.7237	-9.54%

Table LFPDM25D bench test results

Thick-gate DMOS devices:

LFNDM25T

Measurement information

Measurement condition of *id-vg*: VDS=0.1V; VGS is swept from 0V to 12V at a step of 0.12V while VBS is biased at 0V, -1.65V and -3.3V respectively.
Measurement condition of *id-vd*: VBS=0V; VDS is swept from 0V to 18V at a step of 0.25V while VGS is biased at 3V, 6V, 9V and 12V respectively.

Model-silicon verification

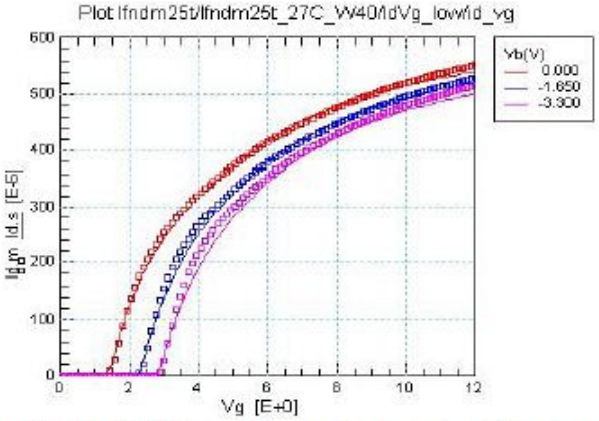

Figure 5 LFNDM25T comparison of measured and simulated id-vg curves at 27C (W=40um)

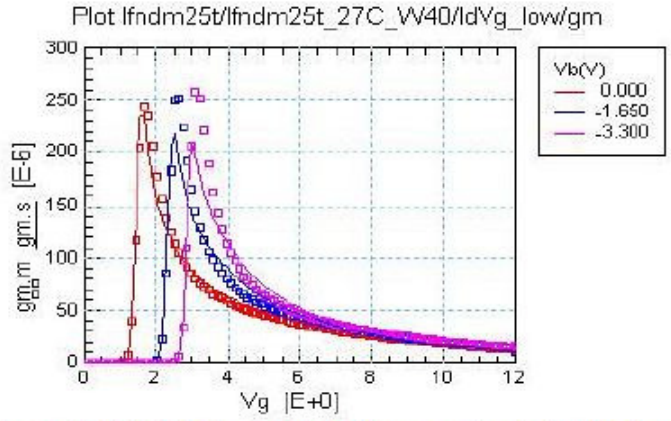

Figure 6 LFNDM25T comparison of measured and simulated gm-vg curves at 27C (W=40um)

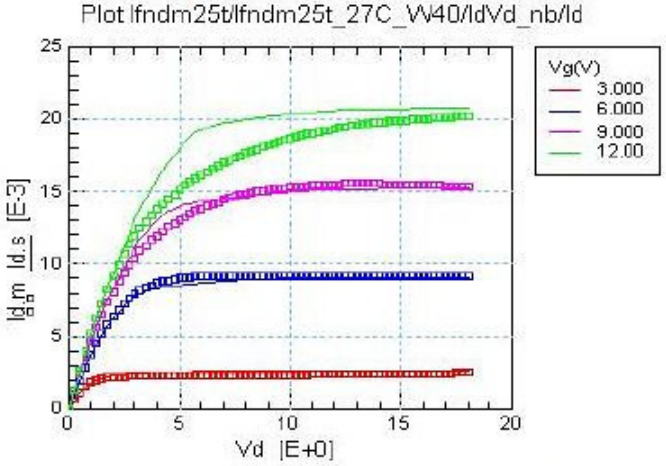

Figure 7 LFNDM25T comparison of measured and simulated id-vd curves at 27C (W=40um)

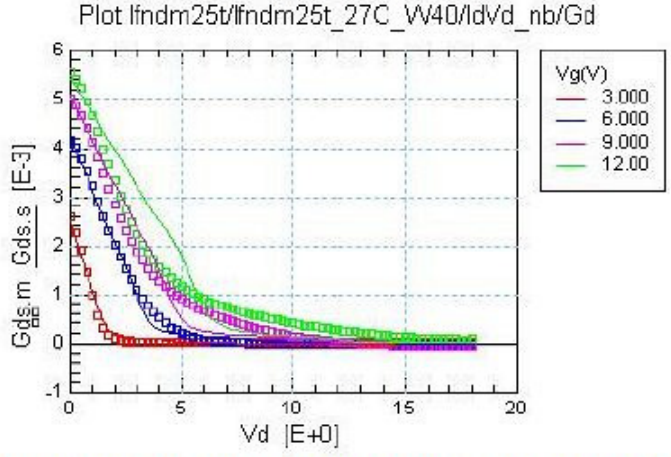

Figure 8 LFNDM25T comparison of measured and simulated gd-vd curves at 27C (W=40um)

Bench test results

Parameters		TRD Targets		Simulation				
	Lower	Mean	Upper	typ	awcp(awc0)	awcp offset	awcs(awc1)	awcs offset
Vt_gm	1.088	1.36	1.632	1.36203	1.0869	-20.20%	1.63204	19.82%
Idsat_6_18	7.48E-03	9.35E-03	1.12E-02	9.3464E-03	1.1151E-02	19.30%	7.4878E-03	-19.89%
Ron_0.5_12	148	185	222	184.016	148.051	-19.54%	222.727	21.04%
Beta_lin	N/A	N/A	N/A	67.2038	74.0129	10.13%	60.9934	-9.24%

Table LFNDM25T bench test results

LFPDM25T

Measurement information

Measurement condition of *id-vg*: VDS=-0.1V; VGS is swept from 0V to -12V at a step of -0.12V while VBS is biased at 0V, 1.65V and 3.3V respectively.
Measurement condition of *id-vd*: VBS=0V; VDS is swept from 0V to -18V at a step of -0.25V while VGS is biased at -3V, -6V, -9V and -12V respectively.

Model-silicon verification

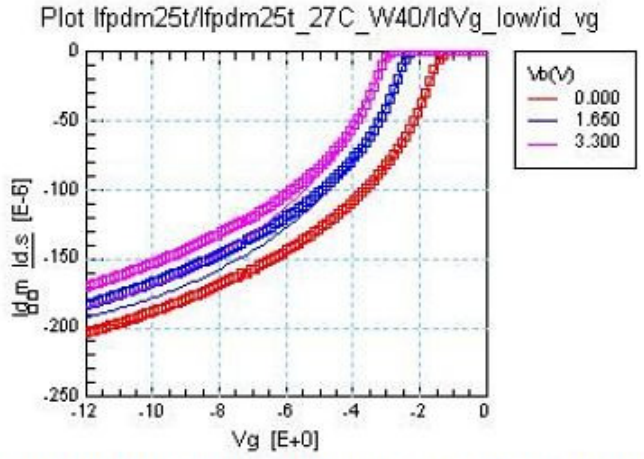

Figure 9 LFPDM25T comparison of measured and simulated id-vg curves at 27C (W=40um)

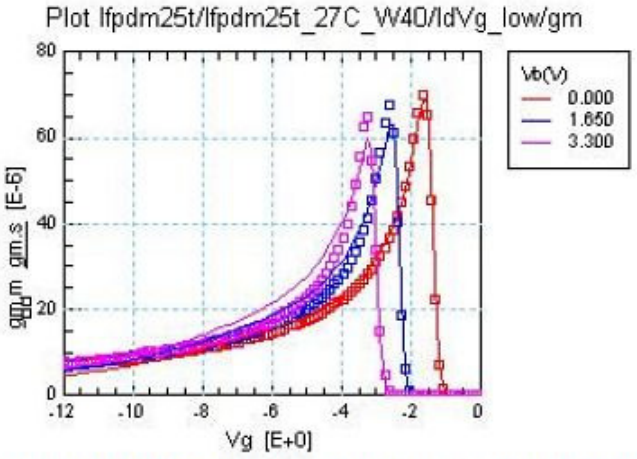

Figure 10 LFPDM25T comparison of measured and simulated gm-vg curves at 27C (W=40um)

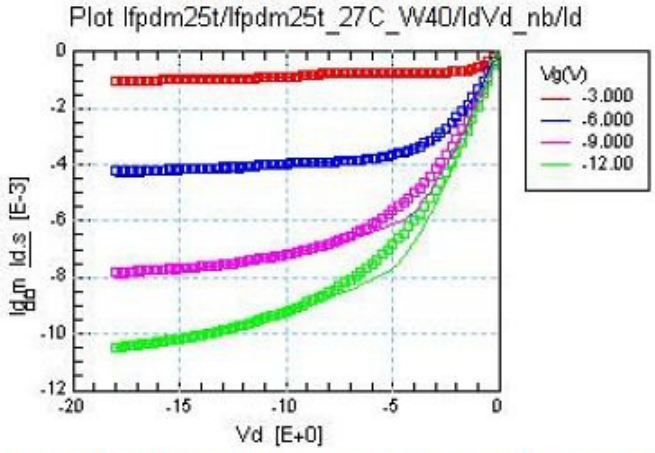

Figure 11 LFPDM25T comparison of measured and simulated id-vd curves at 27C (W=40um)

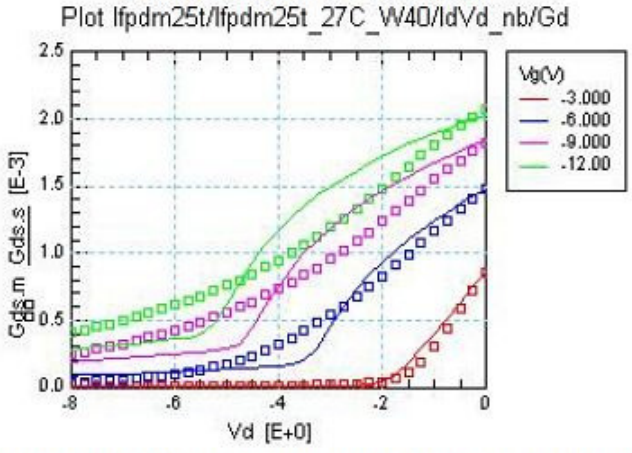

Figure 12 LFPDM25T comparison of measured and simulated gd-vd curves at 27C (W=40um)

Bench test results

Parameters	Temp	TRD Targets	Error (typ)	Simulation				
				typ	awcp(awc0)	awcp offset	awcs(awc1)	awcs offset
Vt_gm	-55	N/A	N/A	-1.4696	-1.2932	-12.00%	-1.6553	12.64%
	27	-1.33	-0.30%	-1.3261	-1.1429	-13.81%	-1.5038	13.41%
	85	N/A	N/A	-1.2181	-1.0408	-14.56%	-1.4032	15.19%
	130	N/A	N/A	-1.1403	-0.9547	-16.28%	-1.3150	15.32%
	200	N/A	N/A	-1.0088	-0.8330	-17.43%	-1.1962	18.57%
Idsat_6_18	-55	N/A	N/A	-5.6356E-03	-7.4945E-03	32.99%	-3.6962E-03	-34.41%
	27	-4.34E-03	0.18%	-4.3477E-03	-5.8856E-03	35.37%	-2.6776E-03	-38.41%
	85	N/A	N/A	-3.7142E-03	-5.0667E-03	36.41%	-2.1803E-03	-41.30%
	130	N/A	N/A	-3.3196E-03	-4.5528E-03	37.15%	-1.8539E-03	-44.15%
	200	N/A	N/A	-2.8123E-03	-3.9028E-03	38.78%	-1.3253E-03	-52.87%
Ron_12_0.5	-55	N/A	N/A	368.91	281.83	-23.60%	477.56	29.45%
	27	500	0.13%	500.67	332.43	-33.60%	691.52	38.12%
	85	N/A	N/A	601.24	373.14	-37.94%	853.51	41.96%
	130	N/A	N/A	680.54	405.07	-40.48%	981.97	44.29%
	200	N/A	N/A	802.32	452.18	-43.64%	1184.39	47.62%

Table LFPDM25T bench test results

LFNDM25DT

Measurement information

Measurement condition of *id-vg*: VDS=0.1V; VGS is swept from 0V to 12V at a step of 0.12V while VBS is biased at 0V, -1.65V and -3.3V respectively.
Measurement condition of *id-vd*: VBS=0V; VDS is swept from 0V to 18V at a step of 0.25V while VGS is biased at 3V, 6V, 9V and 12V respectively.

Model-silicon verification

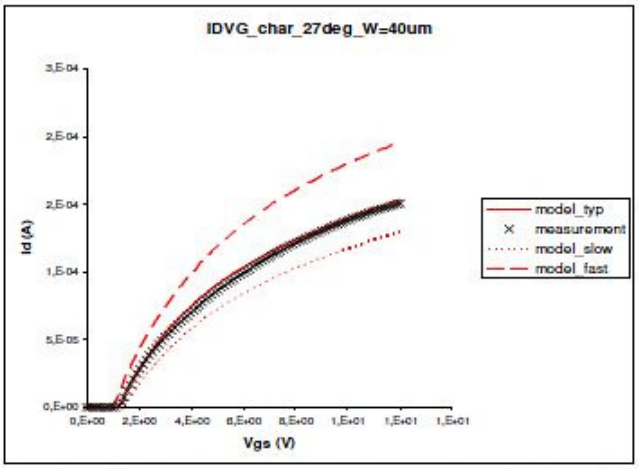

Figure 13 LFNDM25DT comparison of measured and simulated id-vg curves at 27C with corners (W=40um)

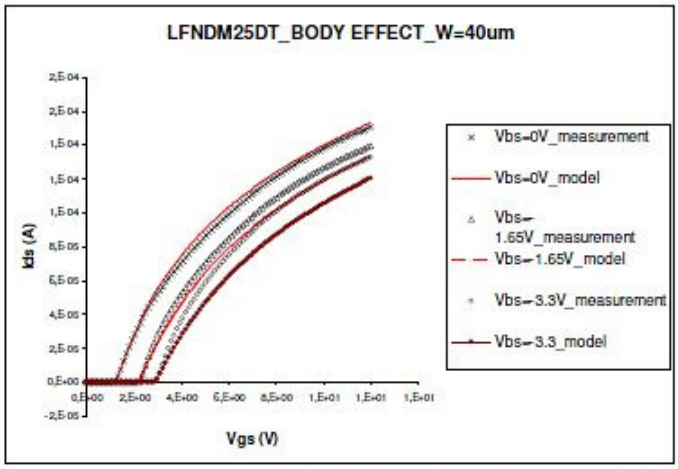

Figure 14 LFNDM25DT comparison of measured and simulated id-vg curves at 27C (W=40um), BODY EFFECT.

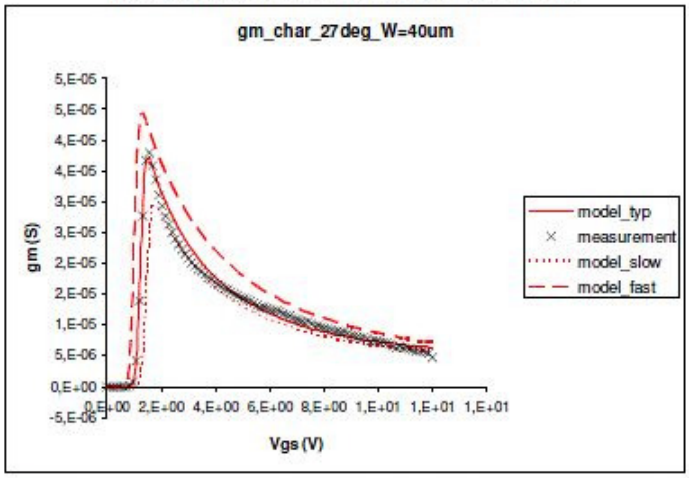

Figure 15 LFNDM25DT comparison of measured and simulated gm-vg curves at 27C (W=40um) with corners

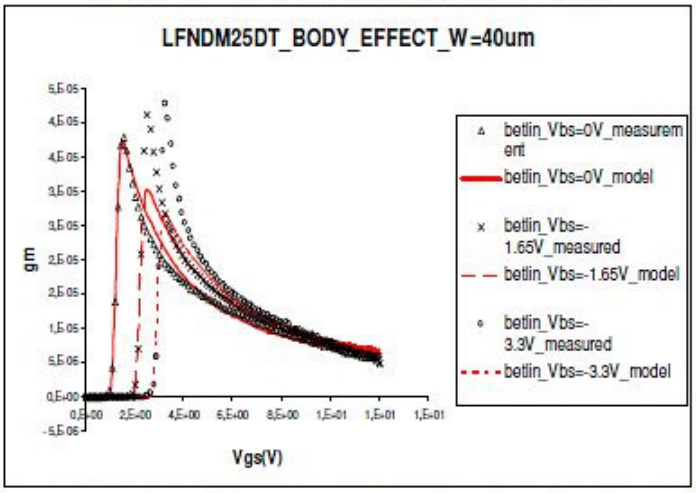

Figure 16 LFNDM25DT comparison of measured and simulated gm-vg curves at 27C (W=40um), BODY EFFECT.

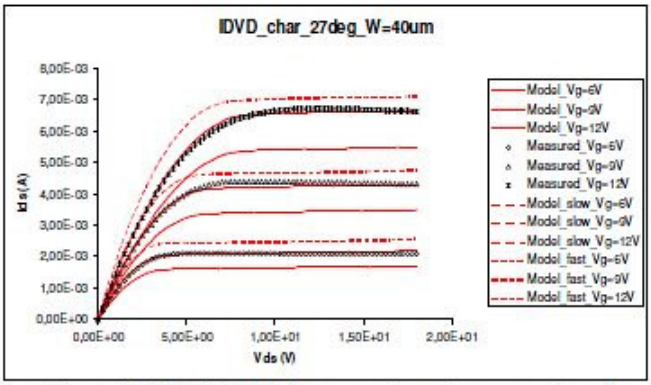

Figure 17 LFNDM25DT comparison of measured and simulated id-vd curves at 27C (W=40um) with corners

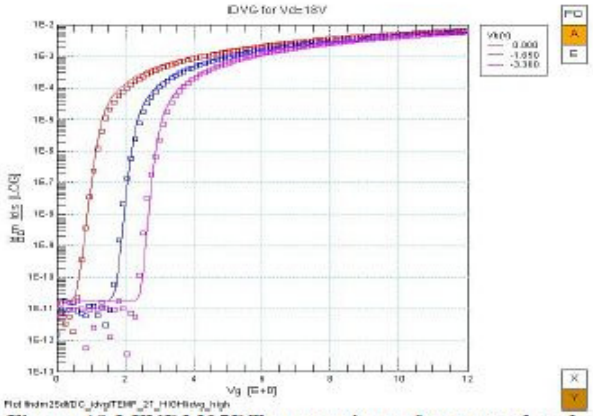

Figure 18 LFNDM25DT comparison of measured and simulated id-vg curves at 27C (W=40um), sub-threshold BODY EFFECT

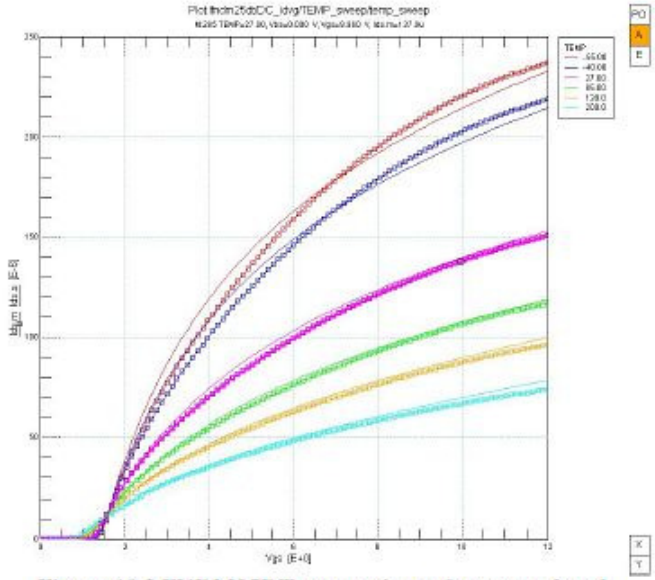

Figure 19 LFNDM25DT comparison of measured and simulated id-vg curves for temperature sweep (W=40um)

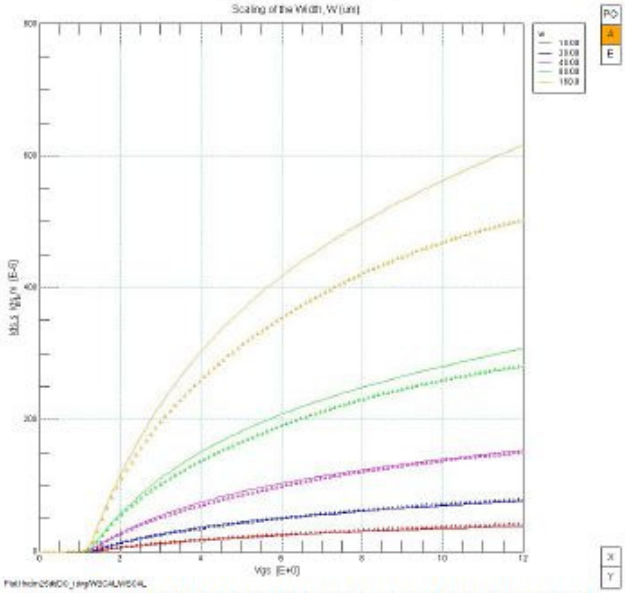

Figure 20 LFNDM25DT comparison of measured and simulated id-vg curves at 27C for different scaling.

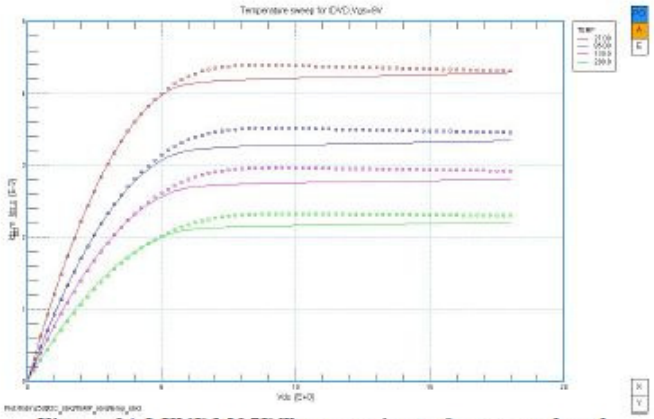

Figure 21 LFNDM25DT comparison of measured and simulated id-vd curves for temperature sweep at Vgs=9V (W=40um)

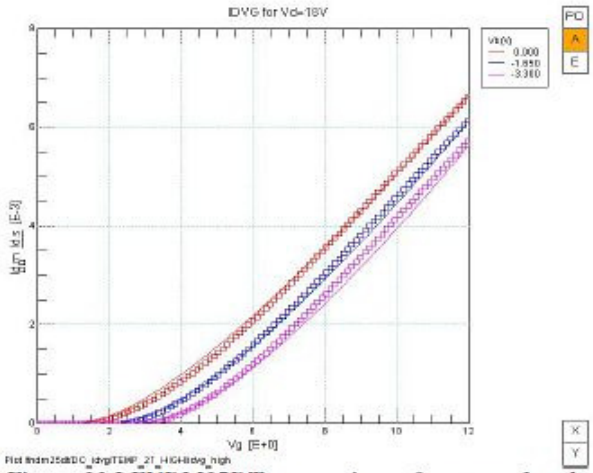

Figure 22 LFNDM25DT comparison of measured and simulated id-vg curves at 27C for Vd=18V (W=40um)

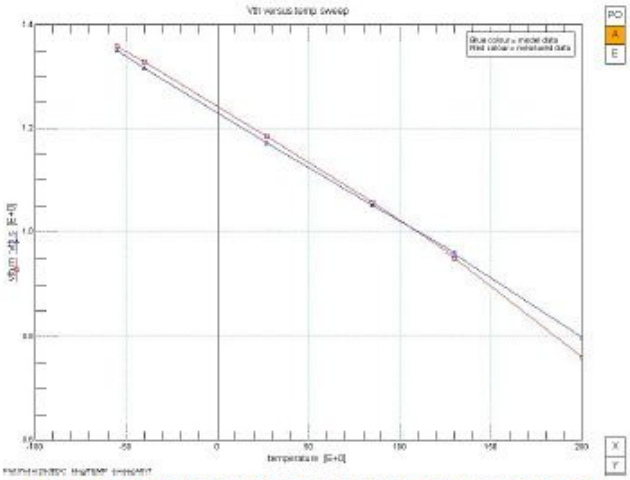

Figure 23 LFNDM25DT comparison of measured and simulated vth for different temperatures (W=40um)

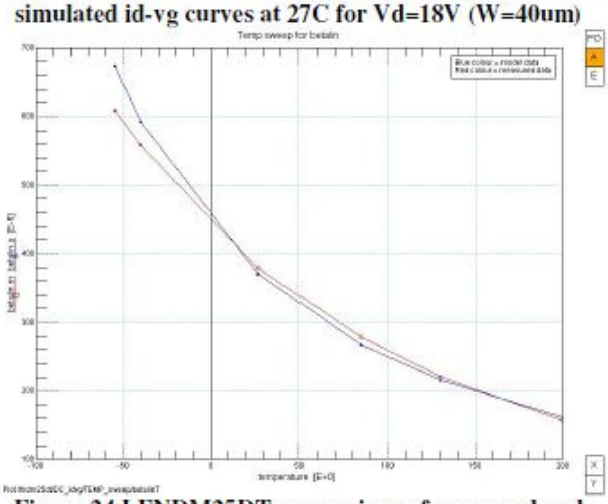

Figure 24 LFNDM25DT comparison of measured and simulated betalin for different temperatures (W=40um)

Bench test results

Parameters	TRD Targets			Simulation					
-	Lower	Mean	Upper	typ	typ offset	awcp(awc0)	awcp offset	awcs(awc1)	awcs offset
Vt_gm	0.936	1.17	1.404	1.17	0%	0.936	0%	1.405	0.1%
Idsat_6_12	1.7E-03	2.12E-03	2.54E-03	2.18E-3	2,8%	2.54E-3	0.2%	1.69E-3	0.04%
Ron_12_0.5	528	660	792	668	1,2%	529	0,2%	794	0.3%

Table LFNDM25DT bench test results

LFPDM25DT

Measurement information

Measurement condition of *id-vg*: VDS=-0.1V; VGS is swept from 0V to -12V at a step of -0.12V while VBS is biased at 0V, 1.65V and 3.3V respectively.
Measurement condition of *id-vd*: VBS=0V; VDS is swept from 0V to -18V at a step of -0.25V while VGS is biased at -3V, -6V, -9V and -12V respectively.

Model-silicon verification

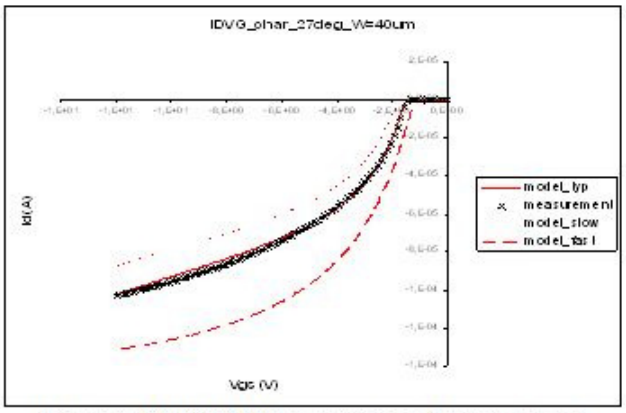

Figure 25 LFPDM25DT comparison of measured and simulated id-vg curves at 27C with corners (W=40um)

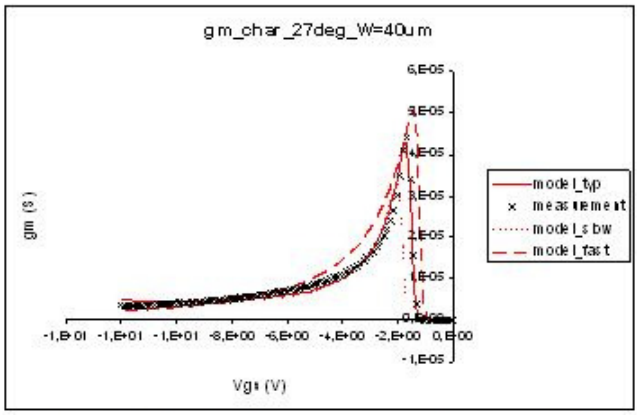

Figure 26 LFPDM25DT comparison of measured and simulated gm-vg curves at 27C with corners (W=40um)

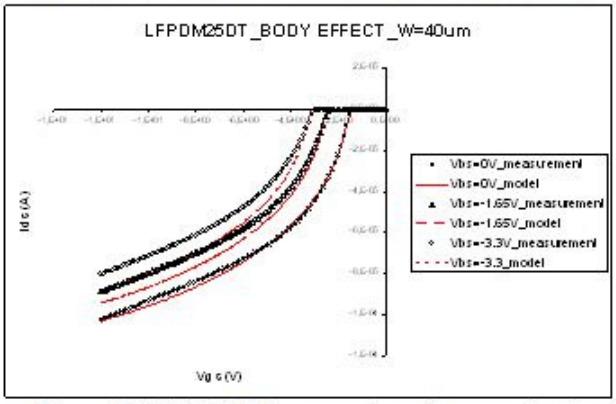

Figure 27 LFPDM25DT comparison of measured and simulated id-vg curves at 27C (W=40um), BODY EFFECT

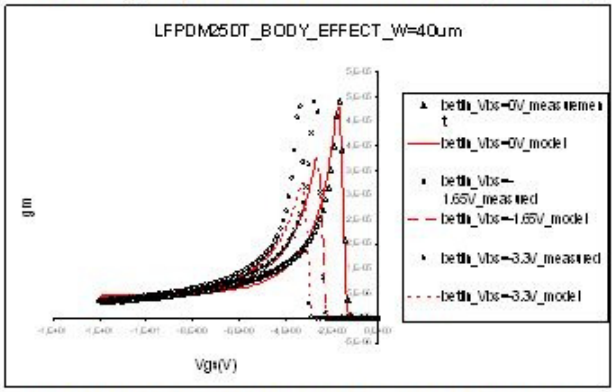

Figure 28 LFPDM25DT comparison of measured and simulated gm-vg curves at 27C (W=40um), BODY EFFECT

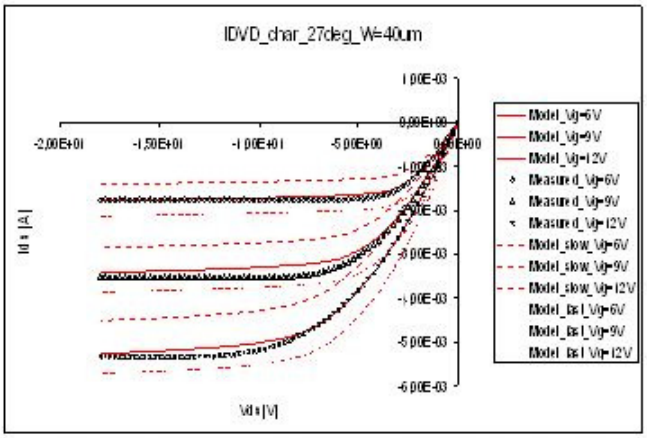

Figure 29 LFPDM25DT comparison of measured and simulated id-vd curves at 27C with corners (W=40um)

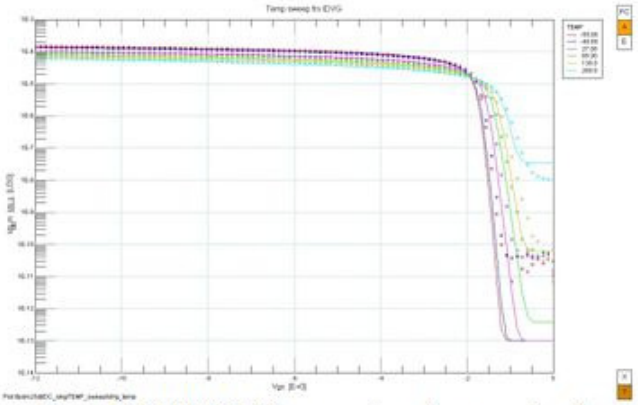

Figure 30 LFPDM25DT comparison of measured and simulated id-vg curves in sub-threshold, temperature sweep (W=40um)

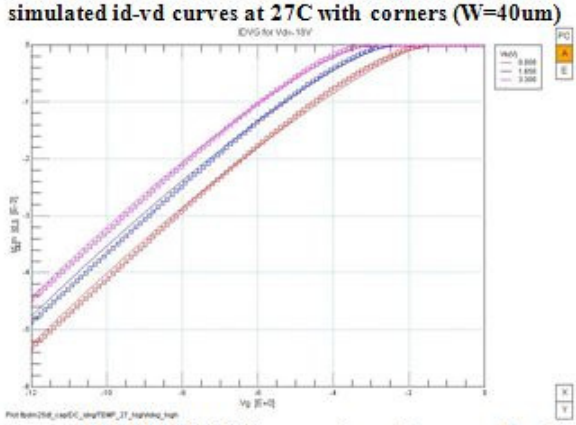

Figure 31 LFPDM25DT comparison of measured and simulated id-vg curves at 27C, Vd=18V, BODY EFFECT (W=40um)

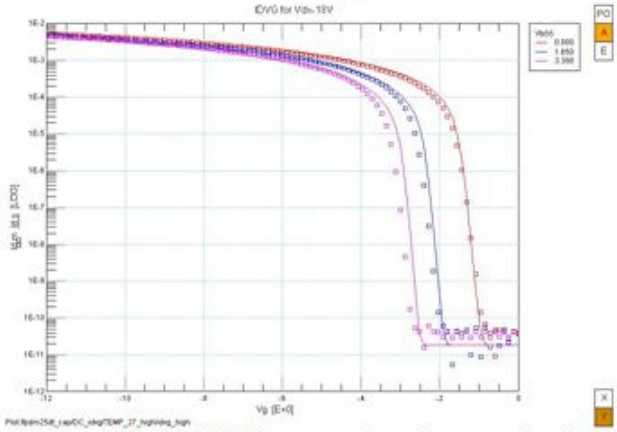

Figure 32 LFPDM25DT comparison of measured and simulated id-vg curves at 27C in sub-threshold, BODY EFFECT (W=40um)

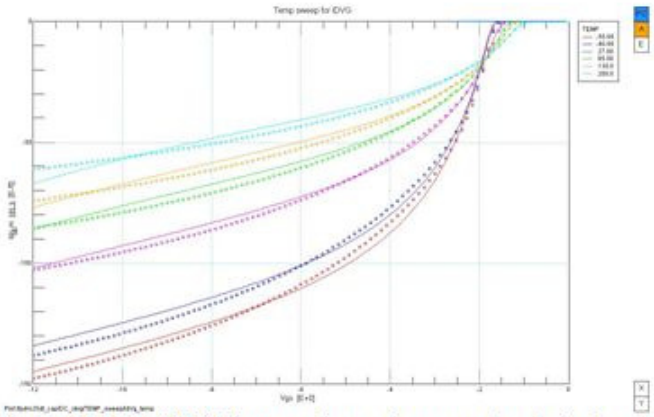

Figure 33 LFPDM25DT comparison of measured and simulated id-vg curves, temperature sweep (W=40um)

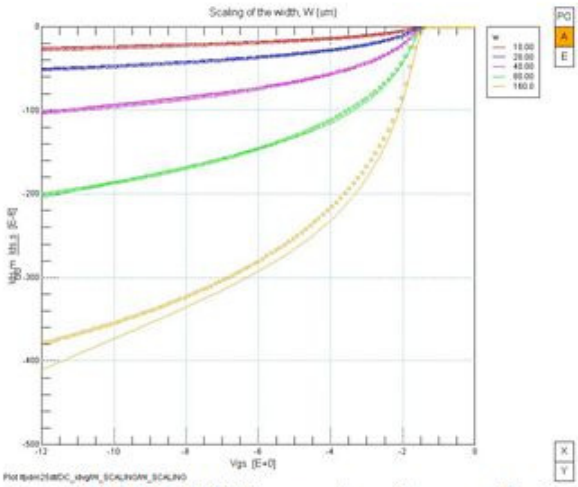

Figure 34 LFPDM25DT comparison of measured and simulated id-vg curves at 27C, scaling

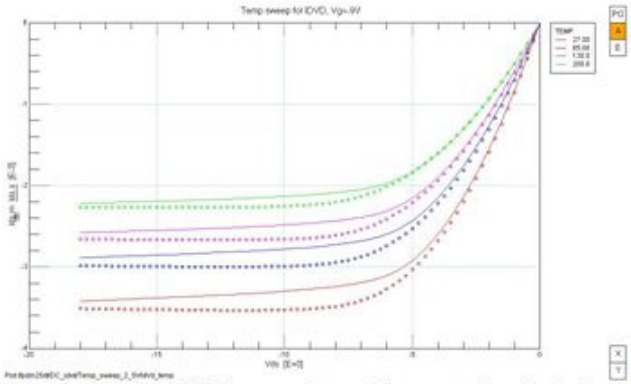

Figure 35 LFPDM25DT comparison of measured and simulated id-vd curves Vgs=9V, temperature sweep (W=40um)

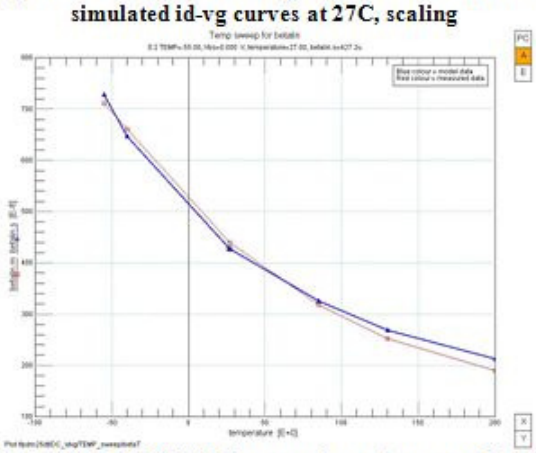

Figure 36 LFPDM25DT comparison of measured and simulated betalin at different temperatures (W=40um)

Bench test results

Parameters	TRD Targets			Simulation					
-	Lower	Mean	Upper	typ	typ offset	awcp(awc0)	awcp offset	awcs(awc1)	awcs offset
Vt_gm	-1.74	-1.45	-1.16	-1.45	0.1%	-1.163	0.3%	-1.746	0.3%
Idsat_6_12	-2.12e-3	-1.77e-3	-1.42e-3	-1.794e-3	1.4%	-2.13e-3	0.3%	-1.42e-3	0%
Ron_12_0.5	784	980	1176	999	1.9%	782	0.2%	1175	0.1%

Table LFPDM25DT bench test results

LFNDM20NT

Measurement information

Measurement condition of *id-vg*: VDS=0.1V, VBS=0V, VGS is swept from 0V to 12V at a step of 0.1V.
Measurement condition of *id-vd*: VBS=0V; VDS is swept from 0V to 12V at a step of 0.25V while VGS is biased at 3V, 6V, 9V and 12V respectively.

Model-silicon verification

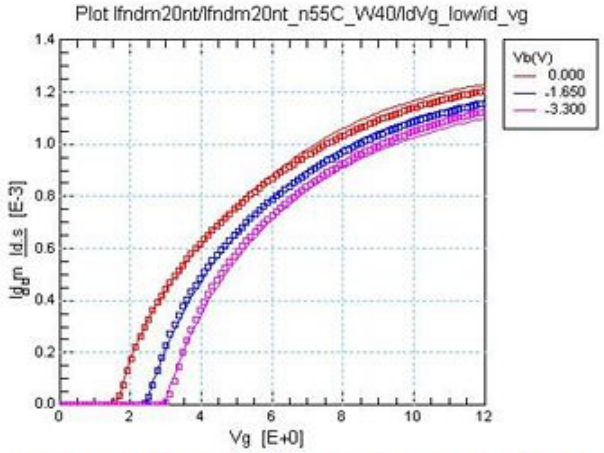

Figure 37 LFNDM20NT: Comparison of measured and simulated id-vg curves at -55C (W=40um)

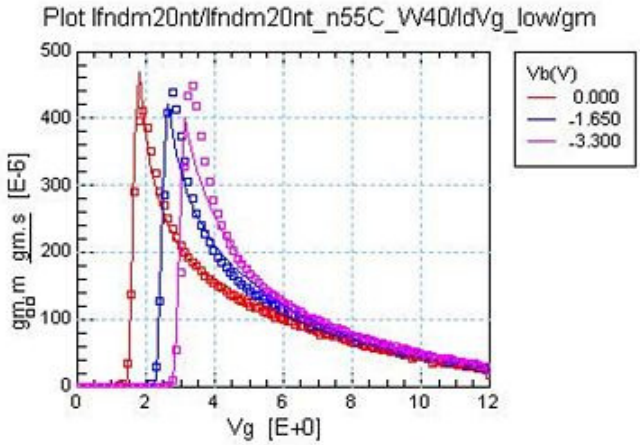

Figure 38 LFNDM20NT:Comparison of measured and simulated gm-vg curves at -55C (W=40um)

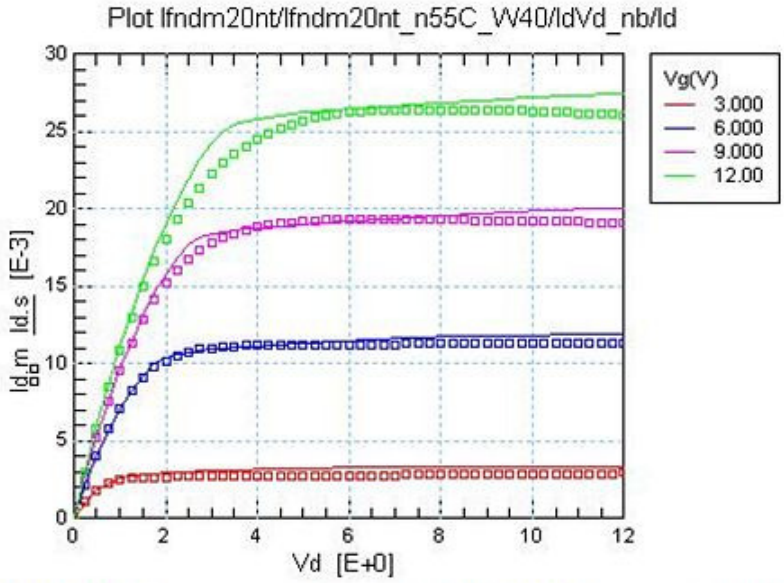

Figure 39 LFNDM20NT:Comparison of measured and simulated id-vd curves at -55C (W=40um)

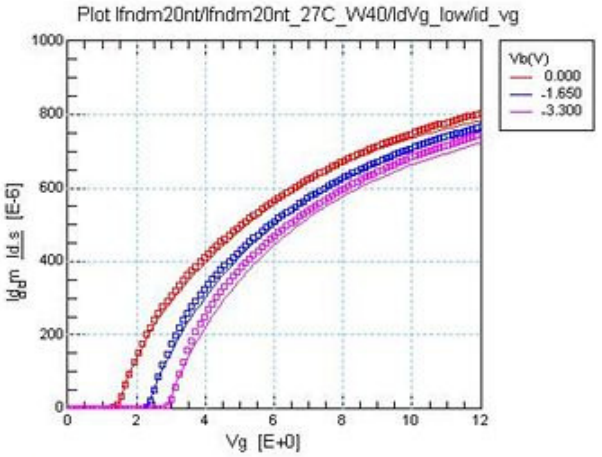

Figure 40 LFNDM20NT:Comparison of measured and simulated id-vg curves at 27C (W=40um)

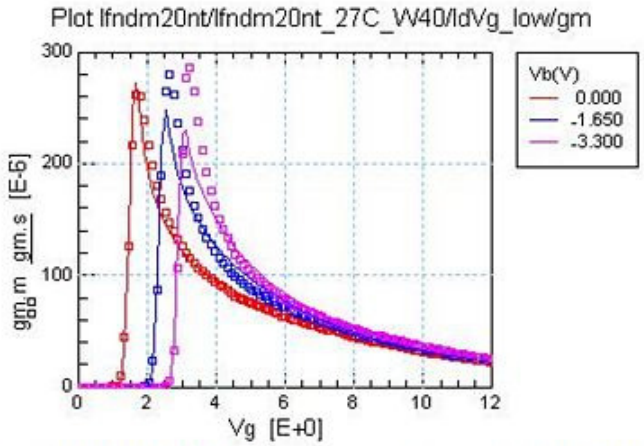

Figure 41 LFNDM20NT:Comparison of measured and simulated gm-vg curves at 27C (W=40um)

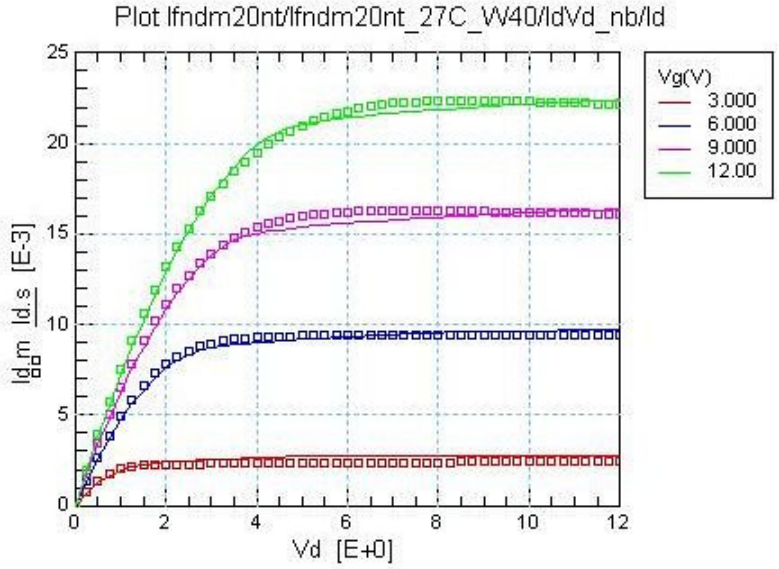

Figure 42 LFNDM20NT:Comparison of measured and simulated id-vd curves at 27C (W=40um)

Bench test results

Parameters		TRD Targets		Simulation				
	Lower	Mean	Upper	typ	awcp(awc0)	awcp offset	awcs(awc1)	awcs offset
Vt_gm	1.104	1.38	1.656	1.37705	1.104	-19.83%	1.65471	20.16%
Idsat_6_12	7.56E-03	9.45E-03	1.13E-02	9.4665E-03	1.1368E-02	20.08%	7.5526E-03	-20.22%
Ron_12_0.5	100	125	150	125.639	100.896	-19.69%	150.656	19.91%
Beta_lin	N/A	N/A	N/A	73.3794	80.1706	9.25%	65.8799	-10.22%

Table Bench test results for LFNDM20NT (w=40um)

LFPDM20NT

Measurement information

Measurement condition of id-vg: VDS=-0.1V, VBS=0V, VGS is swept from 0V to -12V at a step of -0.1V.
Measurement condition of *id-vd*: VBS=0V; VDS is swept from 0V to -12V at a step of -0.25V while VGS is biased at -3V, -6 V, -9V and -12V respectively.

Model-silicon verification

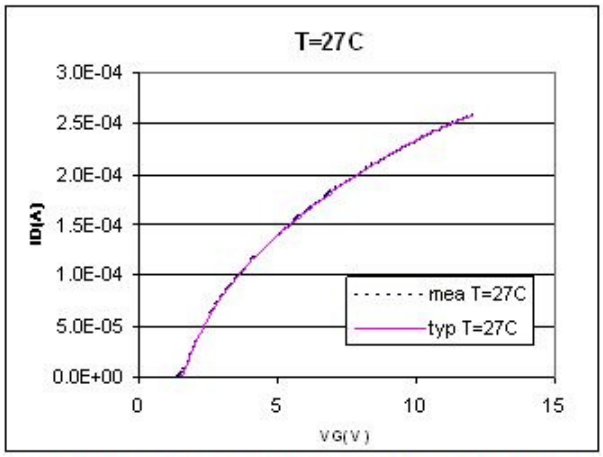

Figure 43 LFPDM20NT:Comparison of measured and simulated id-vg curves at -55C (W=40um)

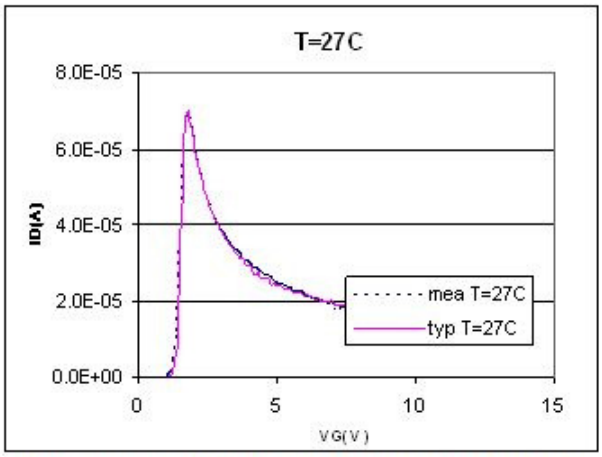

Figure 44 LFPDM20NT:Comparison of measured and simulated gm-vg curves at -55C (W=40um)

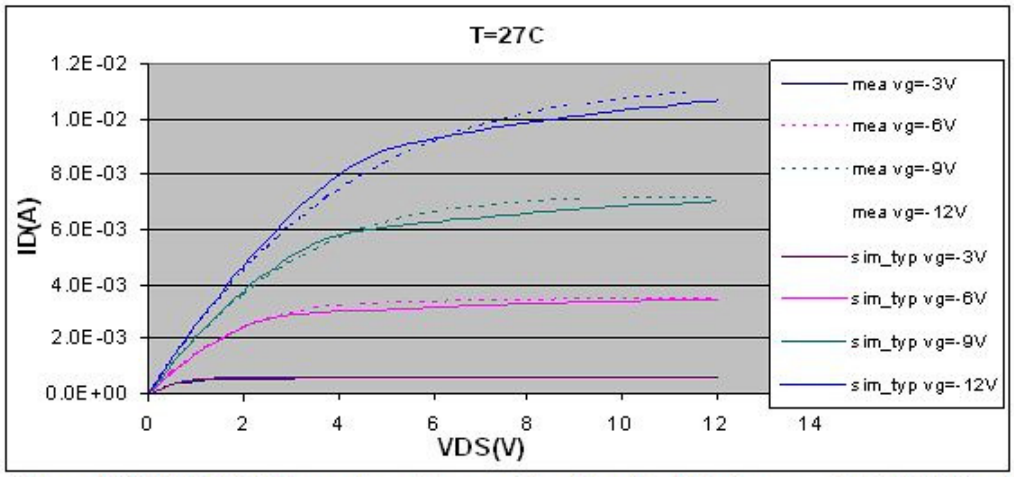

Figure 45 LFPDM20NT:Comparison of measured and simulated id-vd curves at -55C (W=40um)

Bench test results

Parameters	Temp	TRD Target	Simulation					
			typ	typ error	awcp(awc1)	awcp offset	awcs(awc0)	awcs offset
Vt_gm	-55		-1.6754		-1.4535	-13.24%	-1.9313	15.27%
	27	-1.52	-1.5232	0.21%	-1.3025	-14.49%	-1.7813	16.94%
	85		-1.4236		-1.1992	-15.77%	-1.6807	18.06%
	130		-1.3437		-1.1159	-16.95%	-1.5965	18.81%
	200		-1.2170		-0.9914	-18.54%	-1.4770	21.36%
Idsat_6_12	-55		4.6239E-03		6.2453E-03	35.06%	2.9857E-03	-35.43%
	27	3.66E-03	3.6569E-03	-0.08%	5.2657E-03	43.99%	2.1685E-03	-40.70%
	85		3.1808E-03		4.7198E-03	48.38%	1.8069E-03	-43.19%
	130		2.8905E-03		4.3636E-03	50.97%	1.5989E-03	-44.68%
	200		2.5352E-03		3.9010E-03	53.88%	1.3567E-03	-46.48%
Ron_12_0.5	-55		277.85		233.02	-16.13%	343.86	23.76%
	27	395	395.74	0.19%	256.32	-35.23%	570.98	44.28%
	85		477.67		270.54	-43.36%	731.95	53.23%
	130		538.17		278.61	-48.23%	853.89	58.67%
	200		624.19		283.97	-54.50%	1034.82	65.79%

Table Bench test results for LFPDM20NT (w=40um)

LFNDM20DNT

Measurement information

Measurement condition of *id-vg*: VDS=0.1V, VBS=0V, VGS is swept from 0V to 12V at a step of 0.1V.
Measurement condition of *id-vd*: VBS=0V; VDS is swept from 0V to 12V at a step of 0.25V while VGS is biased at 3V, 6V, 9V and 12V respectively.

Model-silicon verification

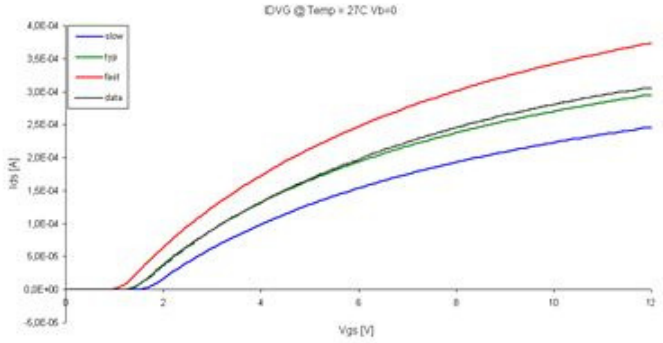

Figure 46 LFNDM20DNT comparison of measured and simulated IDVG @ Vd=0.1, 27deg, Vb=0, w=40, over corners.

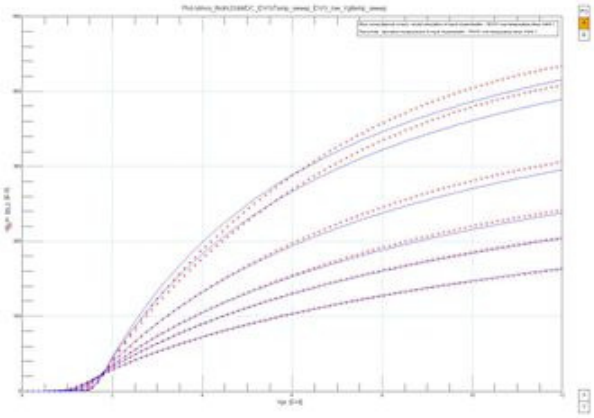

Figure 47 LFNDM20DNT comparison of measured and simulated IDVG @ low Vd=0.1, w=40, over temperature range = { -55 ; -40 ; 27 ; 85 ; 130 ; 200 } °C.

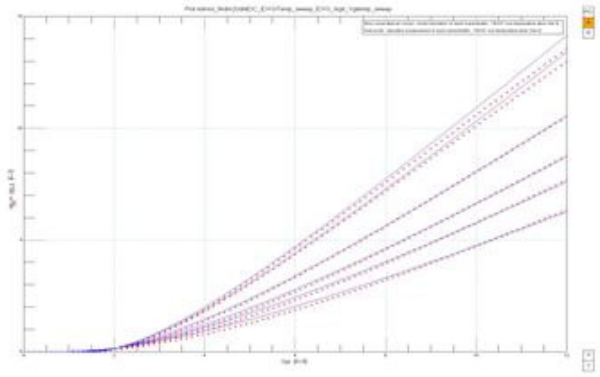

Figure 48 LFNDM20DNT comparison of measured and simulated IDVG @ high Vd=12, w=40, over temperature range = { -55 ; -40 ; 27 ; 85 ; 130 ; 200 } °C.

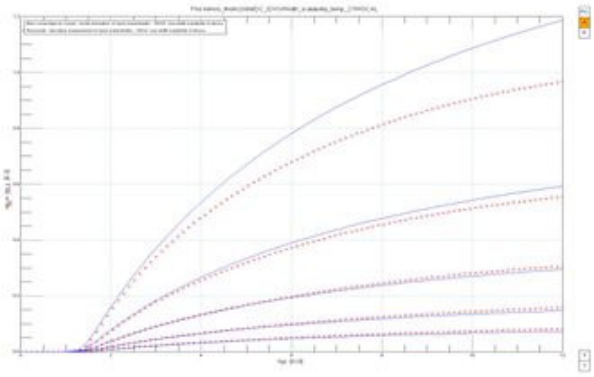

Figure 49 LFNDM20DNT comparison of measured and simulated IDVG @ Vd=0.1, over width scalability = { 5 ; 10 ; 20 ; 40 ; 80 ; 160 } um.

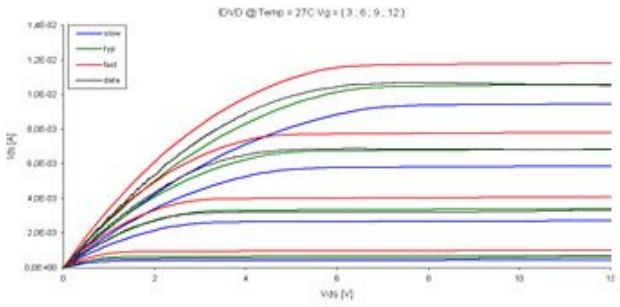

Figure 50 LFNDM20DNT comparison of measured and simulated IDVD @ 27deg, Vg = { 3 ; 6 ; 9 ; 12 } over corners , w=40, Vb=0.

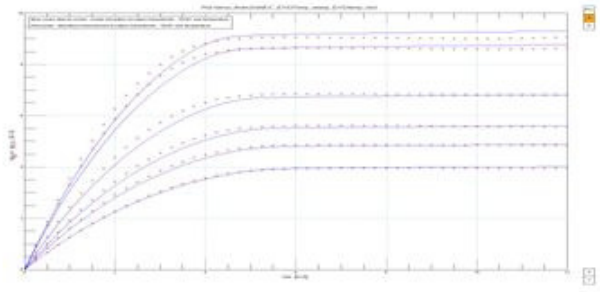

Figure 51 LFNDM20DNT comparison of measured and simulated IDVD @ Vg=9, w=40, over temperature range = { -55 ; -40 ; 27 ; 85 ; 130 ; 200 } °C.

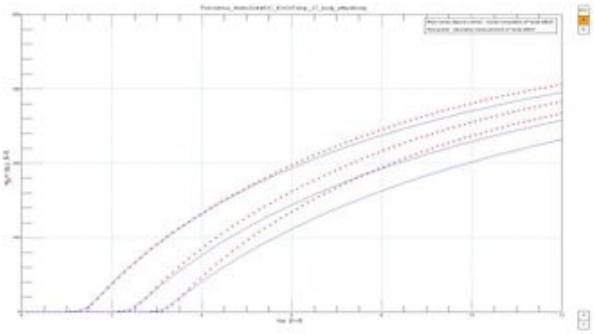

Figure 52 LFNDM20DNT comparison of measured and simulated body effect: IDVG @ Vd=0.1, w=40, Vb= { 0 ; -1.65 ; -3.3 } when 27deg.

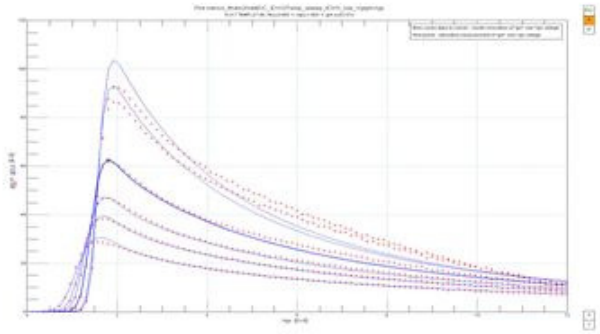

Figure 53 LFNDM20DNT comparison of measured and simulated gm-vg @ Vd=0.1, Vb=0, w=40 over temperature range = { -55 ; -40 ; 27 ; 85 ; 130 ; 200 } °C.

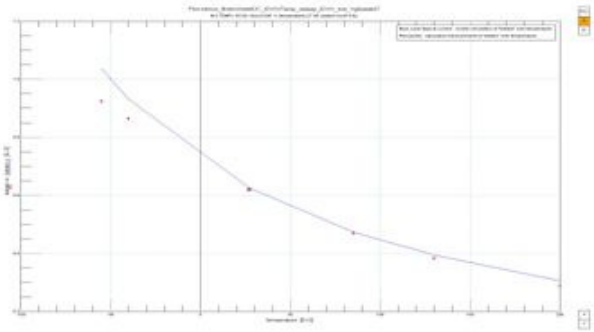

Figure 54 LFNDM20DNT comparison of measured and simulated betalinT: mathematical extrapolation of betalin over temperature range = { -55 ; -40 ; 27 ; 85 ; 130 ; 200 } °C, Vb=0.

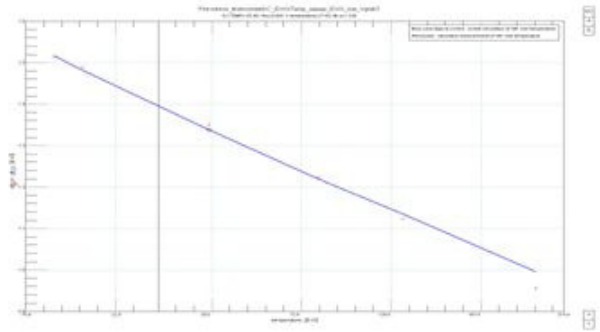

Figure 55 LFNDM20DNT comparison of measured and simulated vthT: mathematical extrapolation of vth over temperature range = { -55 ; -40 ; 27 ; 85 ; 130 ; 200 } °C, Vb=0.

Bench test results

Parameters	TRD Targets			Simulation					
-	Lower	Mean	Upper	typ	typ offset	awcp(awc0)	awcp offset	awcs(awc1)	awcs offset
Vt_gm	1.072	1.34	1.608	1.339	0,07%	1.072	0%	1.608	0%
Idsat_6_12	4.08E-03	3.4E-03	2.72E-02	3.394E-3	0,17%	4.08E-3	0%	2.705E-3	0.55%
Ron_12_0.5	280	350	420	349.89	0,03%	279	0,36%	419.1	0.21%

Table Bench test results for LFNDM20DNT (w=40um)

LFPDM20DNT

Measurement information

Measurement condition of id-vg: VDS=-0.1V, VBS=0V, VGS is swept from 0V to -12V at a step of -0.1V.
Measurement condition of *id-vd*: VBS=0V; VDS is swept from 0V to -12V at a step of -0.25V while VGS is biased at -3V, -6V, -9V and -12V respectively.

Model-silicon verification

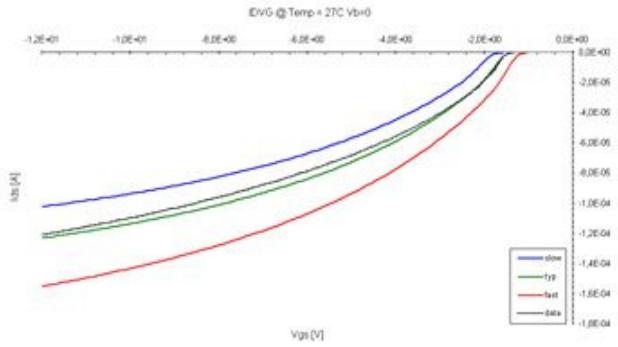

Figure 56 LFPDM20DNT comparison of measured and simulated IDVG @ Vd=-0.1, 27deg, Vb=0, w=40, over corners.

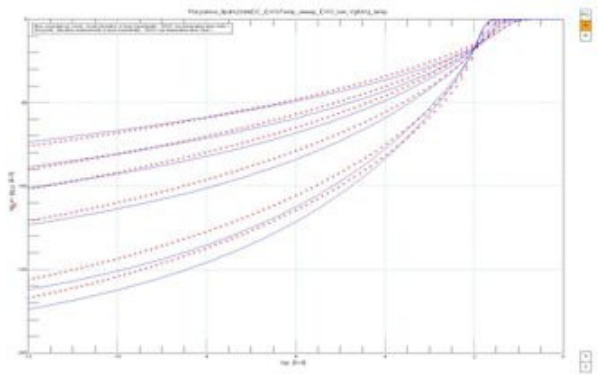

Figure 57 LFPDM20DNT comparison of measured and simulated IDVG @ low Vd=-0.1, w=40, over temperature range = { -55 ; -40 ; 27 ; 85 ; 130 ; 200 } °C.

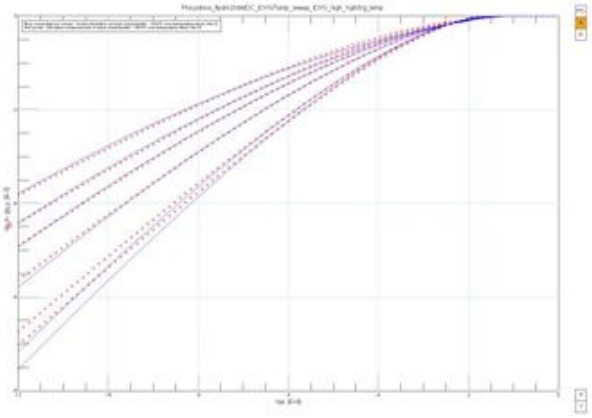

Figure 58 LFPDM20DNT comparison of measured and simulated IDVG @ high Vd=-12, w=40, over temperature range = { -55 ; -40 ; 27 ; 85 ; 130 ; 200 } °C.

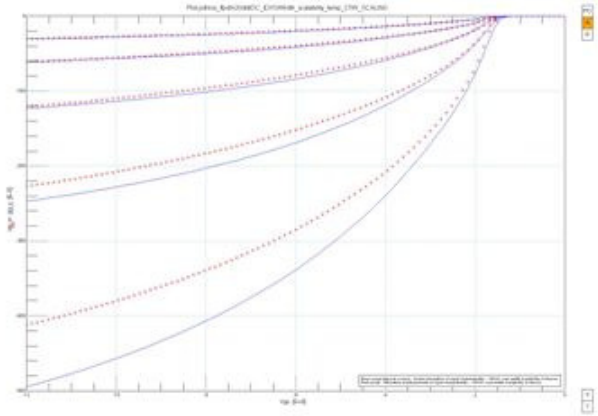

Figure 59 LFPDM20DNT comparison of measured and simulated IDVG @ Vd=-0.1, over width scalability = { 5 ; 10 ; 20 ; 40 ; 80 ; 160 } um.

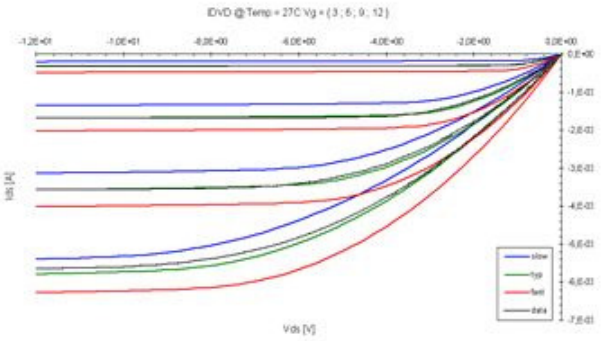

Figure 60 LFPDM20DNT comparison of measured and simulated IDVD @ 27deg, Vg = { -3 ; -6 ; -9 ; -12 } over corners , w=40, Vb=0.

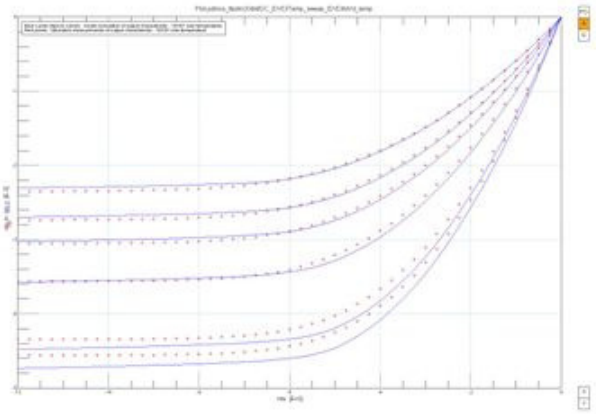

Figure 61 LFPDM20DNT comparison of measured and simulated IDVD @Vg=-9, w=40, over temperature range = { -55 ; -40 ; 27 ; 85 ; 130 ; 200 } °C.

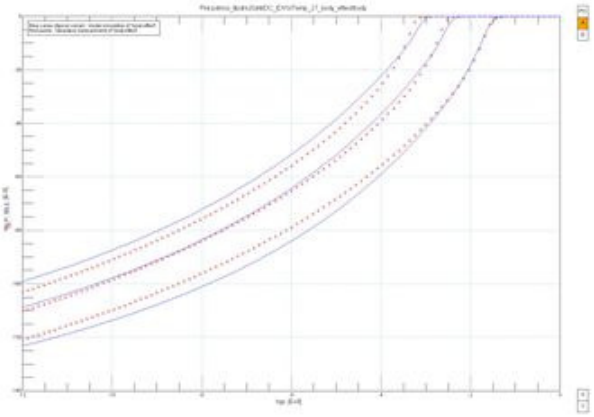

Figure 62 LFPDM20DNT comparison of measured and simulated body effect: IDVG @ Vd=-0.1, w=40, Vb= { 0 ; 1.65 ; 3.3 } when 27deg.

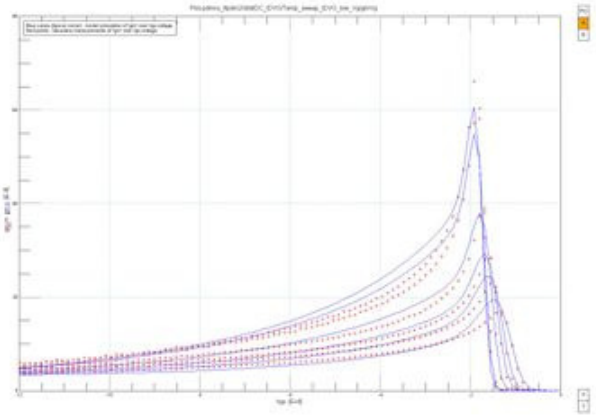

Figure 63 LFPDM20DNT comparison of measured and simulated gm-vg @ Vd=-0.1, Vb=0, w=40 over temperature range = { -55 ; -40 ; 27 ; 85 ; 130 ; 200 } °C.

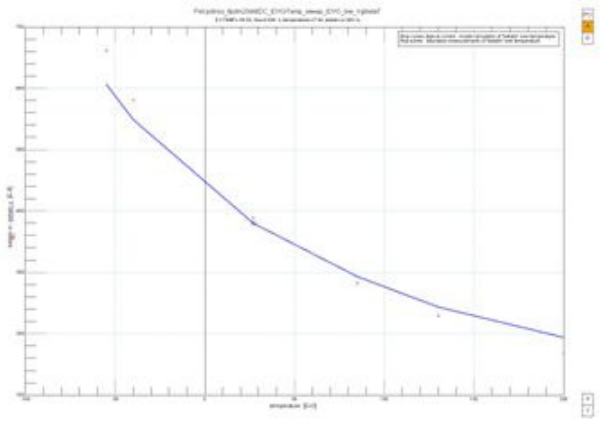

Figure 64 LFPDM20DNT comparison of measured and simulated betalinT: mathematical extrapolation of betalin over temperature range = { -55 ; -40 ; 27 ; 85 ; 130 ; 200 } °C, Vb=0.

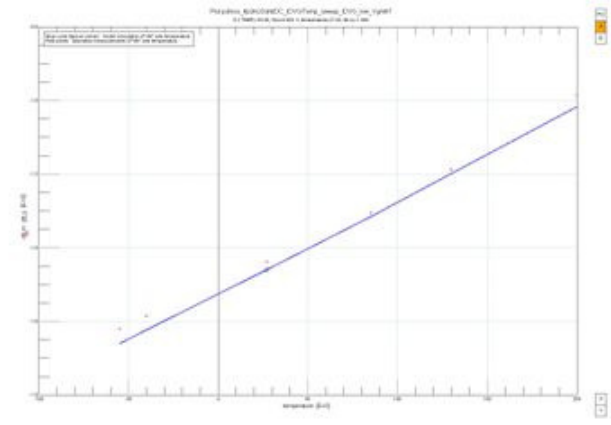

Figure 65 LFPDM20DNT comparison of measured and simulated vthT: mathematical extrapolation of vth over temperature range = { -55 ; -40 ; 27 ; 85 ; 130 ; 200 } °C, Vb=0.

Bench test results

Parameters	TRD Targets			Simulation					
-	Lower	Mean	Upper	typ	typ offset	awcp(awc0)	awcp offset	awcs(awc1)	awcs offset
Vt_gm	-1.168	-1.46	-1.752	-1.46	0%	-1.168	0%	-1.752	0%
Idsat_6_12	-2.028E-3	-1.69E-3	-1.352E-3	-1.692E-3	0.12%	-2.029	0.05%	-1.359E-3	0.51%
Ron_12_0.5	664	830	996	830.4	0.05%	664.18	0.03%	996	0%

Table Bench test results for LFPDM20DNT (w=40um).

I3T25 Electrical Design Rules

Description of Schottky:

The Schottky diode (SCHD) is a fixed size component, modelled as a 3-terminal device with anode (‘plus’), cathode (‘minus’) and deep Pwell – substrate (‘substrate’) nodes. See figure 1 below.

- The parasitic junction capacitance parameter values are from C035U diode model.
  - cj: P+/Nwell diode
  - cjc: Nepi/Psub diode
  - cje: P+/Nwell diode

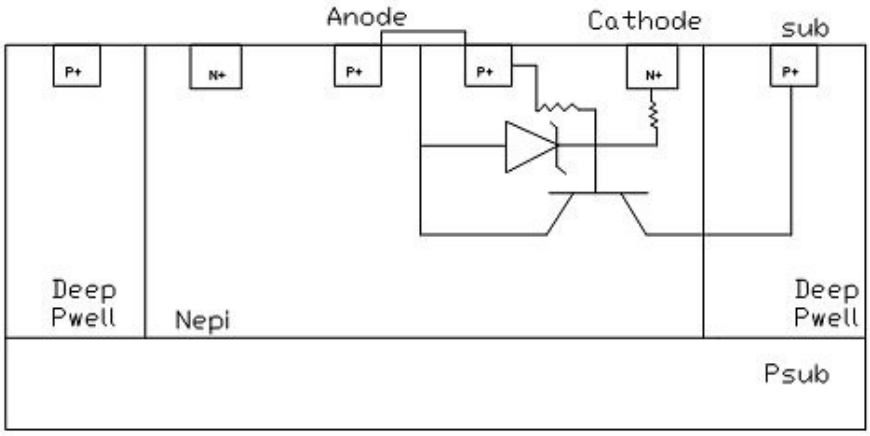

Figure 1 Cross section view of C035U schottky diode

Characteristic curves:

SCHD:

- DC Curves at 30C

  All voltages are in Volts and currents in Amperes.

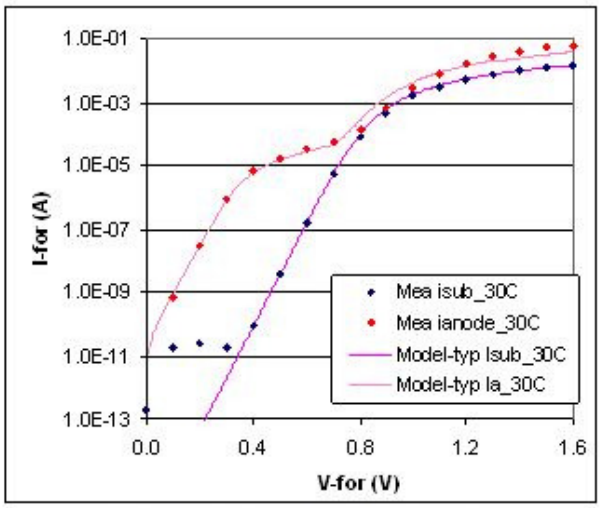

Figure 3 : Overview of forward characteristics at 30C

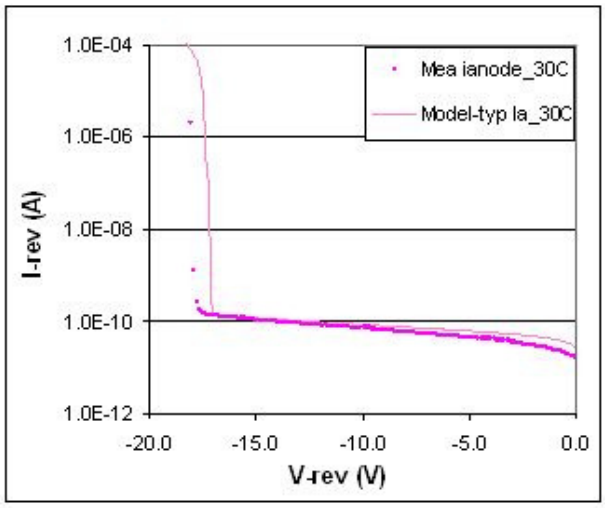

Figure 4 : Overview of reverse characteristics at 30C

Electrical data (Measurement Vs Simulation):

	Bias	30C	85C	130C	200C
Measurement	0.20	2.7804E-08	4.1431E-07	1.1916E-06	4.5252E-06
	0.6	3.2272E-05	4.6735E-05	6.1977E-05	3.7330E-04
	0.9	6.1214E-04	2.4484E-03	2.3846E-03	7.7185E-03
	-5.5	4.8890E-11	3.0979E-09	2.1744E-08	4.6918E-07
	-10.0	7.2900E-11	4.3127E-09	2.9175E-08	6.0682E-07
Simulation	0.20	2.6800E-08	3.2500E-07	1.3100E-06	9.0900E-06
	0.60	2.5500E-05	3.4700E-05	1.0800E-04	2.4500E-03
	0.90	1.4000E-03	2.3600E-03	4.6900E-03	1.1900E-02
	-5.50	6.1600E-11	1.9500E-09	2.3900E-08	1.1500E-06
	-10.00	8.2300E-11	2.4300E-09	3.0000E-08	1.4500E-06
Error	0.20	-3.61%	-21.56%	9.94%	100.88%
	0.6	-20.98%	-25.75%	74.26%	556.31%
	0.9	128.71%	-3.61%	96.68%	54.18%
	-5.5	26.00%	-37.05%	9.91%	145.11%
	-10.0	12.89%	-43.65%	2.83%	138.95%

I3T25 Electrical Design Rules

Capacitors:

Metal2 – Metal2.5 capacitor (Pcell PC_M2IMC)

This capacitor is described in DES-0005.

Metal - Metal Finger Capacitor (Pcells PC_MMCHB and PC_MMCHBXW)

The MMF is realized by means of inter-digitated minimal narrow tracks of metals and poly.
The metal bars of each level are staggered compared to the adjacent levels to increase the total capacitance by means of the fringe capacitances.
The default configuration is made with the first three metal levels and a poly comb underneath. The plates of this capacitor are swappable.
PWELL shield diffusion is available as option for better potential decoupling from the substrate.

No voltage limitations are yet set, but this capacitor should be able to withstand at least 50-60 V: reliability tests are still on going.

The coefficients V_{cl} and V_{cq} (linearity), T_{CL} (temperature dependence) and A (matching) are used in the following formulas:

LINEARITY: $C(V)=C(0)x(1+V_{cl}xV+V_{cq}xV^2)$

TEMP. DEP.: $C(T)=C(0)+T_{CL}xT$

MATCHING : $s(DC/C)=A/\ddot{O}(WxL)$

The typical extracted capacitance from silicon wafers Is:

C=+/- 0.33e-9 F/µm/finger (with standard metal thickness)

For a CPMMF_NW capacitor of $1mm^2$ (std metals):

total capacitance ~218pF + parasitic capacitance to Pwell ~47pF

The temperature coefficient is quite high: TC_CPMMF ~50 ppm/K
The options for the symbol are: number of finger and their length.

Metal – Metal Sandwich Capacitor (Pcells PC_ MMCHP and PC_MMCHPXW)

The metal sandwich capacitor is realized by the overlap of consecutives levels of metal, with the bottom plate

realized by default with poly.
The sandwich metal capacitor is called MMCHP (2-terminals) or MMCHPXW_PW (on PWELL, 3 nodes).

Electrical characteristics:

For a MMCHP PW capacitor of 1mm^2 (std metals), the total capacitance is ~250pF
The temperature coefficient is limited: TC_ MMCHP <5 ppm/K

The options for the symbol are the two sizes, W and L.
The plates of this capacitor are not swappable.

Key electrical parameters table:

Model	Parameter	Unit	Min	Typ	Max
mimc	ca	F/m^2	1.3E-3	1.5E-3	1.7E-3
	cp	F/m	0.28E-9	0.34E-9	0.40E-9
	dW	m	0.1e-6	0.1e-6	0.1e-6
	tc1_ca	ppm/°C	20	45.5	60
	tc1_cp	1/°C	4.44E-3	4.44E-3	4.44E-3
	tc2_ca	1/°C^2	0	0	0
	Tc2_cp	1/°C^2	0	0	0
	vc1	ppm/V	-100	-32.03	100
	vc2	ppm/V^2	-30	18.54	30
	Alpha1		0.643E-4	0.643E-4	1.83E-4
	Alpha2		0.810E-4	0.810E-4	2.31E-4
	Alpha3		2.96E-4	2.96E-4	8.43E-4
	Timeconstant1	Second (ΩF)	0.20E-6	0.20E-6	0.20E-6
	Timeconstant2	Second (ΩF)	2.5E-6	2.5E-6	2.5E-6
	Timeconstant3	Second (ΩF)	3.0E-6	3.0E-6	3.0E-6
mimcxw	ca	F/m^2	1.3E-3	1.5E-3	1.7E-3
	cp	F/m	0.28E-9	0.34E-9	0.40E-9
	dW	m	0.1e-6	0.1e-6	0.1e-6
	tc1_ca	ppm/°C	20	45.5	60
	tc1_cp	Ppm/°C	4.44E-3	4.44E-3	4.44E-3
	tc2_ca	ppm/°C^2	0	0	0
	Tc2_cp		0	0	0
	vc1	ppm/V	-100	-32.03	100
	vc2	ppm/V^2	-30	18.54	30
	mimcxw_tox	m	3.21E-6	2.92E-6	2.63^E-6
	mimcxw_tc1_cox	/°C	-65E-6	-65E-6	-65E-6
	mimcxw_rsh_metal	Ω/□	47.3E-3	43E-3	38.7E-3
	mimcxw_lself	H/m	2.844E-7	3.16E-7	3.476E-7
mmchp **metal1 up to metal3** **Thin metal**	Ca (with poly)	F/m^2	9.8E-5	1.4E-4	1.72E-4
	Ca (without poly)	F/m^2	7E-5	1E-4	1.3E-4
	tc1	ppm/C	-50	-50	-50
mmchb **Metal1 up to metal3** **Thin metal**	c0 (with poly)	F/m	-1.16E-10	-8.94E-11	-6.26E-11
	cf (with poly)	F/m/finger	2.31E-10	3.3E-10	4.29E-10
	c0 (without poly)	F/m	-9.15E-11	-7.044E-11	-4.93E-11
	cf (without poly)	F/m	1.82E-10	2.6E-10	3.38E-10
	tc1		-40	-40	-40

M3m1chb,	c0	F/m	-2.03E-11	-2.03E-11	-2.03E-11
	cf	F/m/finger	1.91E-10	2.73E-10	3.56E-10
m3m1chbxw	tc1	1/C	-5.44E-05	-4.00E-05	-2.56E-05
	Tc2	1/C^2	0	0	0
	vc1	1/V	-1.50E-06	-1.50E-06	-1.50E-06
	vc2	1/V^2	-5.90E-08	-5.90E-08	-5.90E-08
M3po1chb,	c0	F/m	-2.03E-12	-2.90E-12	-3.77E-12
	cf	F/m/finger	2.31E-10	3.30E-10	4.29E-10
m3po1chbxw	tc1	1/C	-2.43E-05	-3.80E-05	-5.17E-05
	Tc2	1/C^2	0	0	0
	vc1	1/V	-8.00E-06	-8.00E-06	-8.00E-06
	vc2	1/V^2	-2.00E-07	-2.00E-07	-2.00E-07
M3m1chp,	Ca	F/m^2	7.14E-05	1.02E-04	1.33E-04
	tc1	1/C	-5.00E-05	-5.00E-05	-5.00E-05
m3m1chpxw	Tc2	1/C^2	0	0	0
	vc1	1/V	-3.80E-07	-3.80E-07	-3.80E-07
	vc2	1/V^2	-4.30E-08	-4.30E-08	-4.30E-08
M3po1chp,	Ca	F/m^2	9.80E-05	1.40E-04	1.82E-04
	tc1	1/C	-5.00E-05	-5.00E-05	-5.00E-05
M3po1chpxw	Tc2	1/C^2	0	0	0
	vc1	1/V	-3.80E-07	-3.80E-07	-3.80E-07
	vc2	1/V^2	-4.30E-08	-4.30E-08	-4.30E-08
M4m1chb,	c0	F/m	-2.69E-11	-3.84E-11	-4.99E-11
	cf	F/m/finger	2.54E-10	3.63E-10	4.71E-10
M4m1chbxw	tc1	1/C	-5.17E-05	-3.80E-05	-2.43E-05
	Tc2	1/C^2	0	0	0
	vc1	1/V	-1.50E-06	-1.50E-06	-1.50E-06
	vc2	1/V^2	-5.90E-08	-5.90E-08	-5.90E-08
M4po1chb,	c0	F/m	-3.52E-12	-5.03E-12	-6.54E-12
	cf	F/m/finger	2.93E-10	4.19E-10	5.44E-10
M4po1chbxw	tc1	1/C	-2.43E-05	-3.80E-05	-5.17E-05
	Tc2	1/C^2	0	0	0
	vc1	1/V	-8.00E-06	-8.00E-06	-8.00E-06
	vc2	1/V^2	-2.00E-07	-2.00E-07	-2.00E-07
M4m1chp,	Ca	F/m^2	1.04E-04	1.49E-04	1.94E-04
	tc1	1/C	-5.00E-05	-5.00E-05	-5.00E-05
M4m1chpxw	Tc2	1/C^2	0	0	0
	vc1	1/V	-3.80E-07	-3.80E-07	-3.80E-07
	vc2	1/V^2	-4.30E-08	-4.30E-08	-4.30E-08
M4po1chp,	Ca	F/m^2	1.32E-04	1.88E-04	2.44E-04
	tc1	1/C	-5.00E-05	-5.00E-05	-5.00E-05
M4po1chpxw	Tc2	1/C^2	0	0	0
	vc1	1/V	-3.80E-07	-3.80E-07	-3.80E-07
	vc2	1/V^2	-4.30E-08	-4.30E-08	-4.30E-08
M5m1chb,	c0	F/m	-3.32E-11	-4.74E-11	-6.16E-11
	cf	F/m/finger	3.14E-10	4.48E-10	5.82E-10
M5m1chbxw	tc1	1/C	-4.76E-05	-3.50E-05	-2.24E-05
	Tc2	1/C^2	0	0	0
	vc1	1/V	-1.50E-06	-1.50E-06	-1.50E-06
	vc2	1/V^2	-5.90E-08	-5.90E-08	-5.90E-08
M5po1chb,	c0	F/m	-5.15E-12	-7.36E-12	-9.57E-12
	cf	F/m/finger	3.61E-10	5.15E-10	6.70E-10
M5po1chbxw	tc1	1/C	-2.43E-05	-3.80E-05	-5.17E-05
	Tc2	1/C^2	0	0	0
	vc1	1/V	-8.00E-06	-8.00E-06	-8.00E-06
	vc2	1/V^2	-2.00E-07	-2.00E-07	-2.00E-07

M5m1chp,	Ca	F/m^2	1.33E-04	1.90E-04	2.47E-04
	tc1	1/C	-5.00E-05	-5.00E-05	-5.00E-05
M5m1chpxw	Tc2	1/C^2	0	0	0
	vc1	1/V	-3.80E-07	-3.80E-07	-3.80E-07
	vc2	1/V^2	-4.30E-08	-4.30E-08	-4.30E-08
M5po1chp,	Ca	F/m^2	1.58E-04	2.26E-04	2.94E-04
	tc1	1/C	-5.00E-05	-5.00E-05	-5.00E-05
M5po1chpxw	Tc2	1/C^2	0	0	0
	vc1	1/V	-3.80E-07	-3.80E-07	-3.80E-07
	vc2	1/V^2	-4.30E-08	-4.30E-08	-4.30E-08
pipc	Cj	F/m^2	1.06E-3	9.42E-4	8.49E-4
	Cjsw	F/m	1.29E-10	8.20E-11	5.19E-11
	Etch	m	9.02E-9	1.04E-8	1.09E-8
	tc1	ppm/°C	30	25	20
	tc2	1/°C^2	0	0	0
	vc1	ppm/V	5	15	40
	vc2	ppm/V^2	-2.9	-3.45	-3.9

Poly Capacitor: PIPC – PIPCXW

PIPC - 2-port poly-poly capacitor, saleable according to the width and length.

PIPCXW – 3-port poly poly capacitor, saleable according to the width and length.

Module Name: CAP_P2P1_MTC_A (LAYOUT)

DR	Description	DUT1	DUT2	DUT3	DUT4
1	Capacitor Width	10	20	40	100
2	Capacitor Length	10	20	40	100
3	# of Caps in X	40	20	10	4
4	# of Caps in Y	40	20	10	4
5	POLY2 space	4	4	4	4
6	METAL1 width	2	2	2	2
7	# Dummy POLY2 stripes	1	1	1	1
8	Dummy POLY2 stripe width	5	5	5	5
	Total Capacitor Area (Cap 1)	80000	80000	80000	80000
	Total Capacitor Area (Cap 2)	80000	80000	80000	80000
	Total Capacitor Perimeter (Cap 1)	32000	16000	8000	3200
	Total Capacitor Perimeter (Cap 2)	32000	16000	8000	3200

Temperature	Device	Manual Measured (p)	Auto Measured (p)
27 C	DUT1	80.31E-12	77.76E-12
	DUT2	78.42E-12	76.60E-12
	DUT3	77.43E-12	76.03E-12
	DUT4	76.91E-12	75.68E-12

The measurements were measured at 100KHz with amplitude of 500mV.

I3T25 (0.35 um) Design Rules

Safe Operating Area

1000115 Rev: E

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I3T25 SAFE OPERATING AREA

DMOS Devices

The Safe Operating Area specifies the limit in drain and gate voltages, and on the corresponding current, during the device operation in order to avoid its degradation or destruction. For DMOS devices, two phenomena limit the SOA.

Safe Operating Area imposed by bipolar turn-on

The first phenomenon limiting the SOA of a DMOS transistor is the turn-on (and subsequent breakdown) of the parasitic bipolar (NPN for the NDMOS devices, PNP for the PDMOS devices): it depends on the instantaneous values of drain voltage and current. The turn-on of the parasitic bipolar is triggered by the DMOS bulk current. This current biases the Emitter/Base junction of the parasitic bipolar forward. This phenomenon is thus dependent on the currents flowing in the device and on the resistive path it follows, i.e. the bulk resistance under the source. The turn on of the bipolar happens immediately and subsequently the DMOS device is destroyed. Operating the DMOS device in the region where this can happen is therefore strictly forbidden.

Safe Operating Area imposed by hot carrier degradation

A second phenomenon defining the SOA of a DMOS is the degradation of the DMOS characteristics with the time, as the device is operated at high voltages or currents. This can be compared with the classic hot carrier degradation of conventional MOS transistors. Operating the devices in this region does not induce an immediate destruction of the device; however, a continuous operation of the transistor in this region can induce quite large shifts in the electrical parameters. The border of the safe operating region for this phenomenon is defined by a maximal degradation of 10% of any prime electrical, after 10 years of continuous operation at this condition.
The SOA presented in the following tables and plots is based contemporarily on the worst results of degradation due to hot carriers injection (HC), gate stress and reverse bias measurements.
In particular, the HC test monitor the maximum allowed shift of the main DC parameters of each transistor: 10% shift of bmax, Ron and IDSsat measured at different conditions) and 100mV variation of Vth0.
The resulting SOA reproduces the voltage ranges (Vgs;Vds) at which the worst case of parameter shift is reached in a time shorter than 10 years. The SOA referring to the parameter showing the fastest degradation is assumed as reference.

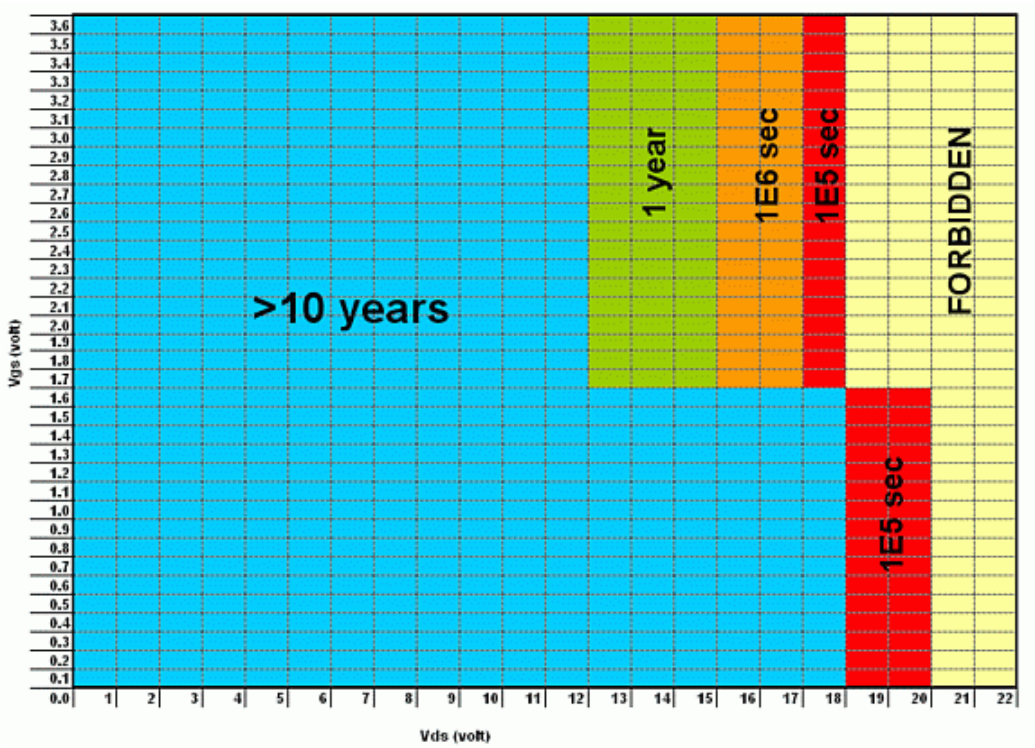
Thingate NDMOS: lfndm25

The following table and graph specify the lfndm25 lifetimes based on hot carrier shift in Ron, Vt_gm, and Idsat.

Thingate NDMOS Lifetimes - Table

DC lifetimes	(VGS, VDS) corresponding areas
10 years	0V<VGS<1.6V and 0V<VDS<18V - 0V<VGS<3.63V and 0V<VDS<12V
1 year	0V<VGS<3.6V and 0V<VDS<15V
1e6 seconds	0V<VGS<3.6V and 0V<VDS<17V
1e5 seconds	0V<VGS<1.6V and 0V<VDS<20V - 0V<VGS<3.63V and 0V<VDS<18V

Thingate NDMOS Lifetimes - Graph



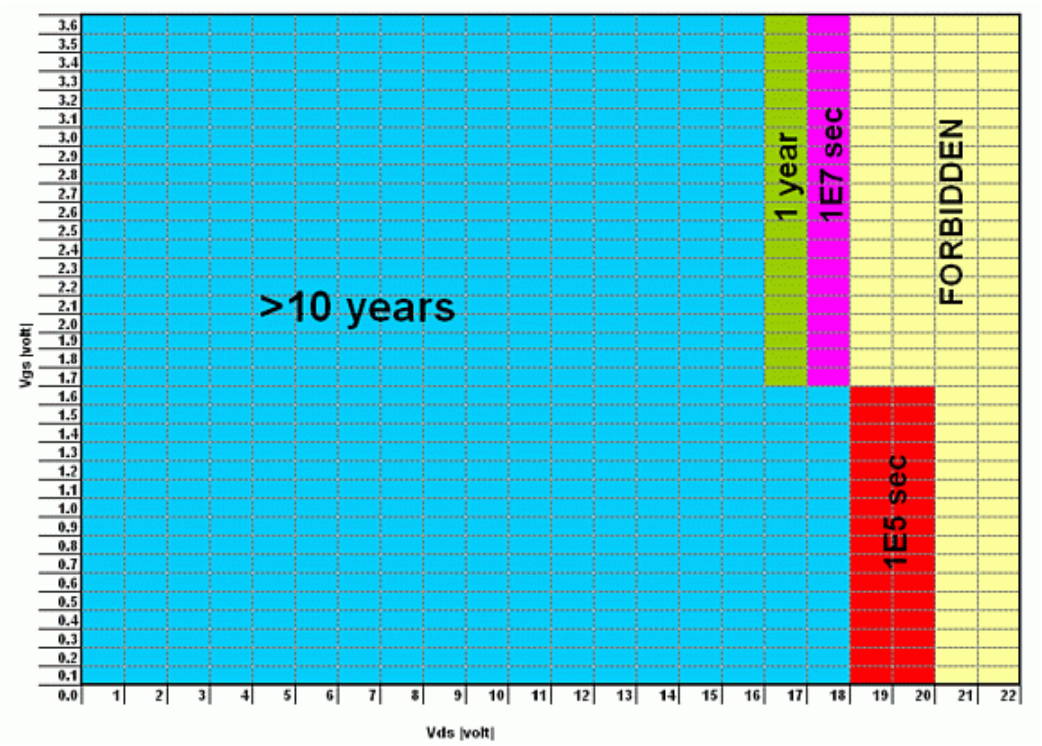
Thingate PDMOS: lfpdm25

The following table and graph specify the lfpdm25 lifetimes based on hot carrier shift in Ron, Vt_gm, and Idsat.

Thingate PDMOS Lifetimes - Table

DC lifetimes	(VGS, VDS) corresponding areas
10 years	0V<VGS<1.6V and 0V<VDS<18V - 0V<VGS<3.63V and 0V<VDS<16V
1 year	0V<VGS<3.6V and 0V<VDS<17V
1e7 seconds	0V<VGS<3.6V and 0V<VDS<18V
1e5 seconds	0V<VGS<1.6V and 0V<VDS<20V

Thingate PDMOS Lifetimes - Graph



Wafer level Hot Carrier Injection (HCI) tests

Wafer level Hot Carrier Injection (HCI) tests were preformed on LFNDM14, LFNDM25, LFPDM25, LFPDM25D, LFNDM25T, LFPDM25T, LFNDM25DT, LFPDM25DT, LFNDM20NT, LPNDM20NT, LFNDM20DNT, LPNDM20DNT device transistors with a 70Å or 300Å SiO_2 gate dielectric processed at the ON Semiconductor's Pocatello Idaho wafer fabrication facility.

Each device was stressed at 30ºC with multiple combinations of DC voltage applied to the drain versus gate for 10000 seconds, following the requirements found in the JEDAC/FSA Joint Publication JP001.01 pg 13, JESD60A, JESD28-A and ON Semiconductor document 1000072. Device lifetimes were calculated for a 10% shift to assess the degradation of device parametric G_{MMAX}, V_{t0}, R_{on} and I_{dSat} in order to create a Safe Operating Area (SOA) model using the Takeda model formula.

Minimum device lifetimes under these conductions and results are listed below.

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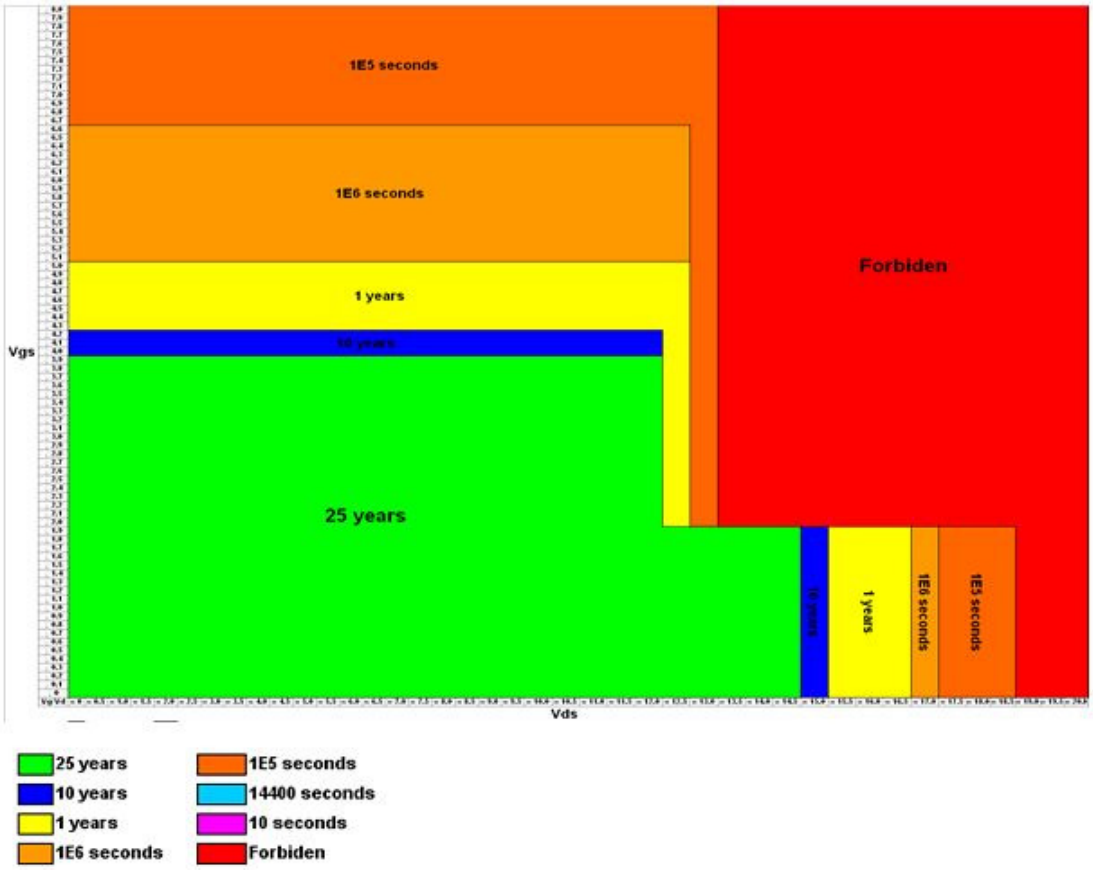
1. **HOT CARRIER INJECTION Stress (HCI) Experiment on LFNDM14 40X1**

A. HCI DC Lifetime and Voltage Safe Operating Area Table

DC Lifetime	Voltage Range
>25 yrs when	0V < Vds ≤ 12.5V & 0V < Vgs ≤ 4.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ 17.0V & 0V < Vgs ≤ 2.0V & Vs = 0V & Vb = 0V
>10 yrs when	0V < Vds ≤ 12.5V & 0V < Vgs ≤ 4.3V & Vs = 0V & Vb = 0V 0V < Vds ≤ 15.5V & 0V < Vgs ≤ 2.0V & Vs = 0V & Vb = 0V
>1 yrs when	0V < Vds ≤ 13.0V & 0V < Vgs ≤ 5.1V & Vs = 0V & Vb = 0V 0V < Vds ≤ 17.0V & 0V < Vgs ≤ 2.0V & Vs = 0V & Vb = 0V
>1E6 sec when	0V < Vds ≤ 13.0V & 0V < Vgs ≤ 6.7V & Vs = 0V & Vb = 0V 0V < Vds ≤ 17.5V & 0V < Vgs ≤ 2.0V & Vs = 0V & Vb = 0V
>1E5 sec when	0V < Vds ≤ 13.5V & 0V < Vgs ≤ 8.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ 19.0V & 0V < Vgs ≤ 2.0V & Vs = 0V & Vb = 0V

Table 1: HCI DC Lifetime and Voltage Safe Operating Area Table

B. HCI DC Lifetime and Voltage Safe Operating Area Chart



Parametric parameter Ron2 was used to create SOA

Figure 1: HCI DC Lifetime and Voltage Safe Operating Area Chart

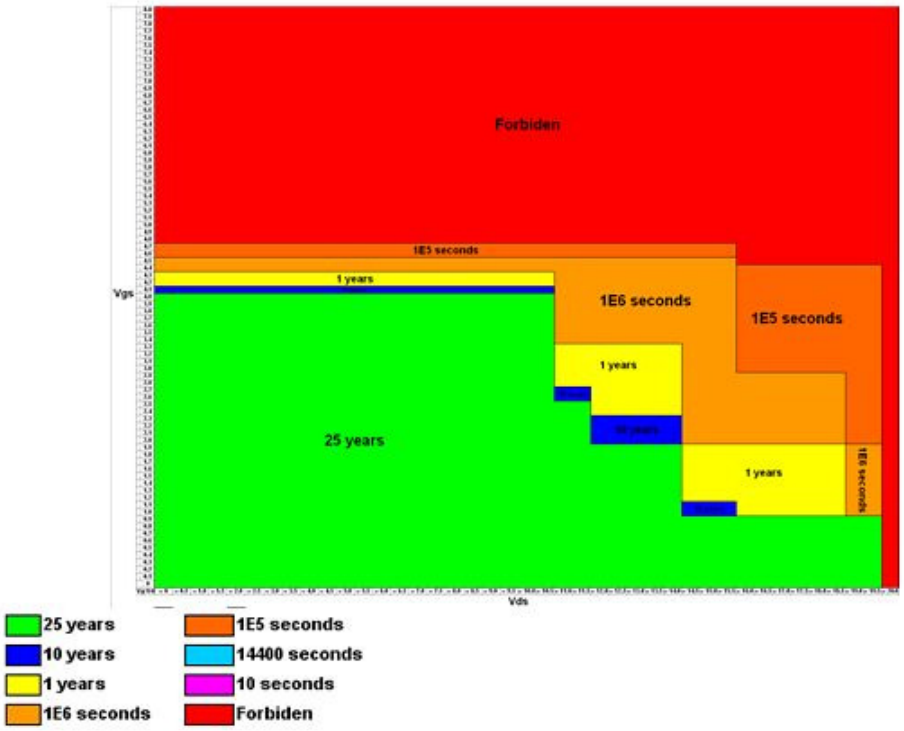
2. HOT CARRIER INJECTION Stress (HCI) Experiment on LFNDM25 40x2.8

A. HCI DC Lifetime and Voltage Safe Operating Area Table

DC Lifetime	Voltage Range
>25 yrs when	0V < Vds ≤ 11.0V & 0V < Vgs ≤ 4.1V & Vs = 0V & Vb = 0V 0V < Vds ≤ 12.0V & 0V < Vgs ≤ 2.6V & Vs = 0V & Vb = 0V 0V < Vds ≤ 14.5V & 0V < Vgs ≤ 2.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ 20.0V & 0V < Vgs ≤ 1.0V & Vs = 0V & Vb = 0V
>10 yrs when	0V < Vds ≤ 11.0V & 0V < Vgs ≤ 4.2V & Vs = 0V & Vb = 0V 0V < Vds ≤ 12.0V & 0V < Vgs ≤ 2.8V & Vs = 0V & Vb = 0V 0V < Vds ≤ 14.5V & 0V < Vgs ≤ 2.4V & Vs = 0V & Vb = 0V 0V < Vds ≤ 16.0V & 0V < Vgs ≤ 1.2V & Vs = 0V & Vb = 0V
>1 yrs when	0V < Vds ≤ 11.0V & 0V < Vgs ≤ 4.4V & Vs = 0V & Vb = 0V 0V < Vds ≤ 14.5V & 0V < Vgs ≤ 3.4V & Vs = 0V & Vb = 0V 0V < Vds ≤ 19.0V & 0V < Vgs ≤ 2.0V & Vs = 0V & Vb = 0V
>1E6 sec when	0V < Vds ≤ 16.0V & 0V < Vgs ≤ 4.6V & Vs = 0V & Vb = 0V 0V < Vds ≤ 19.0V & 0V < Vgs ≤ 3.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ 20.0V & 0V < Vgs ≤ 2.0V & Vs = 0V & Vb = 0V
>1E5 sec when	0V < Vds ≤ 16.0V & 0V < Vgs ≤ 4.8V & Vs = 0V & Vb = 0V 0V < Vds ≤ 20.0V & 0V < Vgs ≤ 4.5V & Vs = 0V & Vb = 0V

Table 2: HCI DC Lifetime and Voltage Safe Operating Area Table

B. HCI DC Lifetime and Voltage Safe Operating Area Chart



Parametric parameter Ron2 was used to create SOA

Figure 2: HCI DC Lifetime and Voltage Safe Operating Area Chart

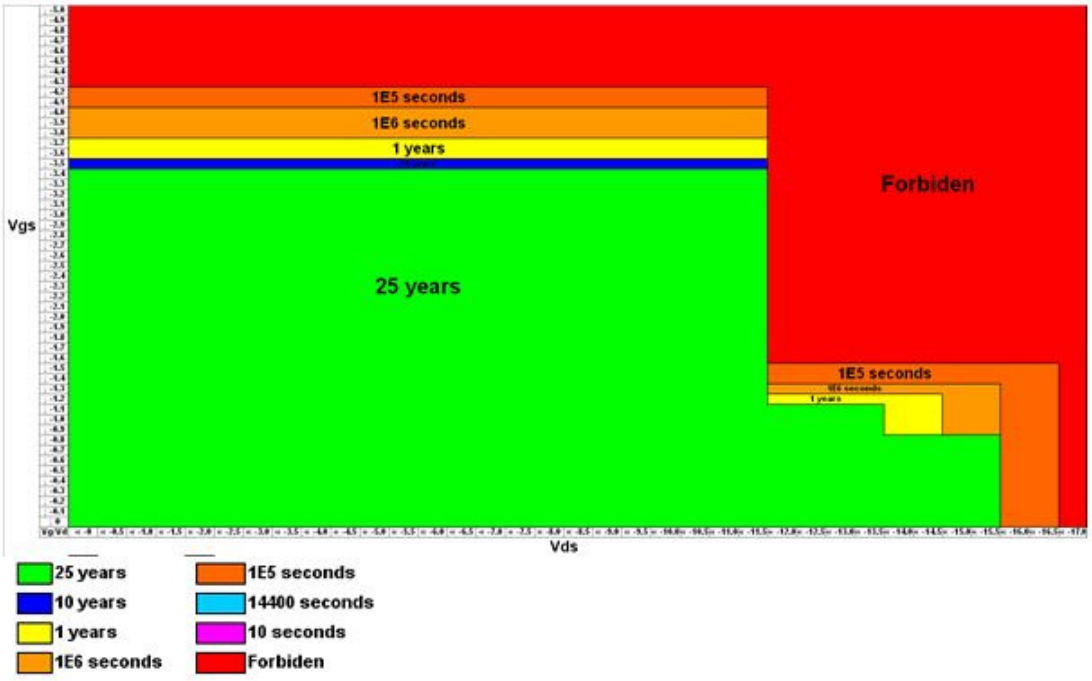
3. HOT CARRIER INJECTION Stress (HCI) Experiment on LFPDM25 40x2.1

A. HCI DC Lifetime and Voltage Safe Operating Area Table

DC Lifetime	Voltage Range
>25 yrs when	0V < Vds ≤ -12.0V & 0V < Vgs ≤ -3.5V & Vs = 0V & Vb = 0V 0V < Vds ≤ -14.0V & 0V < Vgs ≤ -1.2V & Vs = 0V & Vb = 0V 0V < Vds ≤ -16.0V & 0V < Vgs ≤ -0.9V & Vs = 0V & Vb = 0V
>10 yrs when	0V < Vds ≤ -12.0V & 0V < Vgs ≤ -3.6V & Vs = 0V & Vb = 0V
>1 yrs when	0V < Vds ≤ -12.0V & 0V < Vgs ≤ -3.8V & Vs = 0V & Vb = 0V 0V < Vds ≤ -15.0V & 0V < Vgs ≤ -1.3V & Vs = 0V & Vb = 0V
>1E6 sec when	0V < Vds ≤ -12.0V & 0V < Vgs ≤ -4.1V & Vs = 0V & Vb = 0V 0V < Vds ≤ -15.0V & 0V < Vgs ≤ -1.4V & Vs = 0V & Vb = 0V
>1E5 sec when	0V < Vds ≤ -12.0V & 0V < Vgs ≤ -4.3V & Vs = 0V & Vb = 0V 0V < Vds ≤ -15.0V & 0V < Vgs ≤ -1.6V & Vs = 0V & Vb = 0V

Table 3: HCI DC Lifetime and Voltage Safe Operating Area Table

B. HCI DC Lifetime and Voltage Safe Operating Area Chart



Parametric parameter Ron2 was used to create SOA.

Figure 3: HCI DC Lifetime and Voltage Safe Operating Area Chart

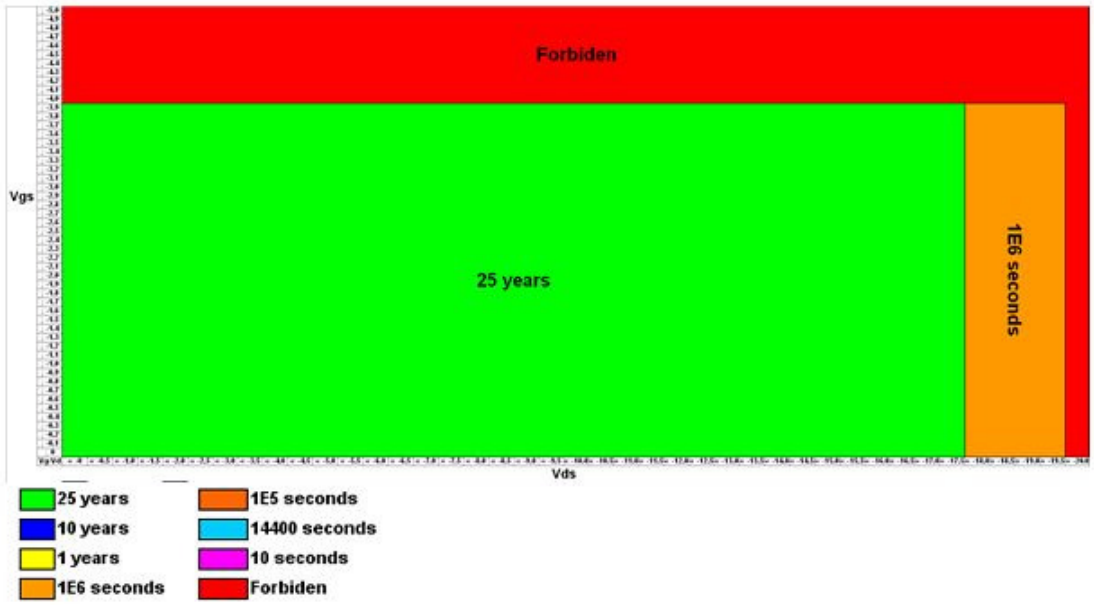
4. HOT CARRIER INJECTION Stress (HCI) Experiment on LFPDM25D 40x2.2

A. HCI DC Lifetime and Voltage Safe Operating Area Table

DC Lifetime	Voltage Range
>25 yrs when	0V < Vds ≤ -18V & 0V < Vgs ≤ -4V & Vs = 0V & Vb = 0V
>1E6 sec when	0V < Vds ≤ -20V & 0V < Vgs ≤ -4V & Vs = 0V & Vb = 0V

Table 4: HCI DC Lifetime and Voltage Safe Operating Area Table

B. HCI DC Lifetime and Voltage Safe Operating Area Chart



Parametric parameter Ron2 was used to create SOA

Figure 4: HCI DC Lifetime and Voltage Safe Operating Area Chart

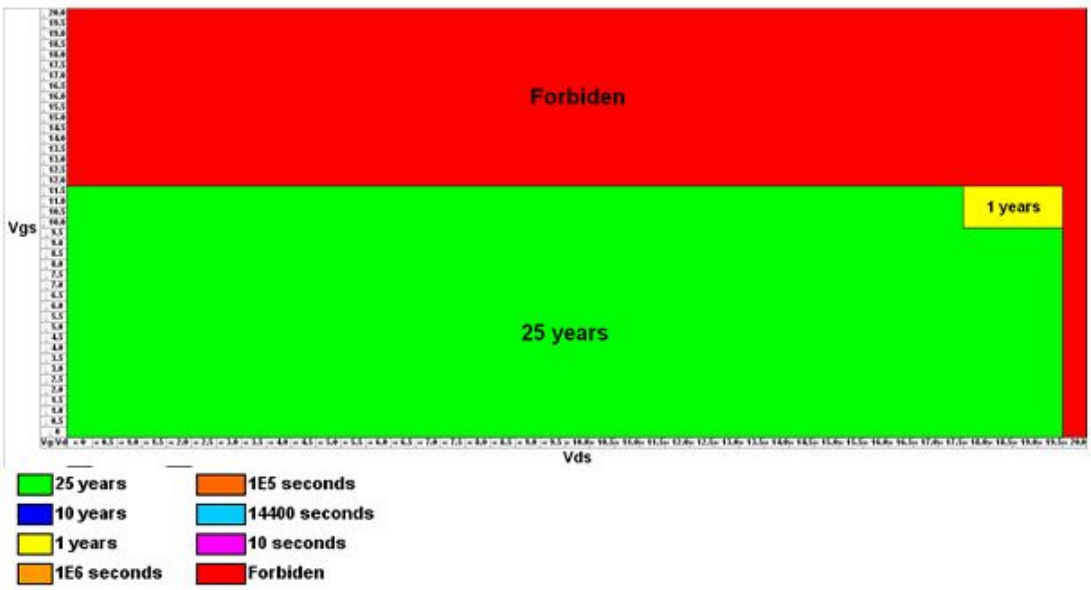
5. HOT CARRIER INJECTION Stress (HCI) Experiment on LFNDM25T 40x3.25

A. HCI DC Lifetime and Voltage Safe Operating Area Table

DC Lifetime	Voltage Range
>25 yrs when	0V < Vds ≤ 18.0V & 0V < Vgs ≤ 12.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ 20.0V & 0V < Vgs ≤ 10.0V & Vs = 0V & Vb = 0V
>10 yrs when	0V < Vds ≤ 20.0V & 0V < Vgs ≤ 12.0V & Vs = 0V & Vb = 0V

Table 5: HCI DC Lifetime and Voltage Safe Operating Area Table

B. HCI DC Lifetime and Voltage Safe Operating Area Chart



Parametric parameter Ron2 was used to create SOA.

Figure 5: HCI DC Lifetime and Voltage Safe Operating Area Chart

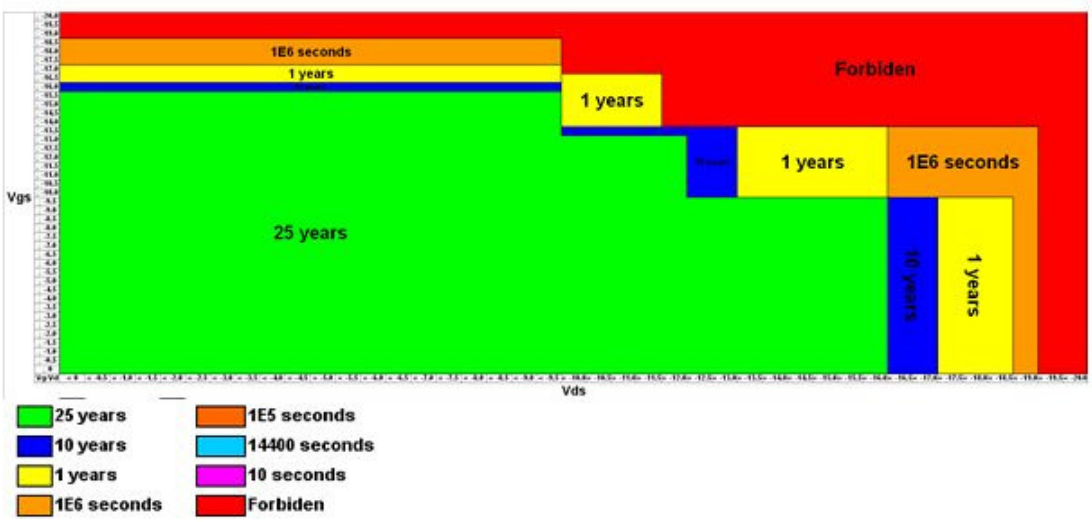
6. HOT CARRIER INJECTION Stress (HCI) Experiment on LFPDM25T 40x2.65

A. HCI DC Lifetime and Voltage Safe Operating Area Table

DC Lifetime	Voltage Range
>25 yrs when	0V < Vds ≤ -10.0V & 0V < Vgs ≤ -16.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ -12.5V & 0V < Vgs ≤ -13.5V & Vs = 0V & Vb = 0V 0V < Vds ≤ -16.5V & 0V < Vgs ≤ -10.0V & Vs = 0V & Vb = 0V
>10 yrs when	0V < Vds ≤ -10.0V & 0V < Vgs ≤ -16.5V & Vs = 0V & Vb = 0V 0V < Vds ≤ -13.5V & 0V < Vgs ≤ -14.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ -17.5V & 0V < Vgs ≤ -10.0V & Vs = 0V & Vb = 0V
>1 yrs when	0V < Vds ≤ -10.0V & 0V < Vgs ≤ -17.5V & Vs = 0V & Vb = 0V 0V < Vds ≤ -12.0V & 0V < Vgs ≤ -17.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ -16.5V & 0V < Vgs ≤ -14.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ -19.0V & 0V < Vgs ≤ -10.0V & Vs = 0V & Vb = 0V
>1E6 sec when	0V < Vds ≤ -10.0V & 0V < Vgs ≤ -19.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ -19.5V & 0V < Vgs ≤ -14.0V & Vs = 0V & Vb = 0V

Table 6: HCI DC Lifetime and Voltage Safe Operating Area Table

B. HCI DC Lifetime and Voltage Safe Operating Area Chart



Parametric parameter Ron2 was used to create SOA

Figure 6: HCI DC Lifetime and Voltage Safe Operating Area Chart

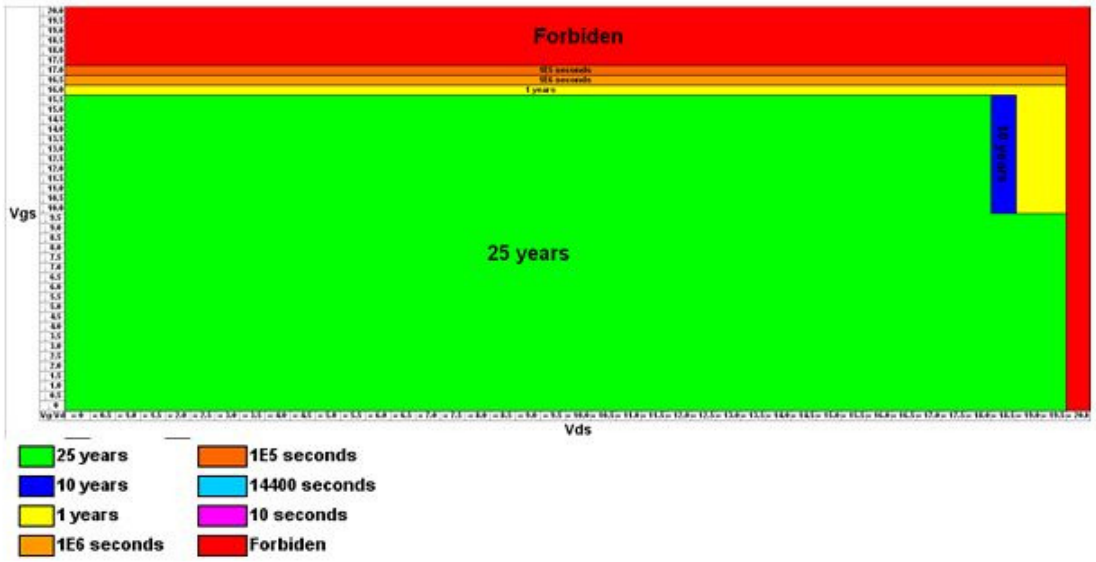
7. HOT CARRIER INJECTION Stress (HCI) Experiment on LFNDM25DT 40x4

A. HCI DC Lifetime and Voltage Safe Operating Area Table

DC Lifetime	Voltage Range
>25 yrs when	0V < Vds ≤ 18.0V & 0V < Vgs ≤ 16.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ 20.0V & 0V < Vgs ≤ 10.0V & Vs = 0V & Vb = 0V
>10 yrs when	0V < Vds ≤ 19.0V & 0V < Vgs ≤ 16.0V & Vs = 0V & Vb = 0V
>1 yrs when	0V < Vds ≤ 16.5V & 0V < Vgs ≤ 20.0V & Vs = 0V & Vb = 0V
>1E6 sec when	0V < Vds ≤ 17.0V & 0V < Vgs ≤ 20.0V & Vs = 0V & Vb = 0V
>1E5 sec when	0V < Vds ≤ 17.5V & 0V < Vgs ≤ 20.0V & Vs = 0V & Vb = 0V

Table 7: HCI DC Lifetime and Voltage Safe Operating Area Table

B. HCI DC Lifetime and Voltage Safe Operating Area Chart



Parametric parameter Ron2 was used to create SOA

Figure 7: HCI DC Lifetime and Voltage Safe Operating Area Chart

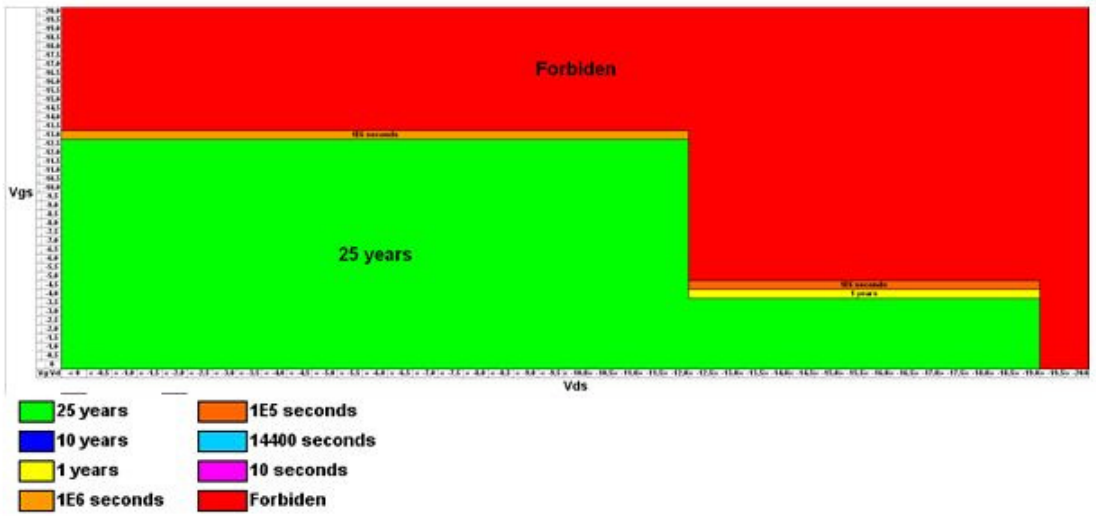
8. HOT CARRIER INJECTION Stress (HCI) Experiment on LFPDM25DT 40x2

A. HCI DC Lifetime and Voltage Safe Operating Area Table

DC Lifetime	Voltage Range
>25 yrs when	0V < Vds ≤ -12.5V & 0V < Vgs ≤ -13.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ -19.5V & 0V < Vgs ≤ -4.0V & Vs = 0V & Vb = 0V
>1 yrs when	0V < Vds ≤ -19.5V & 0V < Vgs ≤ -4.5V & Vs = 0V & Vb = 0V
>1E6 sec when	0V < Vds ≤ -12.5V & 0V < Vgs ≤ -13.5V & Vs = 0V & Vb = 0V 0V < Vds ≤ -19.5V & 0V < Vgs ≤ -5.0V & Vs = 0V & Vb = 0V

Table 8: HCI DC Lifetime and Voltage Safe Operating Area Table

B. HCI DC Lifetime and Voltage Safe Operating Area Chart



Parametric parameter Ron2 was used to create SOA

Figure 8: HCI DC Lifetime and Voltage Safe Operating Area Chart

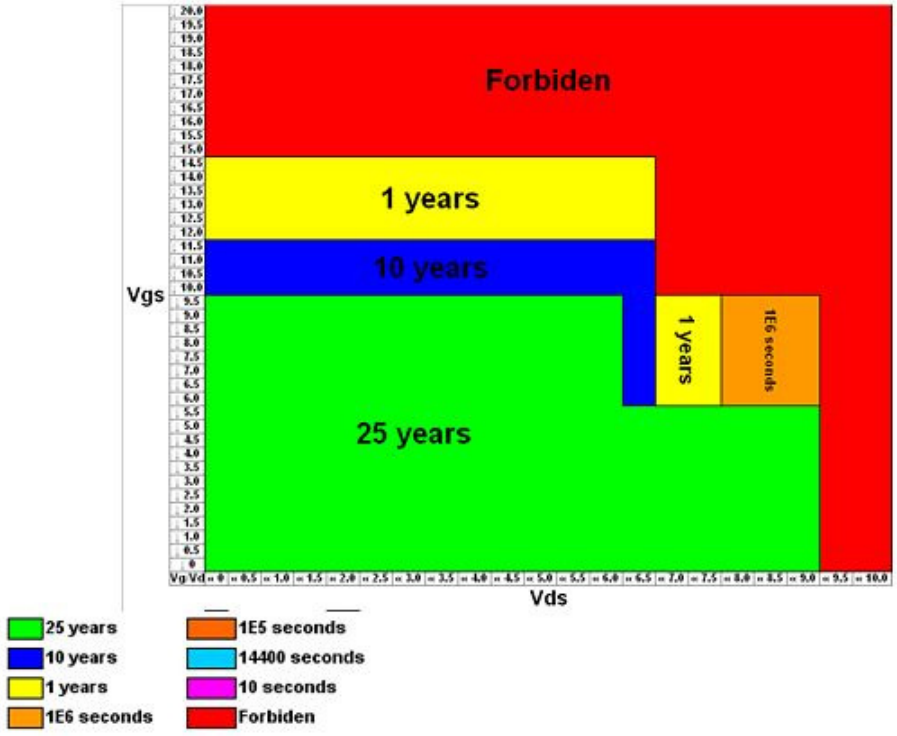
9. HOT CARRIER INJECTION STRESS (HCI) EXPERIMENT ON LFNDM20NT 40X1.6

A. HCI DC Lifetime and Voltage Safe Operating Area Table

DC Lifetime	Voltage Range
>25 yrs when	0V < Vds ≤ 6.5V & 0V < Vgs ≤ 10.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ 9.5V & 0V < Vgs ≤ 6.0V & Vs = 0V & Vb = 0V
>10 yrs when	0V < Vds ≤ 7.0V & 0V < Vgs ≤ 12.0V & Vs = 0V & Vb = 0V
>1 yrs when	0V < Vds ≤ 7.0V & 0V < 15.0Vgs ≤ V & Vs = 0V & Vb = 0V 0V < Vds ≤ 8.0V & 0V < 10.0Vgs ≤ V & Vs = 0V & Vb = 0V
>1E6 sec when	0V < Vds ≤ 9.5V & 0V < Vgs ≤ 10.0V & Vs = 0V & Vb = 0V

Table 9: HCI DC Lifetime and Voltage Safe Operating Area Table

B. HCI DC Lifetime and Voltage Safe Operating Area Chart



Parametric parameter Ron2 was used to create SOA

Figure 9: HCI DC Lifetime and Voltage Safe Operating Area Chart

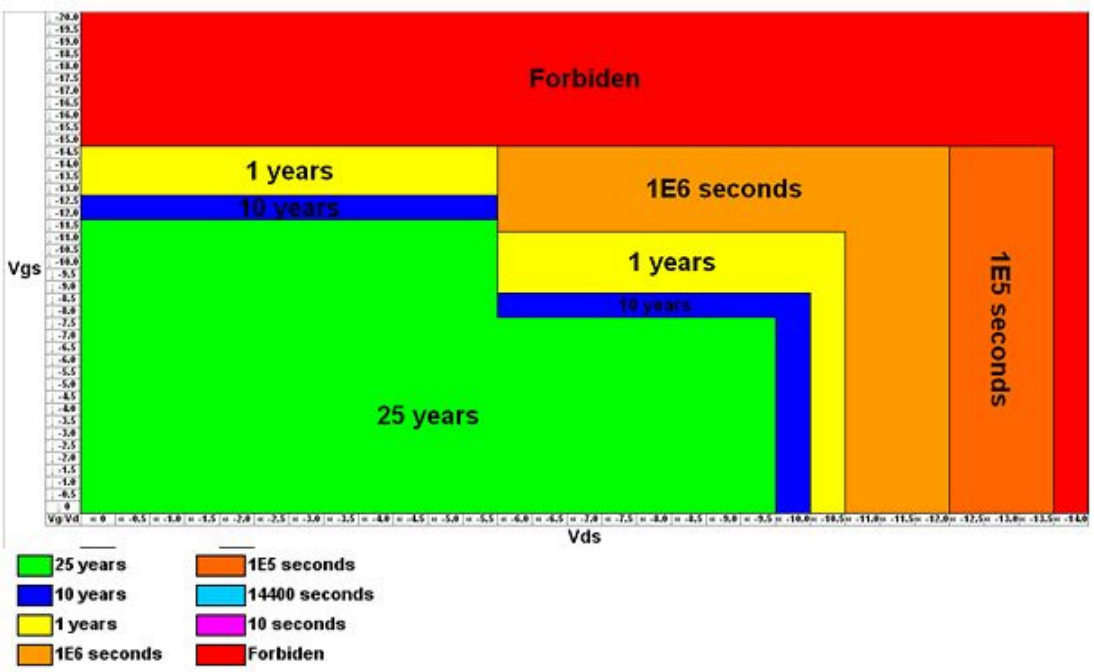
10. HOT CARRIER INJECTION Stress (HCI) Experiment on LFPDM20NT 40x1.3

A. HCI DC Lifetime and Voltage Safe Operating Area Table

DC Lifetime	Voltage Range
>25 yrs when	0V < Vds ≤ -6.0V & -0V < Vgs ≤ -12.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ -10.0V & -0V < Vgs ≤ -8.0V & Vs = 0V & Vb = 0V
>10 yrs when	0V < Vds ≤ -6.0V & -0V < Vgs ≤ -13.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ -10.5V & -0V < Vgs ≤ -9.0V & Vs = 0V & Vb = 0V
>1 yrs when	0V < Vds ≤ -6.0V & -0V < Vgs ≤ -15.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ -11.0V & -0V < Vgs ≤ -11.5V & Vs = 0V & Vb = 0V
>1E6 sec when	0V < Vds ≤ -12.5V & -0V < Vgs ≤ -15.0V & Vs = 0V & Vb = 0V
>1E5 sec when	0V < Vds ≤ -14.0V & -0V < Vgs ≤ -15.0V & Vs = 0V & Vb = 0V

Table 10: HCI DC Lifetime and Voltage Safe Operating Area Table

B. HCI DC Lifetime and Voltage Safe Operating Area Chart



Parametric parameter Ron2 was used to create SOA

Figure 10: HCI DC Lifetime and Voltage Safe Operating Area Chart

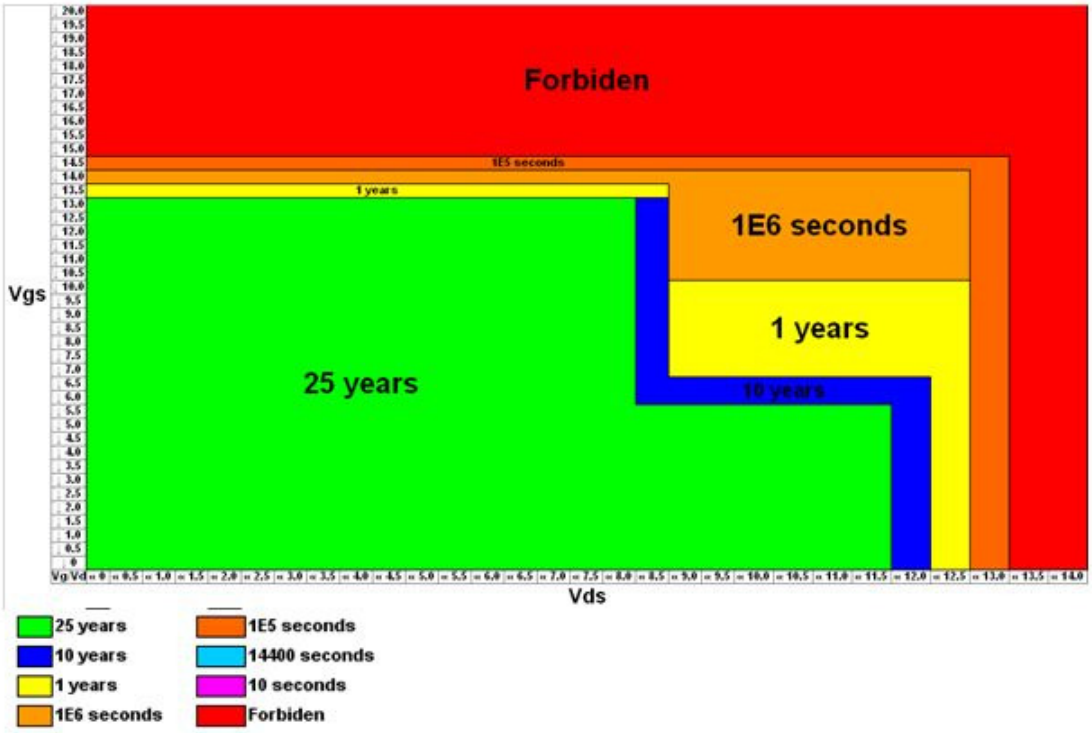
11. HOT CARRIER INJECTION Stress (HCI) Experiment on LFNDM20DNT 40x5.2

A. HCI DC Lifetime and Voltage Safe Operating Area Table

DC Lifetime	Voltage Range
>25 yrs when	0V < Vds ≤ 8.5V & 0V < Vgs ≤ 13.5V & Vs = 0V & Vb = 0V 0V < Vds ≤ 12.0V & 0V < Vgs ≤ 6.0V & Vs = 0V & Vb = 0V
>10 yrs when	0V < Vds ≤ 9.0V & 0V < Vgs ≤ 13.5V & Vs = 0V & Vb = 0V 0V < Vds ≤ 12.5V & 0V < Vgs ≤ 7.0V & Vs = 0V & Vb = 0V
>1 yrs when	0V < Vds ≤ 9.0V & 0V < Vgs ≤ 14.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ 13.0V & 0V < Vgs ≤ 10.5V & Vs = 0V & Vb = 0V
>1E6 sec when	0V < Vds ≤ 13.0V & 0V < Vgs ≤ 14.5V & Vs = 0V & Vb = 0V
>1E5 sec when	0V < Vds ≤ 13.5V & 0V < Vgs ≤ 15.0V & Vs = 0V & Vb = 0V

Table 11: HCI DC Lifetime and Voltage Safe Operating Area Table

B. HCI DC Lifetime and Voltage Safe Operating Area Chart



Parametric parameter Ron2 was used to create SOA

Figure 11: HCI DC Lifetime and Voltage Safe Operating Area Chart

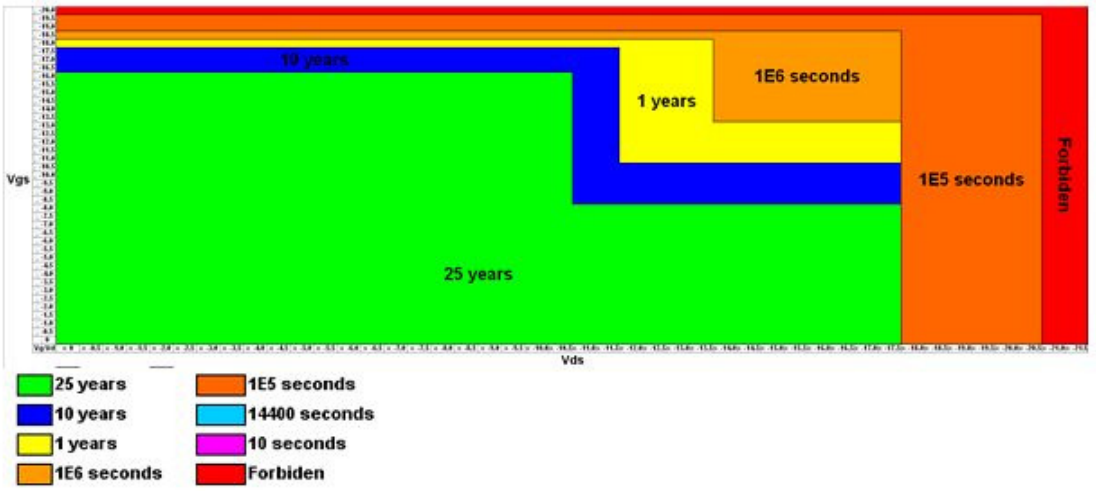
12. HOT CARRIER INJECTION Stress (HCI) Experiment on LFPDM20DNT 40x3.2

A. HCI DC Lifetime and Voltage Safe Operating Area Table

DC Lifetime	Voltage Range
>25 yrs when	0V < Vds ≤ -11.0V & 0V < Vgs ≤ -16.5V & Vs = 0V & Vb = 0V 0V < Vds ≤ -18.0V & 0V < Vgs ≤ -8.5V & Vs = 0V & Vb = 0V
>10 yrs when	0V < Vds ≤ -12.0V & 0V < Vgs ≤ -18.0V & Vs = 0V & Vb = 0V 0V < Vds ≤ -18.0V & 0V < Vgs ≤ -11.0V & Vs = 0V & Vb = 0V
>1 yrs when	0V < Vds ≤ -14.0V & 0V < Vgs ≤ -18.5V & Vs = 0V & Vb = 0V 0V < Vds ≤ -18.0V & 0V < Vgs ≤ -13.5V & Vs = 0V & Vb = 0V
>1E6 sec when	0V < Vds ≤ -18.0V & 0V < Vgs ≤ -19.0V & Vs = 0V & Vb = 0V
>1E6 sec when	0V < Vds ≤ -20.0V & 0V < Vgs ≤ -21.0V & Vs = 0V & Vb = 0V

Table 12: HCI DC Lifetime and Voltage Safe Operating Area Table

B. HCI DC Lifetime and Voltage Safe Operating Area Chart



Parametric parameter Ron2 was used to create SOA

Figure 12: HCI DC Lifetime and Voltage Safe Operating Area Chart