# D2 Interim Report

## Team Z

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Jane Smith
Vincent Dummy

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# Interim Report Section A

This section of the sample report will give you extra information about the requirements for your interim report.

## Section A

A brief text description of your design, no more than one side of A4.

## Section B

The ciruit diagram showing your design before the addition of testability should meet the following requirements:
- It should contain only the input pads described in the design specification.
- In addition to the output pads described in the design specification you may include other important outputs. You should not clutter your diagram with output pads.
- You may (and should) use wire labels to make your schematic more readable. Using *join by name* as described in the Gate Array documentation will alllow you to separate your design into more readable blocks in order to avoid spaghetti wiring without adding unnecessary input pads or output pads.
- No wire or pad name should contain the underscore character, _.

## Section C

The annotated circuit diagram showing exactly how your design is implemented should match your implementation gate for gate and pad for pad. Obvious failures here are diagrams with more than 14 input pads or more than 17 output pads. Other common problems include a single gate on the schematic turning into two identical gates on the layout or two identical gates on the schematic implemented as one gate on the layout. Liberal use of wire labels (in addition to the essential gate name annotations) should help to reduce these problems.

## Section D

The CGA Template for your design should match the annotated diagram gate for gate and pad for pad. Ensure that the gate names here are unique so that you can see exactly which gate from the annotated diagram corresponds to any gate on the template. The template should of course also match the layout.

## Section E

The netlist is the `netlist.txt` file returned when you netlist your layout.

## Section F

The pinout is the `pinout.txt` file returned when you netlist your layout.

## Section G

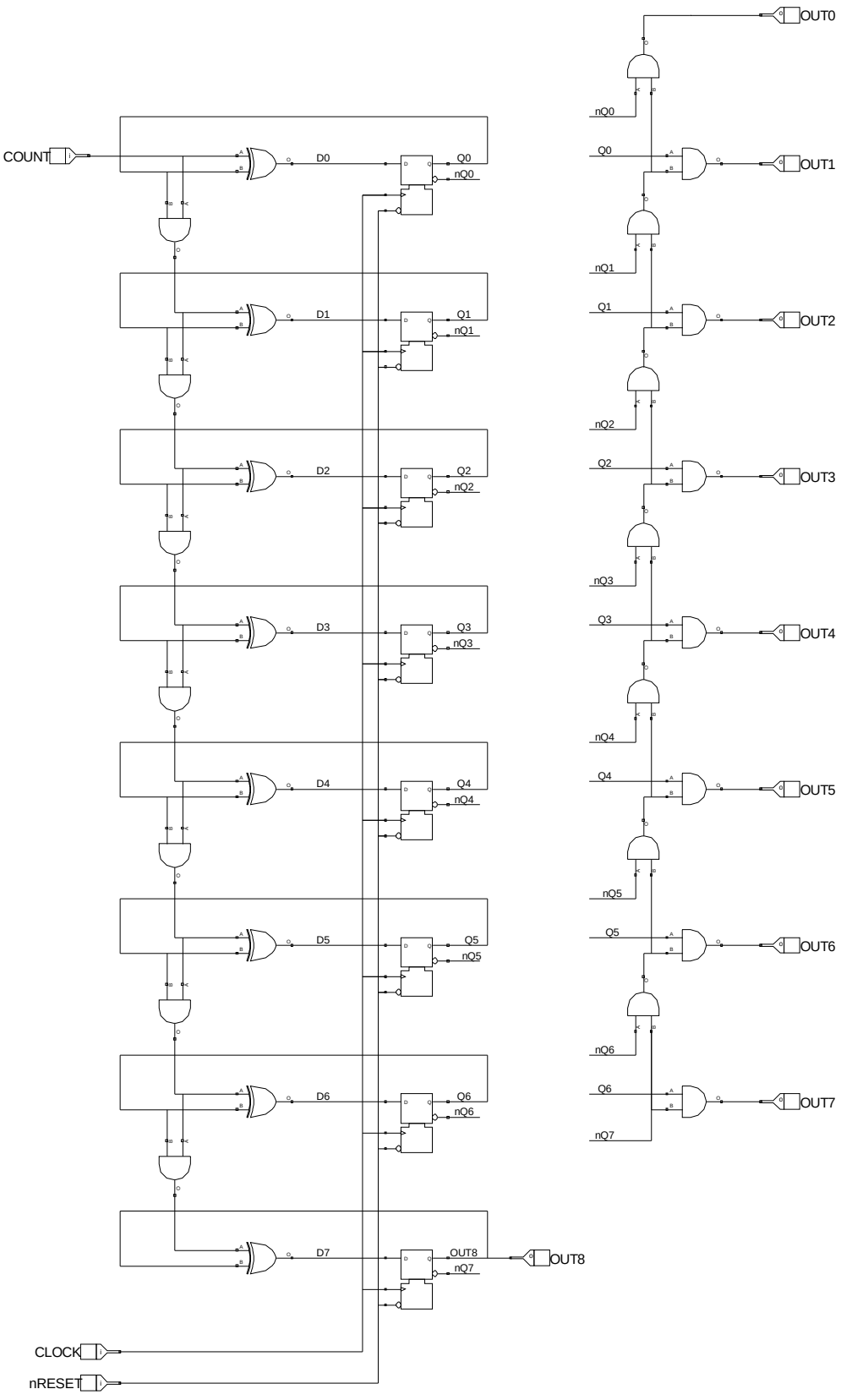
The simulation should include one or more waveform plots to show functionality and should also include relevent text information such as the "Simulation OK" message. Don't be afraid to use glue and scissors to produce the right information. The simulation should be for the layout rather than one of the schematics.

## Section H

The design submission form gives details of the submission and of the division of work. This is your opportunity to tell us of your input to the design and to flag team members who aren't pulling their weight.

Interim Report Section B

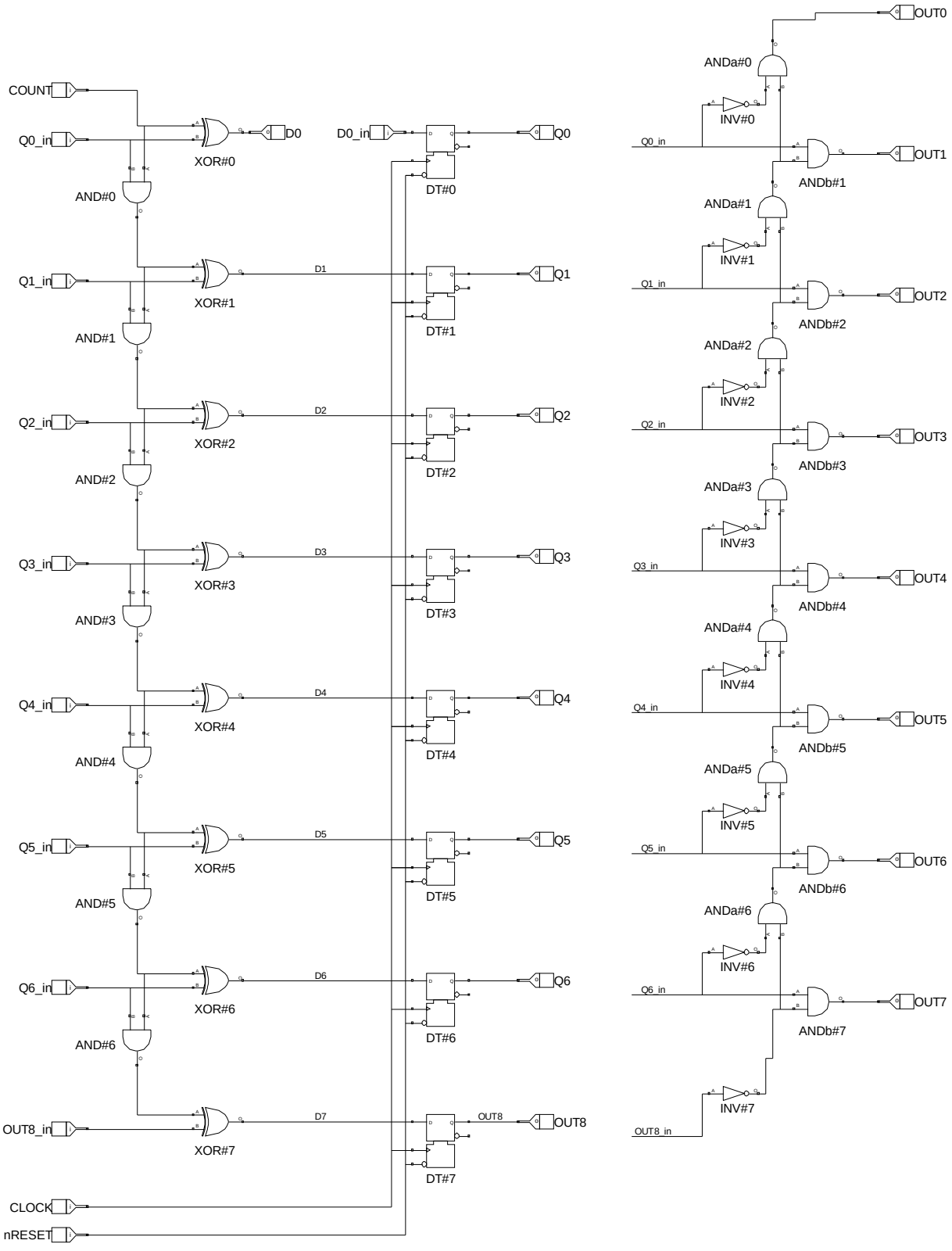
# Circuit Diagram for a Logarithmic Thingy



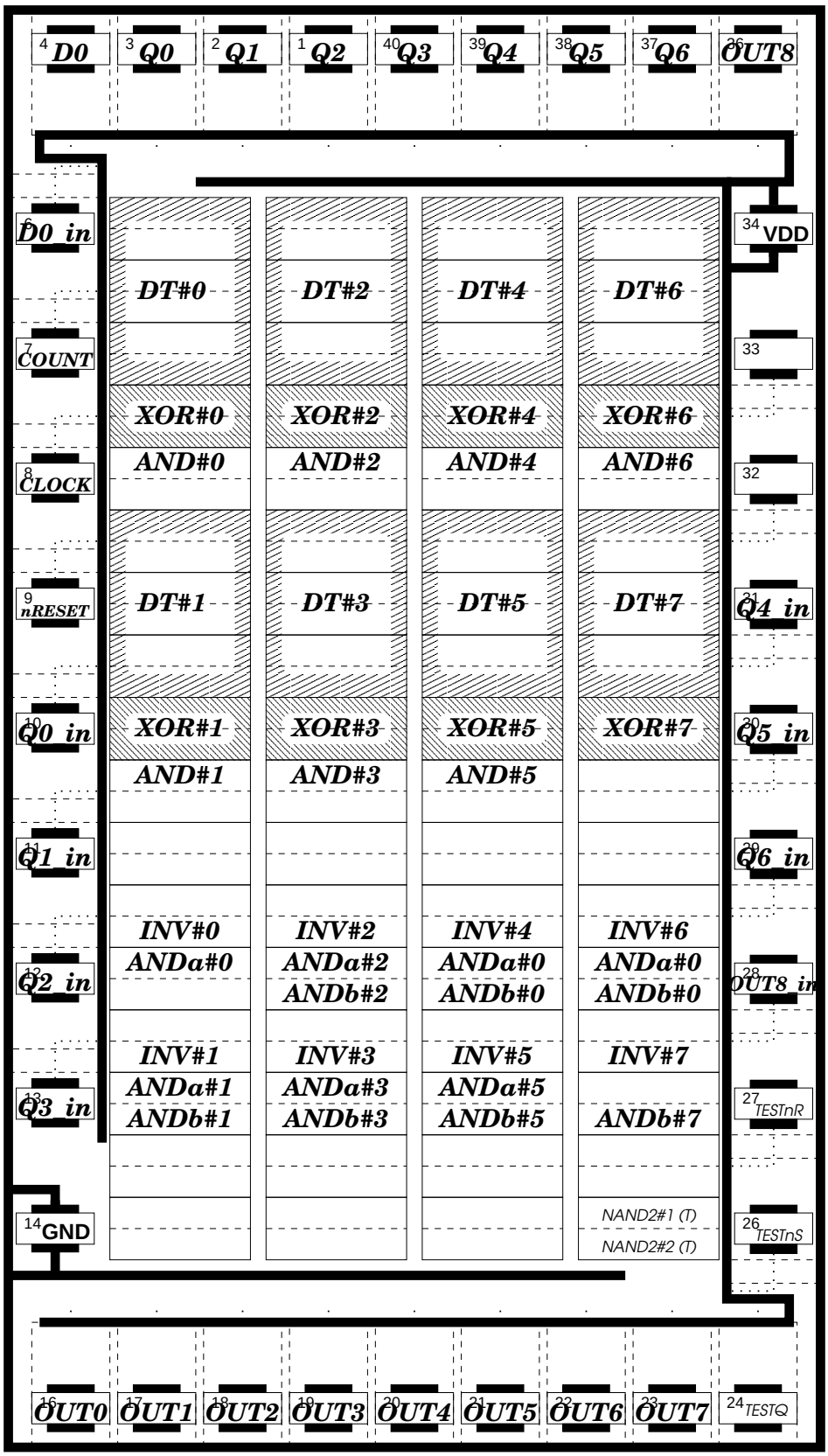
Interim Report Section C

# Circuit Diagram for a Logarithmic Thingy

including testability and gate name annotation



# CMOS Gate Array Placement Template



## Netlist for Layout

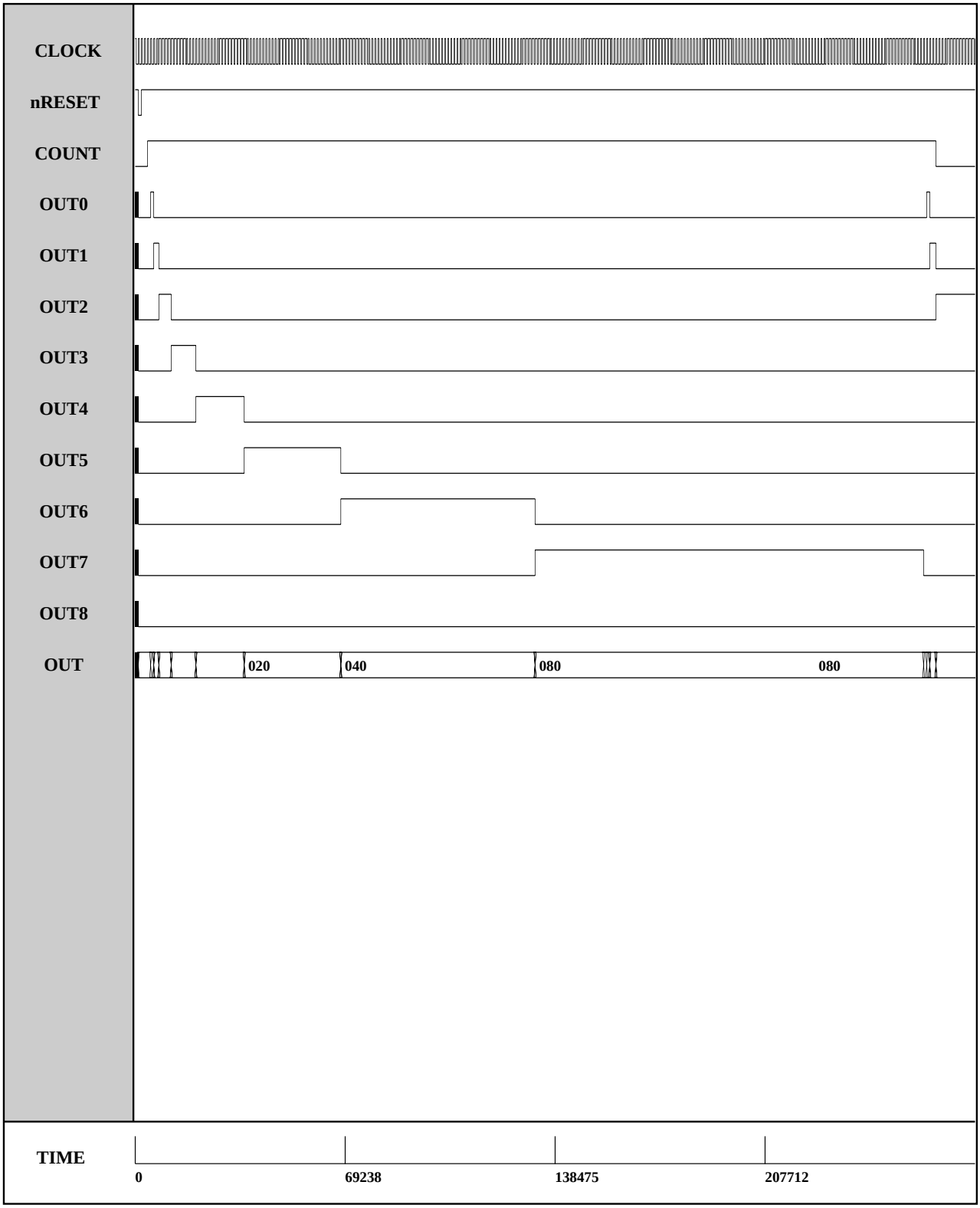
```
//Netlist for cell layout from library teamz

//Design extracted ok

and #1 I17 ( OUT0 , not38 , and30 );
and #1 I18 ( OUT1 , Q0_in , and30 );
and #1 I19 ( and19 , not44 , not39 );
and #1 I20 ( OUT7 , Q6_in , not39 );
and #1 I21 ( and21 , not40 , and19 );
and #1 I22 ( OUT6 , Q5_in , and19 );
and #1 I23 ( and23 , not41 , and21 );
and #1 I24 ( OUT5 , Q4_in , and21 );
and #1 I25 ( and25 , not42 , and23 );
and #1 I26 ( OUT4 , Q3_in , and23 );
and #1 I27 ( and27 , not43 , and25 );
and #1 I28 ( OUT3 , Q2_in , and25 );
and #1 I29 ( OUT2 , Q1_in , and27 );
and #1 I30 ( and30 , not45 , and27 );
and #1 I31 ( and31 , and32 , Q6_in );
and #1 I32 ( and32 , and33 , Q5_in );
and #1 I33 ( and33 , and34 , Q4_in );
and #1 I34 ( and34 , and35 , Q3_in );
and #1 I35 ( and35 , and36 , Q2_in );
and #1 I36 ( and36 , and37 , Q1_in );
and #1 I37 ( and37 , COUNT , Q0_in );
not #1 I38 ( not38 , Q0_in );
not #1 I39 ( not39 , OUT8_in );
not #1 I40 ( not40 , Q5_in );
not #1 I41 ( not41 , Q4_in );
not #1 I42 ( not42 , Q3_in );
not #1 I43 ( not43 , Q2_in );
not #1 I44 ( not44 , Q6_in );
not #1 I45 ( not45 , Q1_in );
dtype #1 I46 ( Q0 , d46nq , CLOCK , nRESET , D0_in );
dtype #1 I47 ( OUT8 , d47nq , CLOCK , nRESET , D7 );
dtype #1 I48 ( Q6 , d48nq , CLOCK , nRESET , D6 );
dtype #1 I49 ( Q5 , d49nq , CLOCK , nRESET , D5 );
dtype #1 I50 ( Q4 , d50nq , CLOCK , nRESET , D4 );
dtype #1 I51 ( Q3 , d51nq , CLOCK , nRESET , D3 );
dtype #1 I52 ( Q2 , d52nq , CLOCK , nRESET , D2 );
dtype #1 I53 ( Q1 , d53nq , CLOCK , nRESET , D1 );
xor #1 I66 ( D1 , and37 , Q1_in );
xor #1 I67 ( D2 , and36 , Q2_in );
xor #1 I68 ( D3 , and35 , Q3_in );
xor #1 I69 ( D4 , and34 , Q4_in );
xor #1 I70 ( D5 , and33 , Q5_in );
xor #1 I71 ( D6 , and32 , Q6_in );
xor #1 I72 ( D7 , and31 , OUT8_in );
xor #1 I73 ( D0 , COUNT , Q0_in );

// assignments to reconnect broken links:

assign D0_in = D0;
assign Q1_in = Q1;
assign Q2_in = Q2;
assign Q3_in = Q3;
assign Q4_in = Q4;
assign Q5_in = Q5;
assign Q6_in = Q6;
assign OUT8_in = OUT8;
assign Q0_in = Q0;
```

Pinout

| | |
|---|---|
| 1 | Q2 |
| 2 | Q1 |
| 3 | Q0 |
| 4 | D0 |
| 5 | ---- |
| 6 | D0_in |
| 7 | COUNT |
| 8 | CLOCK |
| 9 | nRESET |
| 10 | Q0_in |
| 11 | Q1_in |
| 12 | Q2_in |
| 13 | Q3_in |
| 14 | GND |
| 15 | ---- |
| 16 | OUT0 |
| 17 | OUT1 |
| 18 | OUT2 |
| 19 | OUT3 |
| 20 | OUT4 |
| 21 | OUT5 |
| 22 | OUT6 |
| 23 | OUT7 |
| 24 | TESTQ |
| 25 | ---- |
| 26 | TESTnS |
| 27 | TESTnR |
| 28 | OUT8_in |
| 29 | Q6_in |
| 30 | Q5_in |
| 31 | Q4_in |
| 32 | InputPad19 |
| 33 | InputPad16 |
| 34 | VDD |
| 35 | ---- |
| 36 | OUT8 |
| 37 | Q6 |
| 38 | Q5 |
| 39 | Q4 |
| 40 | Q3 |

# Interim Report Section G

| | | |
|---|---|---|
| **Header: Simulation of Logarithmic Thingy (Layout)** | | |
| **User: Fred Bloggs** | | |
| **Date: Oct 2, 1999 00:37:22** | **Time Scale From: 0 To: 276950** | **Page: 1 of 1** |




------- Your design simulates OK! -------

# Interim Report Section H

## Design Submission Form for Team: *Z*

### Electronic Design Submission

☑ Design submitted OK

Submitted by (ecsid): ***fb399***

Date of submission: ***2/11/00***

☐ Design NOT submitted

We have discussed this with Iain McNally and have obtained his signature below:

I McNally

### Paper Deliverables

| | | |
|---|---|---|
| Interim report section A | ☑ | Text description of your design, no more than one side of A4. |
| Interim report section B | ☑ | Circuit diagram showing your design before the addition of testability. |
| Interim report section C | ☑ | Annotated circuit diagram showing exactly how your design is implemented. |
| Interim report section D | ☑ | CGA Template for your design (filled in). |
| Interim report section E | ☑ | Netlist for your design. |
| Interim report section F | ☑ | Pinout for your design. |
| Interim report section G | ☑ | Simulation results including a waveform plot. |
| Interim report section H | ☑ | This form. |

### Team Members

| | Name | % Effort (sums to 100) | Description of individual contribution | Signature |
|---|---|---|---|---|
| 1 | ***Fred Bloggs*** | ***48*** | ***Helped with schematic<br>Responsible for layout<br>Performed simulations*** | *F.Bloggs* |
| 2 | ***Jane Smith*** | ***48*** | ***Original design,<br>Responsible for schematic<br>Helped with layout*** | *Jane S. Smith* |
| 3 | ***Vincent Dummy*** | ***4*** | ***Didn't show up after introductory laboratory*** | |
| 4 | | | | |
| 5 | | | | |
| 6 | | | | |

***Please fill in all parts of this form.***

***Marks will be lost where deliverables are missing, late or not as specified.***

***In addition to the two submitted copies, it is strongly advised that each team member should have their own copy of this report for reference during the later stages of this design exercise.***