

Digital Simulations

Dr Basel Halak

Learning Outcomes



After completing this unit, you should be able to:

- To describe the different Sign-off stages in the digital design process
- To compile and simulate HDL models in Modelsim
- To perform different types of digital simulations

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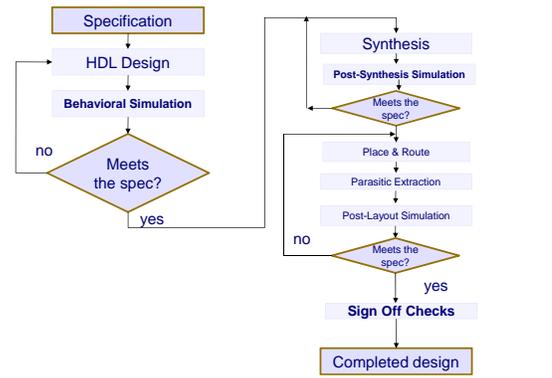


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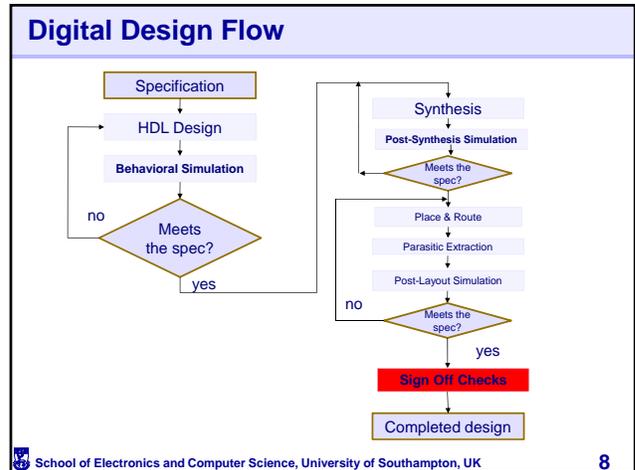
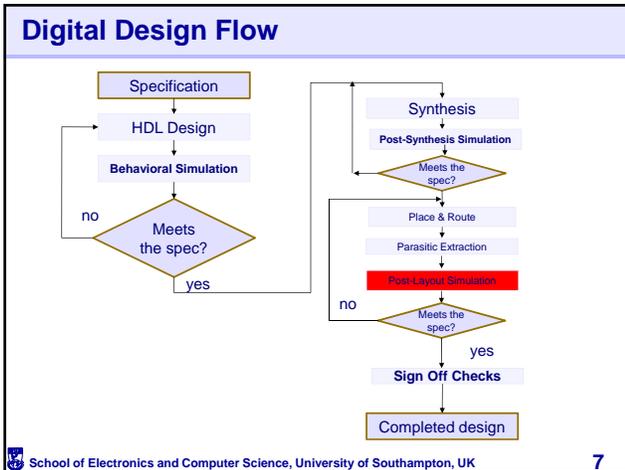
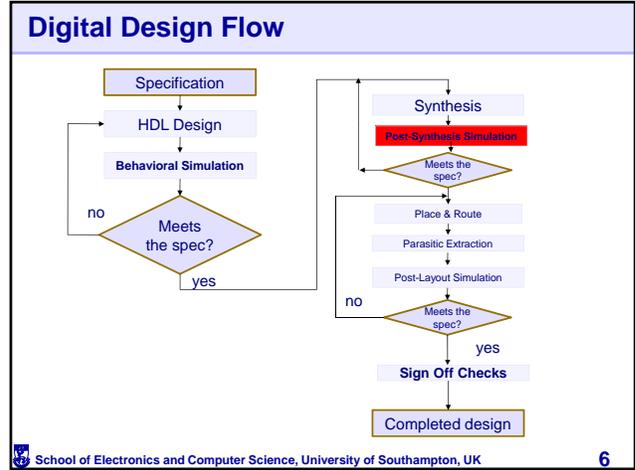
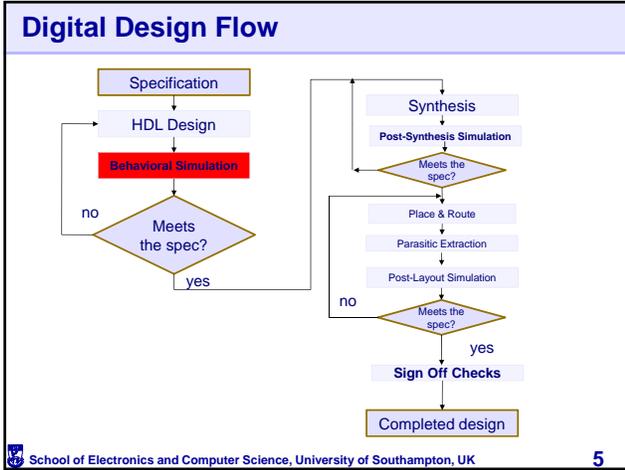
Digital Design Flow



```

    graph TD
      Spec[Specification] --> HDL[HDL Design]
      HDL --> Beh[Behavioral Simulation]
      Beh --> M1{Meets the spec?}
      M1 -- no --> HDL
      M1 -- yes --> Syn[Synthesis]
      Syn --> PostSyn[Post-Synthesis Simulation]
      PostSyn --> M2{Meets the spec?}
      M2 -- no --> Syn
      M2 -- yes --> PR[Place & Route]
      PR --> PE[Parasitic Extraction]
      PE --> PostLayout[Post-Layout Simulation]
      PostLayout --> M3{Meets the spec?}
      M3 -- no --> Syn
      M3 -- yes --> SignOff[Sign Off Checks]
      SignOff --> Comp[Completed design]
    
```

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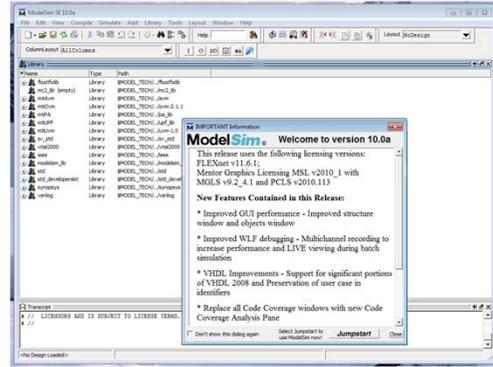
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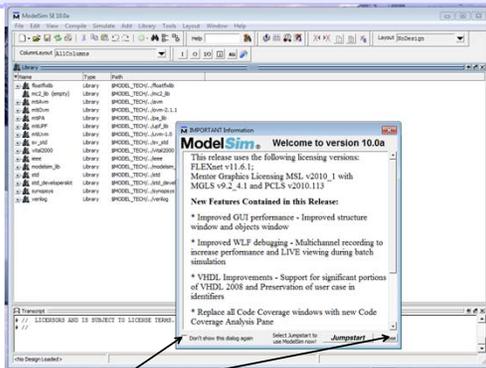
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Load Modelsim: CAD->Modelsim

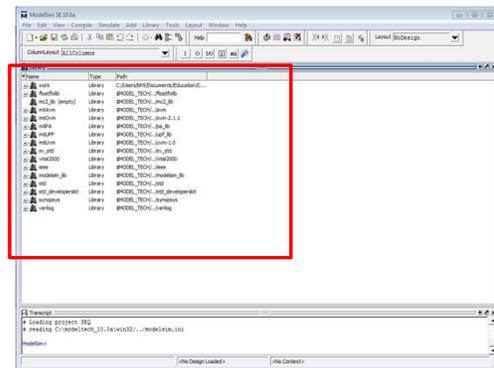


Load Modelsim: CAD->Modelsim



Click this and get rid of it

Libraries



Transcript -> commands

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Usual Windows Style menus

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Step 1 : Create a Project

- File -> New -> project

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Create the new directory

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Add the files

The 'Add Items to the Project' dialog box contains four options: 'Create New File', 'Add Existing File', 'Create Simulation', and 'Create New Folder'. An arrow points from 'Add Existing File' to the 'Add file to Project' dialog box. The 'Add file to Project' dialog box shows a 'File Name' field, a 'Browse...' button, 'Add file as type' (default), 'Folder' (Top Level), and radio buttons for 'Reference from current location' (selected) and 'Copy to project directory'.

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Add the files

- You can reference the files, or you can copy into the directory – this is a good idea if you are going to modify things

The 'Add file to Project' dialog box shows the 'Reference from current location' radio button selected, highlighted with a red box. The 'File Name' field contains 'H:/vhd/counter4bit/counter4bit.vhd'.

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Note the transcript & workspace...

The ModelSim SE 10.0a interface shows the workspace window with a list of files: 'topLevelCounter.vhd', 'topLevelCounter.vhd', and 'topLevelCounter7.vhd'. The transcript window at the bottom shows the command 'loading project: testproject.sim'. Both the workspace and transcript windows are highlighted with red boxes.

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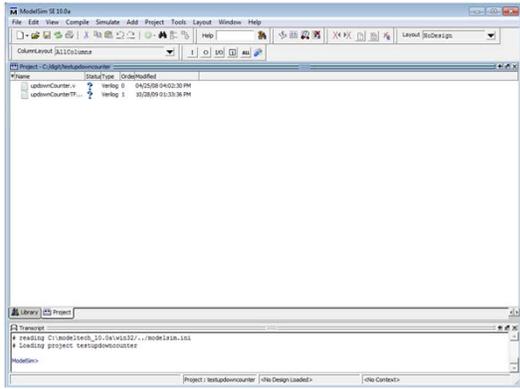
You can add more files

- File -> Add to project -> Existing Files

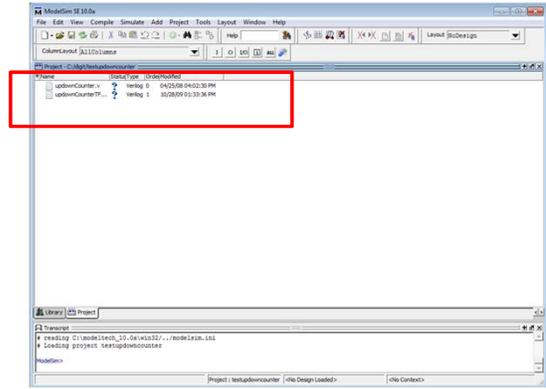
The 'Add file to Project' dialog box shows the 'File Name' field with 'H:/vhd/counter4bit/test.vhd'. The 'Reference from current location' radio button is selected.

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Now we have the complete project



Note the status and type

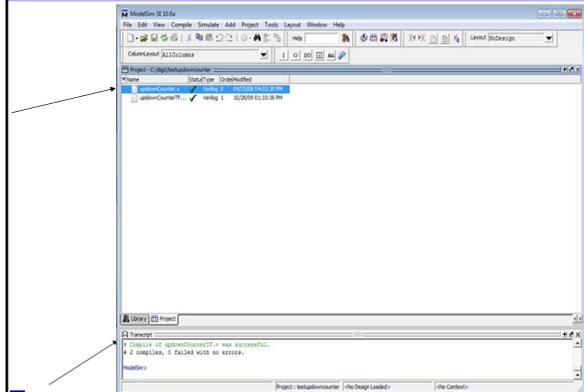


What Now – Compile

- We can compile individual files
 - Useful for large designs
- We can compile ALL the Verilog files
 - What we usually do when all the individual files have been checked
- Compile -> Compile All (from the menus)
 - Or use the menu bar icon

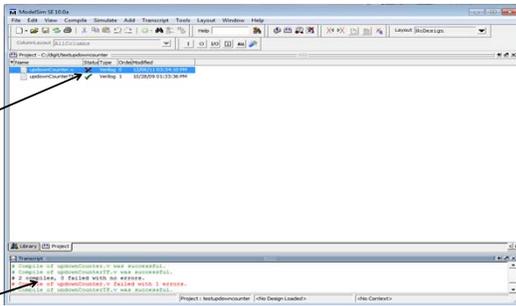


Compile Status



What if it goes wrong?

- E.g. syntax error



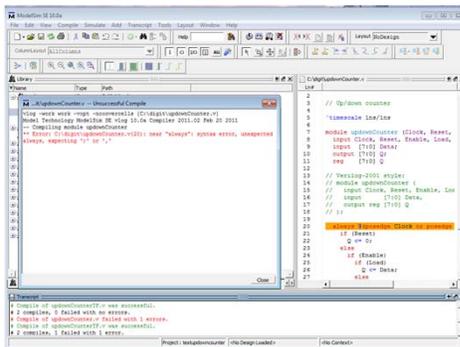
Edit a Verilog File

- Right click on the Verilog file and choose Edit from the pop up menu to bring up the editor
- Double click on the error in the transcript to see where the error is...

Double Click Again

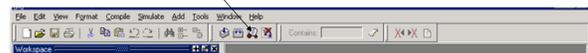


Debug the model

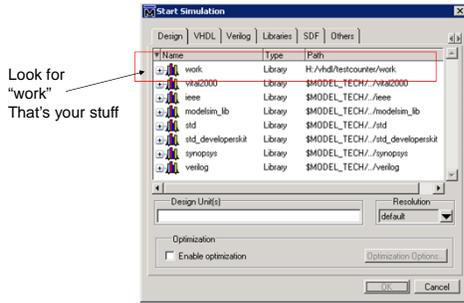


Simulate

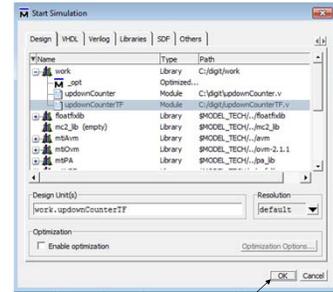
- Simulate -> Start Simulation
- Or click on the icon:



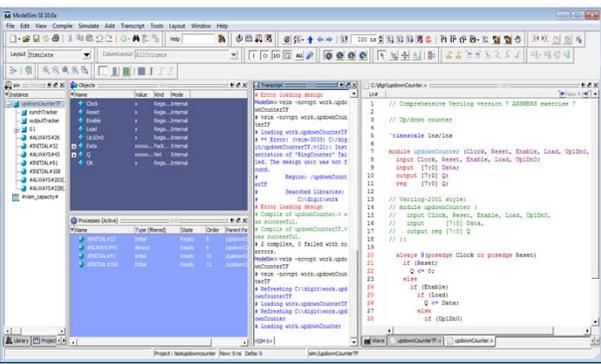
List of compiled Units



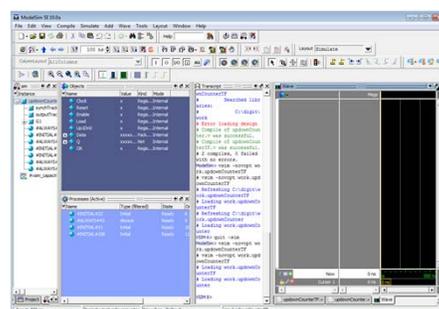
Choose the test circuit



The Design loads up...



Get wave viewer



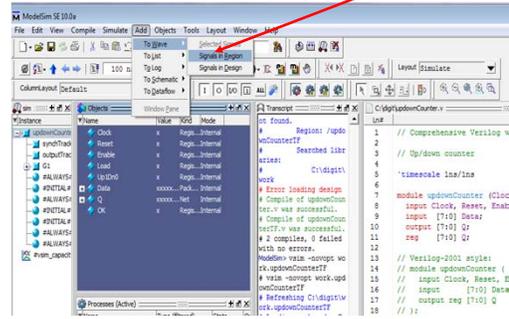
Waveform Window



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33

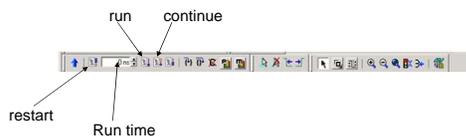
Add Signals to the waveform window



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34

Run Commands

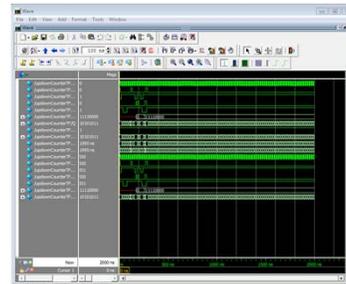


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35

Run a 50 us simulation

- Type the following command:
 - Run 2 us



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36

Learning Outcomes



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Types of Digital Simulations

■ Behavioural Simulations:

- It is used to check the functionality of the design **before synthesis**
- You will need the following files:
 1. HDL description of your design
 2. A test bench

Types of Digital Simulations

■ Behavioural gate level simulation

- It is a **post-synthesis simulation**
- **You will need :**
 1. HDL description of the synthesized design
 2. HDL models of all cells in your design (e.g. Verilog models), and
 3. A test bench

▪ **How to perform Behavioural gate level simulation**

Copy all the required files into your simulation directory and follow the same procedure for behavioural simulation.

Types of Digital Simulations

■ Behavioural gate level simulation with SDF timing

- It is a **post-synthesis simulation**
- **You will need:**
 1. HDL description of the synthesized design
 2. SDF (standard delay format) file (which can be obtained for the synthesis tool and from the layout tool)
 3. HDL models of all cells in your design (e.g. Verilog models), these models should contain specify blocks in their behavioural view that have delay information
 4. A test bench

Note: you can generate SDF files in Design Compiler using this command:

write_sdf filename.sdf

Types of Digital Simulations

How to do Behavioural gate level simulation with SDF timing

- Copy all the required files into your simulation directory
- Edit the HDL description of the synthesised design by adding the following statement:
initial \$sdf_annotate ("filename.sdf") as shown in figure 1
- Save changes to your HDL
- Follow the same procedure for behavioural simulations

```

module aka ( Clock, A, B, Op, F, Cout, Equal )
input [7:0] A;
input [7:0] B;
input [3:0] Op;
output [7:0] F;
input Clock;
output Cout, Equal;
wire M02, M03, M04, M05, M06, M07, M08, M09, M10, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, M21, M22, M23, M24, M25, M26, M27, M28, M29, M30, M31, M32, M33, M34, M35, M36, M37, M38, M39, M40, M41, M42, M43, M44, M45, M46, M47, M48, M49, M50, M51, M52, M53, M54, M55, M56, M57, M58, M59, M60, M61, M62, M63, M64, M65, M66, M67, M68, M69, M70, M71, M72, M73, M74, M75, M76, M77, M78, M79, M80, M81, M82, M83, M84, M85, M86, M87, M88, M89, M90, M91, M92;
wire [7:0] Temp;
initial $sdf_annotate ("design.sdf");

DF1 F_reg_7 (.D(Temp[7]), .C(Clock), .Q(F[7])) ;
DF1 F_reg_6 (.D(Temp[6]), .C(Clock), .Q(F[6])) ;
DF1 F_reg_5 (.D(Temp[5]), .C(Clock), .Q(F[5])) ;
DF1 F_reg_4 (.D(Temp[4]), .C(Clock), .Q(F[4])) ;
DF1 F_reg_3 (.D(Temp[3]), .C(Clock), .Q(F[3])) ;
DF1 F_reg_2 (.D(Temp[2]), .C(Clock), .Q(F[2])) ;
DF1 F_reg_1 (.D(Temp[1]), .C(Clock), .Q(F[1])) ;
DF1 F_reg_0 (.D(Temp[0]), .C(Clock), .Q(F[0])) ;

```

Figure 1

Types of Digital Simulations

Why use SDF file?

```

(CELL
(CELLTYPE "NOR40")
(INSTANCE U214)
(Delay
ABSTRACT
(OPATH A Q (0.310;0.311;0.311) (0.401;0.401;0.401))
(OPATH B Q (0.287;0.288;0.288) (0.255;0.255;0.255))
(OPATH C Q (0.260;0.262;0.262) (0.269;0.270;0.270))
(OPATH D Q (0.294;0.293;0.293) (0.224;0.243;0.243))
)
)
SDF delay information for an Instance of the NOR40 cell

```

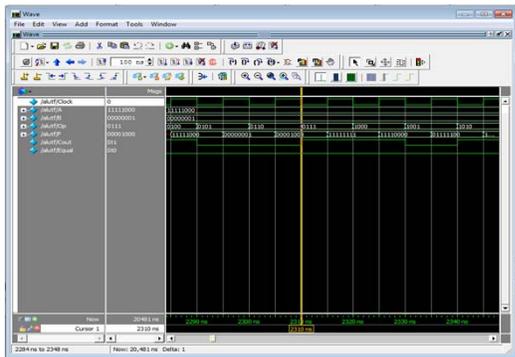
```

module NOR40 (A,B,C,D,Q):
output Q;
input A,B,C,D;
nor (Q,D,C,B,A);
`ifdef functional
`else
specify
(A => Q) = (1,1);
(B => Q) = (1,1);
(C => Q) = (1,1);
(D => Q) = (1,1);
endspecify
`endif
endmodule

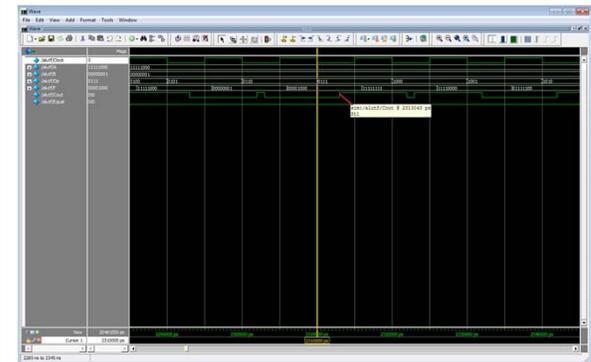
```

Behavioural Verilog Code for NOR40

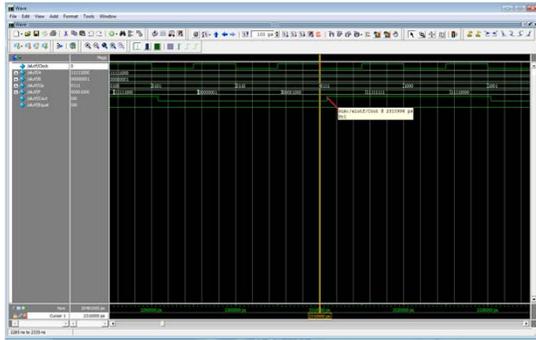
Behavioural Simulations



Behavioural Gate Level Simulation



Behavioural Gate Level Simulation with SDF timing



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45

Digital Simulation Lab Instructions

For this lab you will need:

For Behavioural simulation

1. HDL model of the design (qmults.v)
2. A test bench (test.v)

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46

SOC Encounter Lab Instructions

For this lab you will need:

For post Synthesis simulation

1. A synthesised Verilog net list of the design (this is obtained from the synthesis stage)
2. A test bench
3. Your timing constraints file "design.sdf" (this is obtained from the synthesis stage)
4. HDL models of all cells in technology library

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47

SOC Encounter Lab Instructions

For this lab you will need:

For post Layout simulation

1. Post layout netlist (this is obtained from the layout stage)
2. A test bench
3. Your timing constraints file "design.sdf" (this is obtained from the layout stage)
4. HDL models of all cells in technology library

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48

Behavioural Simulations

1. Create a working directory called BehaviouralSim.
2. Save the qmults HDL file and the test bench in this folder.
3. Open the test bench in a text editor and investigate it.
4. Set the clock period in the test to 2 ns.
5. Create a Modelsim Project.
6. Compile all files.
7. Run the simulations and verify the design function correctly.
8. Does the design simulate correctly if you reduce clock period to 0.5 ns? Why?.
9. Save a printout of your simulations.

Post Synthesis Simulations

1. Create a working directory called PostSynSim.
2. Save the qmults HDL file, the test bench, HDL models of the technology library and SDF timing file in this folder.
3. Open the test bench in a text editor and set the clock frequency in the test to your maximum achievable frequency (from the synthesis stage).
4. Open the SDF file in a text editor and comment out all lines that begin with the word "Removal".
5. Create a second Modelsim Project.
6. Compile all files.
7. Run the simulations and verify the design function correctly.
8. Does the design simulate correctly if you reduce clock period to 0.5 ns? Why?
9. Save a printout of your simulations.

Post Layout Simulations

1. Create a working directory called PostLaySim
2. Save the qmults HDL file, the test bench, HDL models of the technology library and SDF timing file in this folder.
3. Open the test bench in a text editor and set the clock frequency in the test to your maximum achievable frequency (from the synthesis stage).
4. Open the SDF file in a text editor and comment out all lines that begin with the word "Removal"
5. Create a third Modelsim Project
6. Compile all files
7. Run the simulations and verify the design function correctly.
8. Does the design simulate correctly if you reduce clock period to 0.5 ns? Why?
9. Save a printout of your simulations