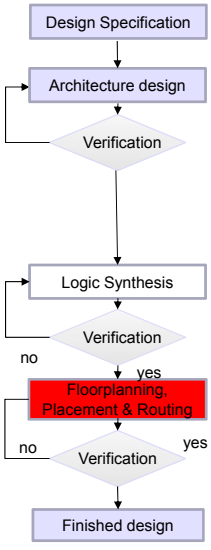
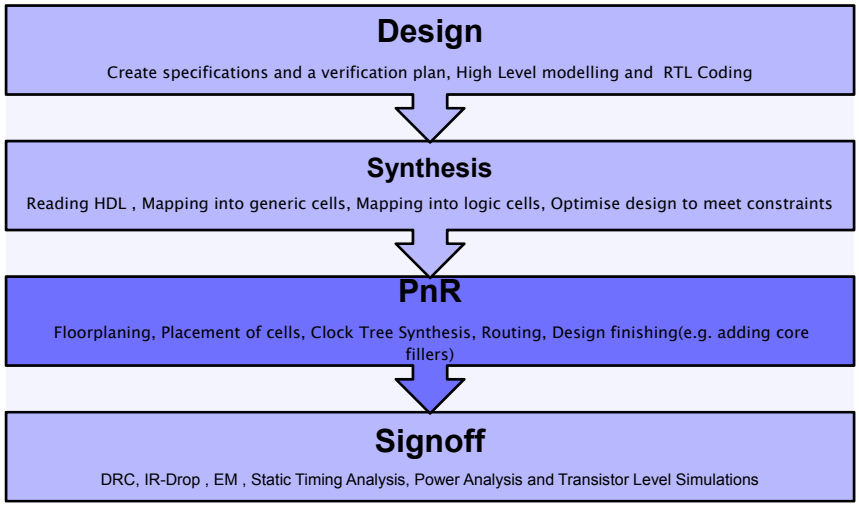
Cadence SoC Encounter – with AMS c35

Dr Basel Halak

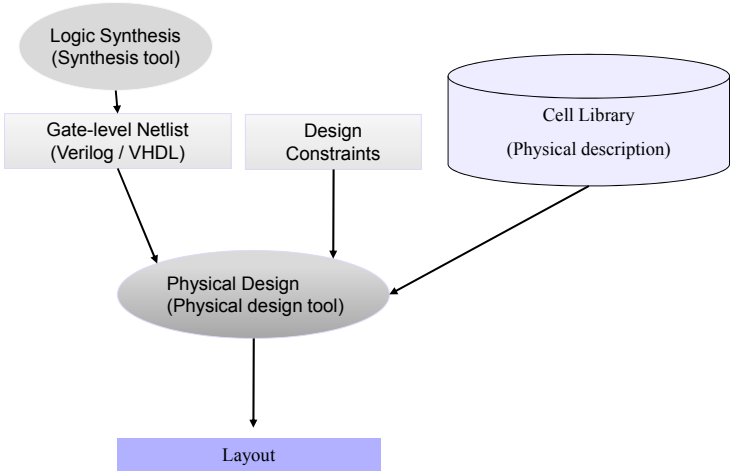
Digital Design Flow



Design Stage



Digital IC Design Flow: Place&Route



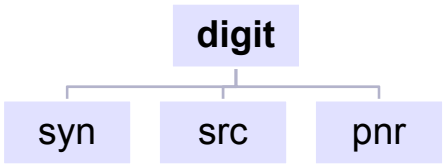
SOC Encounter Lab Instructions

For this lab you will need:

1. A synthesised Verilog net list of the design (this is obtained from the synthesis stage)
2. Your timing constraints file "design.sdc" (this is obtained from the synthesis stage)
3. Configuration file (design.conf) this is provided
4. MMMC (Multi-Mode Multi-Corner) view definition file (design.view) this is provided

Design Directory Management

1. Inside your design directory create a sub-directory called pnr
2. Copy the design files into pnr

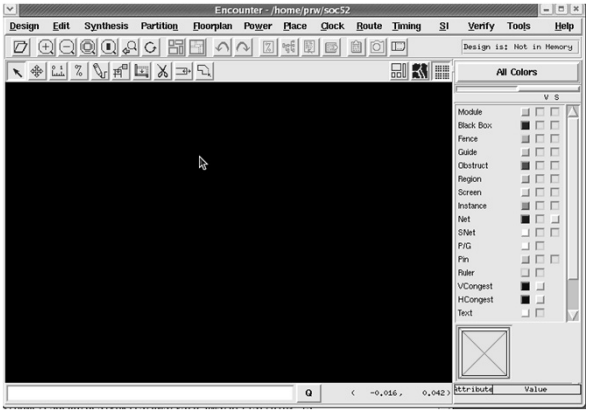


Introduction

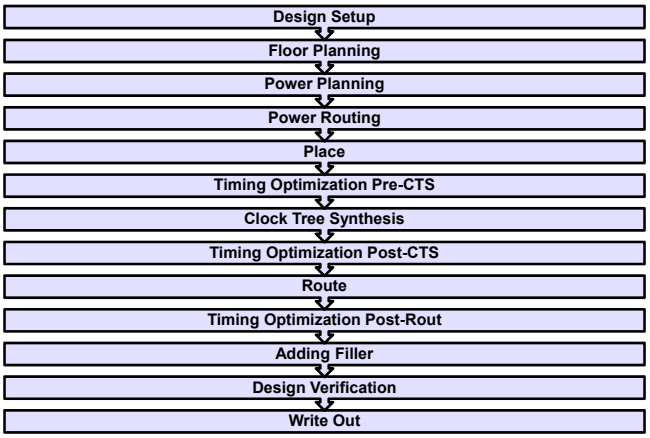
- The place and Route software within the Cadence software is called “velocity”
- To be able to run this software you need to first set up your directory for the required AMS c35 design files
- In this work, the environment has been setup to run “velocity” properly. So you don’t actually need to do anything by yourself

Running encounter

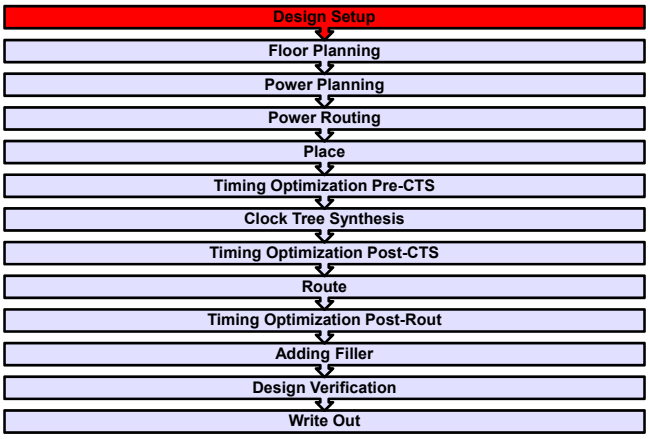
- Simply type “velocity” at a command prompt and the basic encounter GUI with appear:



Stages of the lab

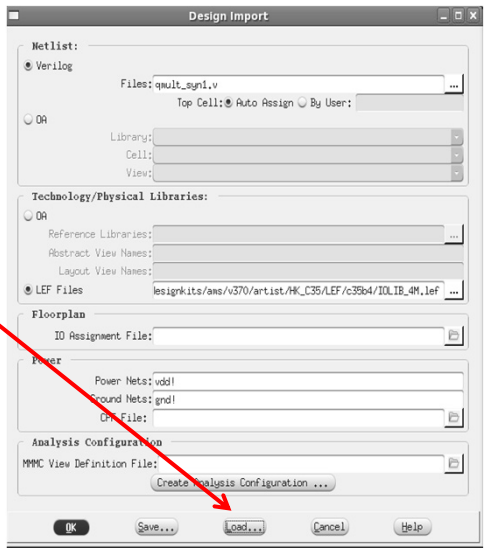


P&R Process



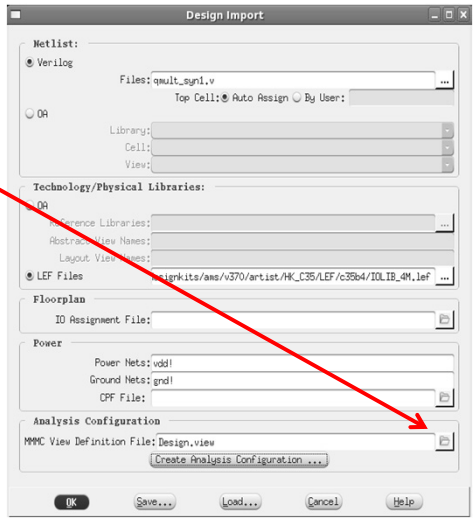
Import the Design

- **Choose Design – import Design to open the form**
- Load up the configuration file (design.conf).



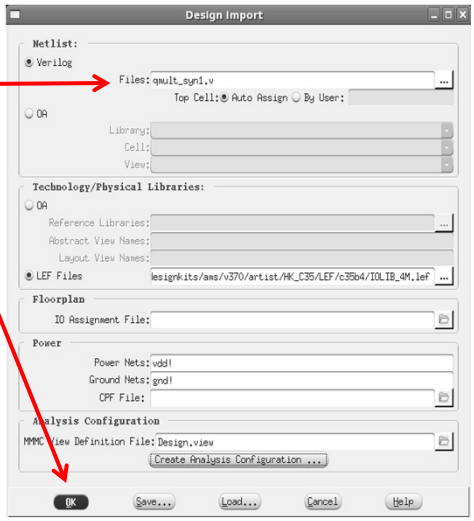
Import the Design

- Load up MMMC definition view file (design.view).



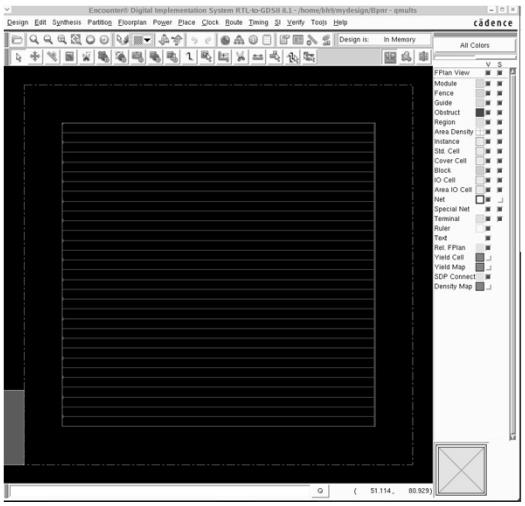
Import the Design

- Change the name of the verilog net list to match your own).
- Then click ok, this will setup your libraries and read in all the relevant cell definitions and calculate the initial floor plan

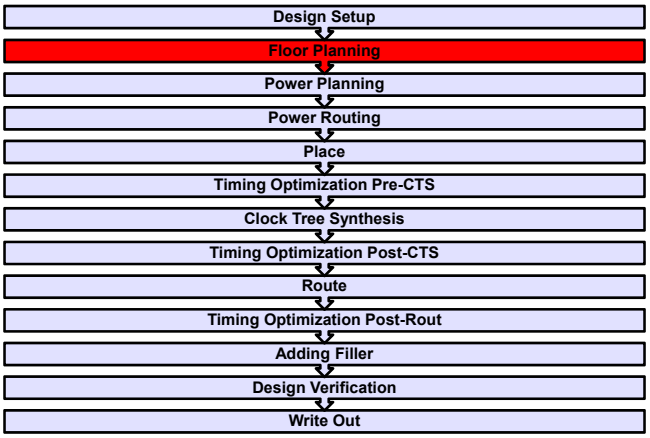


Design Prepped

- **Note the design is ready for placement…**



P&R Process

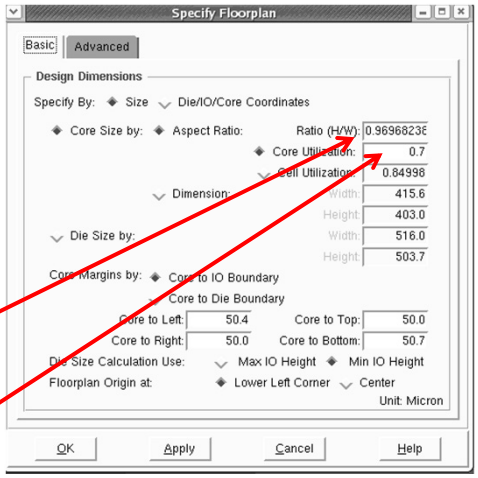


Floorplanning

- Can specify details of the floor plan

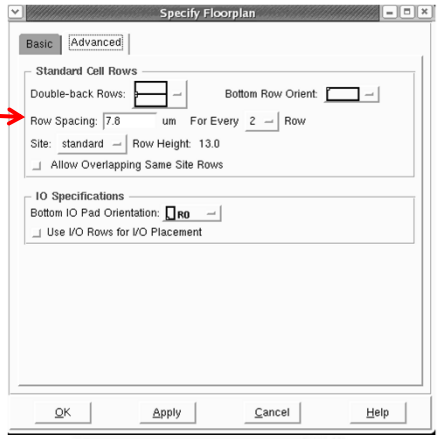
Floorplan -> Specify Floorplan

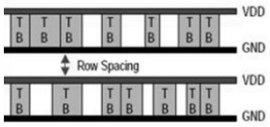
- The CORE is the part of the design containing the cells, and the periphery is for all the IO and power rings
- Select the core size as follows(notice the core dimensions)
- Set the core utilization to 0.7 to allow room for routing



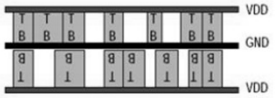
Floorplanning

- **Set the advanced option as shown here**
- **Note that row spacing is set here to 7.8 to facilitate routing**





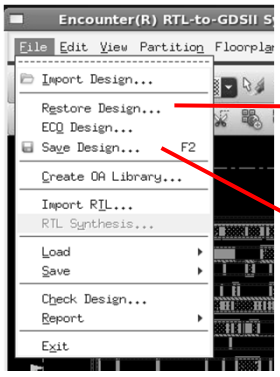
Non Abutted Rows



Abutted and Flipped Rows

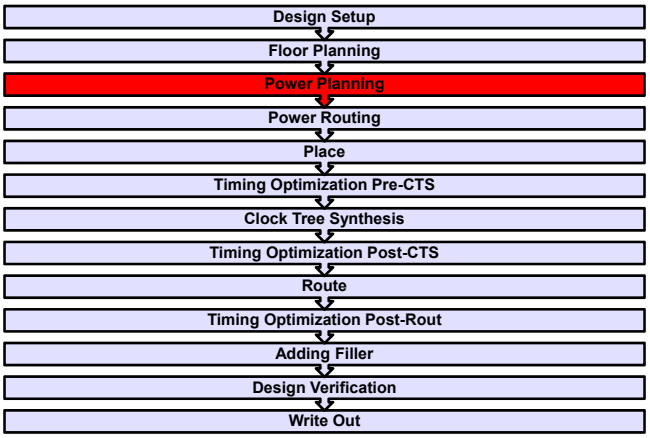
Save the Design

To save/restore the design:



Choose Data Type as Encounter

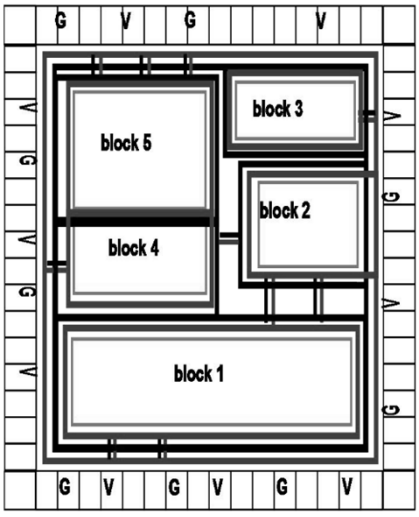
P&R Process



Power Planning

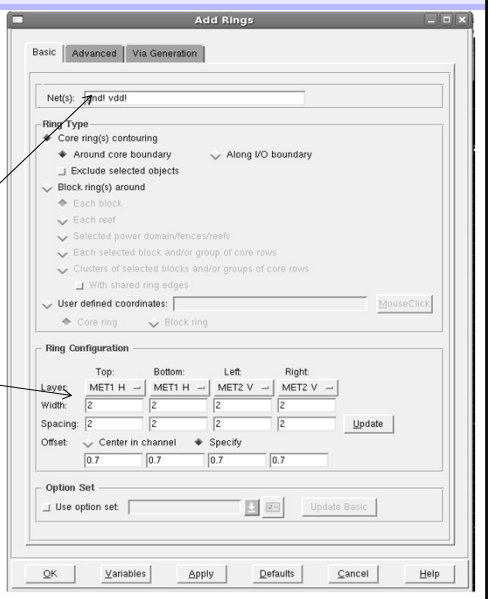
During Power Planning:

You define the global wire and grounds nets and create the power structures that corresponds to the global nets

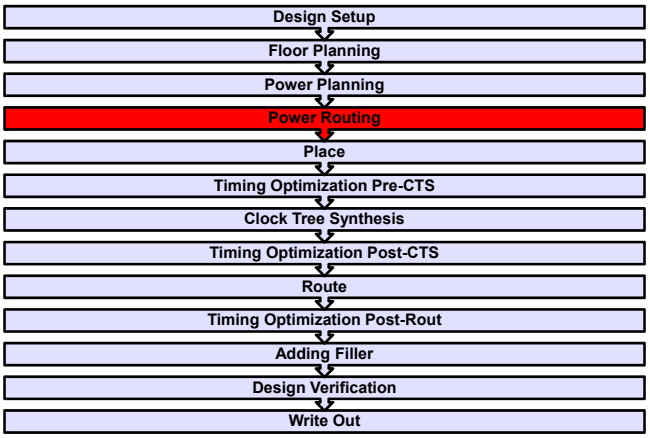


Power and Ground Rings

- You can automatically add power and ground rings around the design using **Power >Power Planning > Add Rings**
- Specify the names of the power and ground connections
- From here you can change the layer and dimensions of power and grounds rings
- **Click ok, this will add a ring for power and ground around the design**

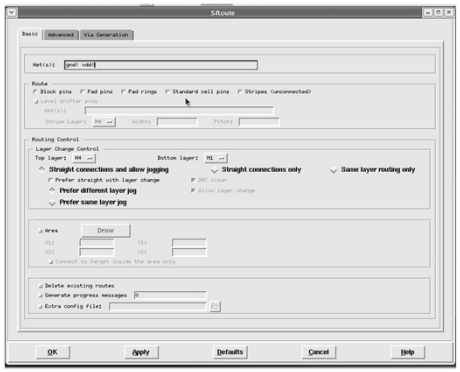


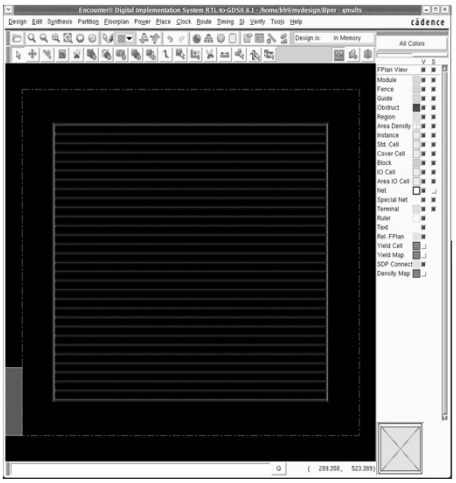
P&R Process



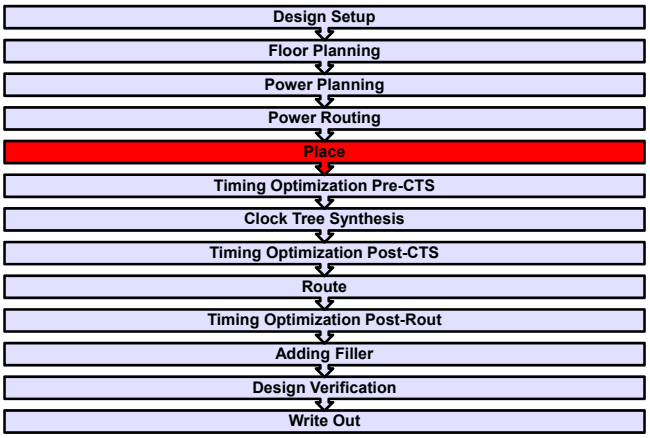
Connect Power and Ground to Core

- To connect to the core you need to complete a route -> special route:



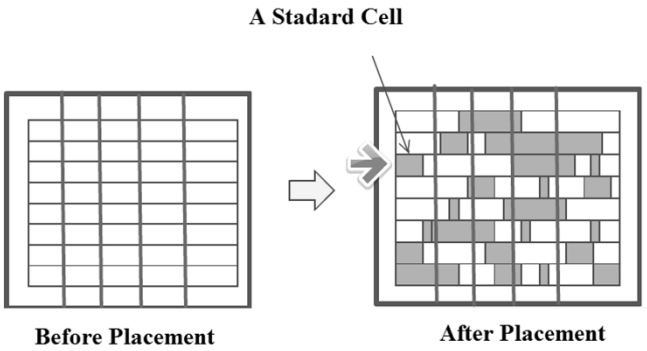


P&R Process



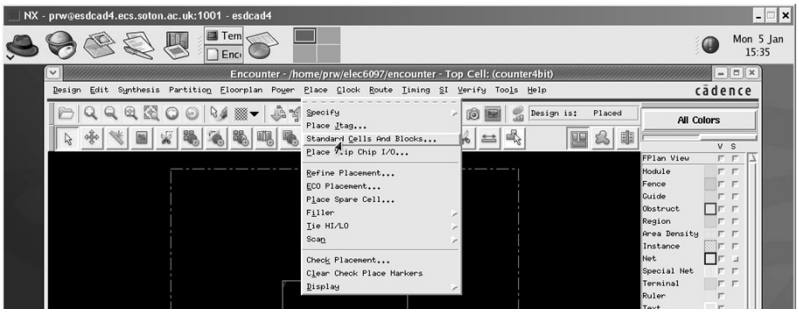
Placement

Placement is the process of placing the standard cells and blocks into the floor planned design



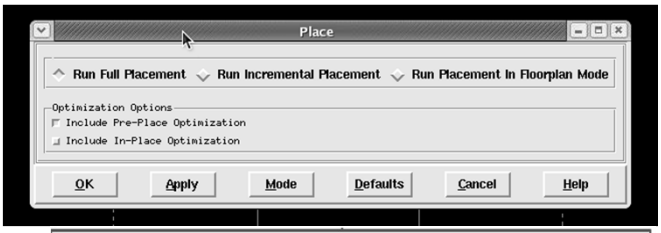
Placement

- **This is simply to show the quickest place and route approach (Place >> Standard Cells)**



Placement

- **Choose the full placement – on a simple design it won't take very long at all to complete**



Include Pre-Place Optimization

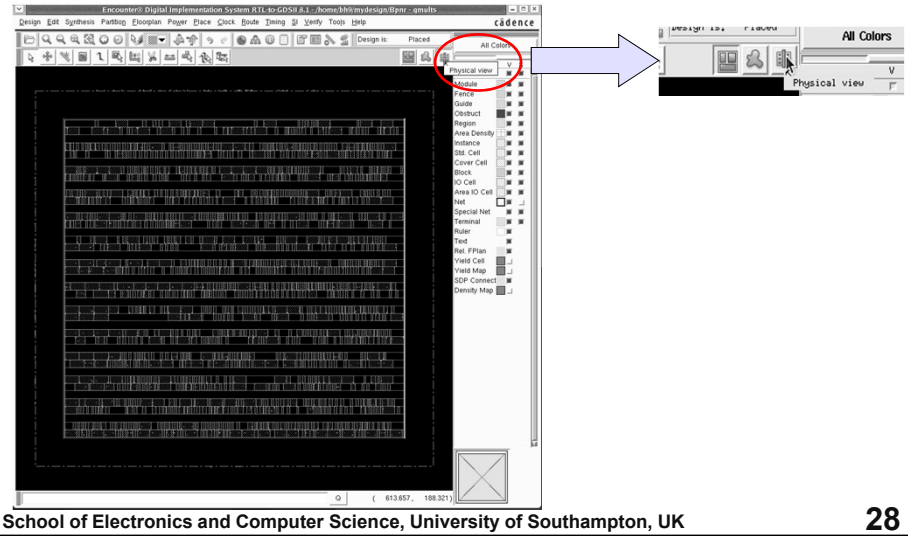
Runs optimization on the netlist before placing the cells.

Include In-Place Optimization

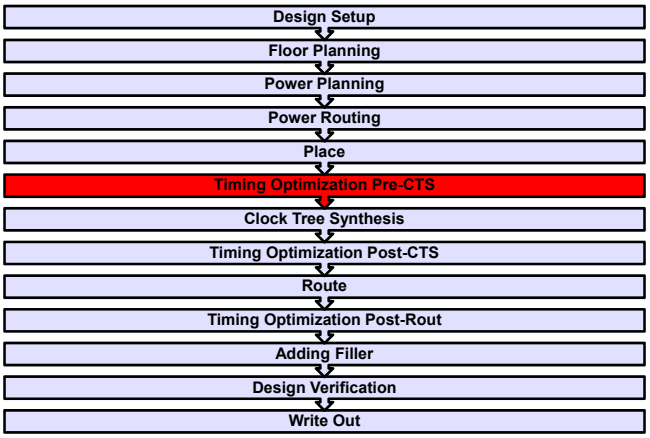
Runs optimization on the netlist to better meet timing constraints.

Placement

- **Then select the physical view option to see the placed cells**



P&R Process

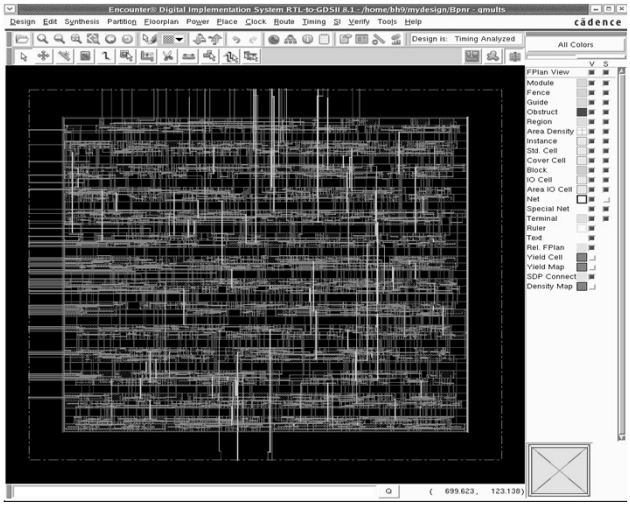


Timing Optimization

- **Select : Optimize > Optimize Design**
- **In the dialog box select Pre-CTS**
- **Select the type of Optimization**
- **Click ok**

Note that you need to perform Timing Optimization at different design stages

Timing Optimization Pre-CTS: Trial Rout



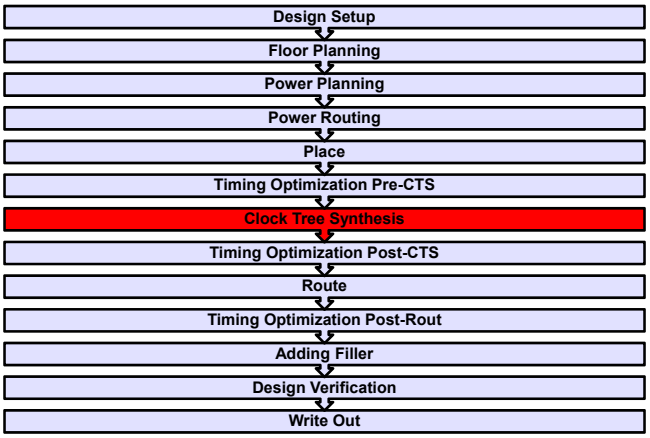
Timing Optimization

- You will get a summary of the optimization,
- Figure 1 show is an extract for that report that shows that setup timing constraints are met

```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

+--------------------+--------+--------+--------+---------+---------+---------+
|     Setup mode     |   all  | reg2reg | in2reg | reg2out | in2out  | clkgate |
+--------------------+--------+--------+--------+---------+---------+---------+
|           WNS (ns):| 0.102  | 0.102  | 1.006  |   N/A   |   N/A   |   N/A   |
|           TNS (ns):| 0.000  | 0.000  | 0.000  |   N/A   |   N/A   |   N/A   |
|    Violating Paths:|   0    |   0    |   0    |   N/A   |   N/A   |   N/A   |
|          All Paths:|  229   |  193   |  227   |   N/A   |   N/A   |   N/A   |
+--------------------+--------+--------+--------+---------+---------+---------+
```

Figure 1

P&R Process



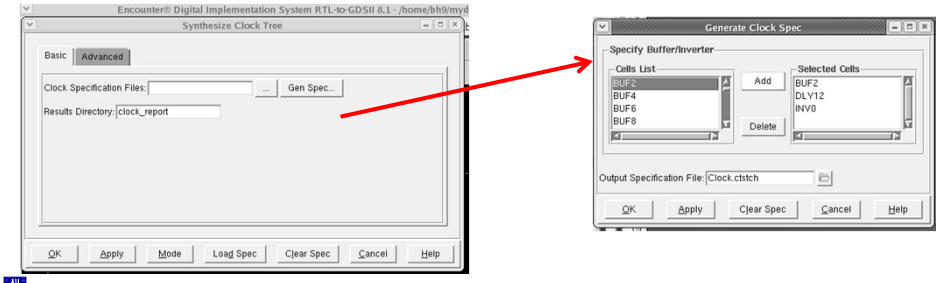
Clock Tree Synthesis

- Set clock tree synthesis mode by typing the following command:

  setCTSMode -engine ck

Clock Tree Synthesis

1. Select **Clock > Synthesize Clock Tree**
2. Click on **Gen Spec** button to create a clock specification file
3. Choose from the **Cells List** the name of the cell you want to use during timing optimization
4. Click ok in **Generate Clock Spec form** to generate a file called Clock.ctstch that contains that clock specification
5. Click ok in **Synthesize Clock Tree** form to synthesize the clock
6. You can clear these specs from the clear spec Tab



Clock Tree Synthesis

- To see the clock tree select Clock > Display > Display Clock Tree
- In the dialog box select the options as shown in figure one and click ok
- You should see the clock tree in a white colour as in figure 2

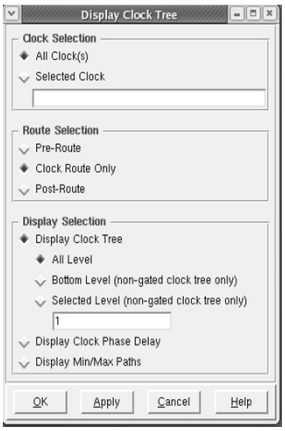


Figure 1

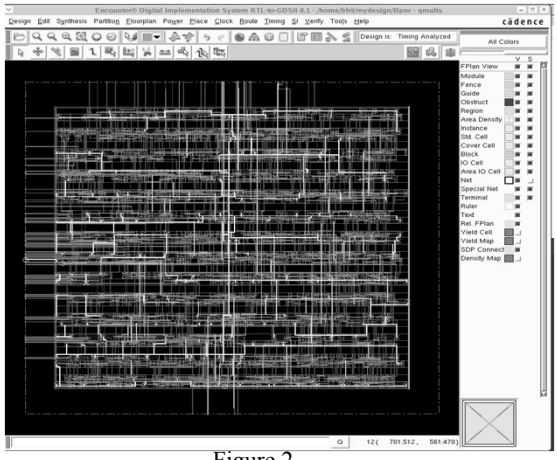
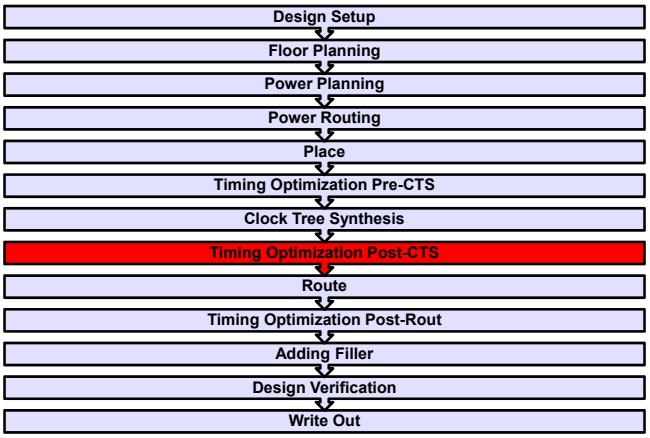


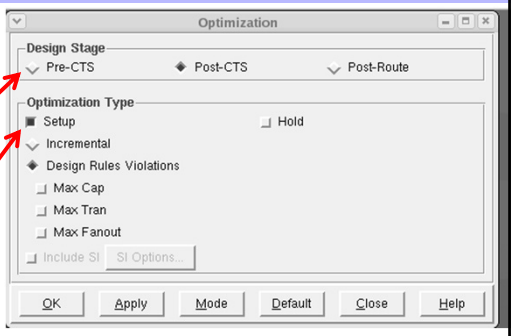
Figure 2

P&R Process



Timing Optimization

- Select : Optimize > Optimize Design
- In the dialog box select Post-CTS
- Select the type of Optimization
- Click ok



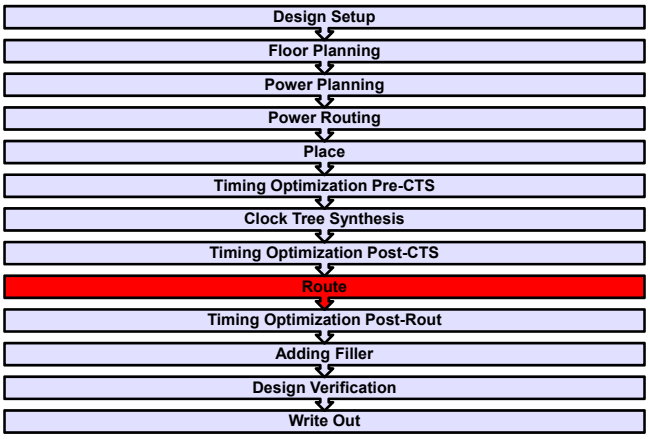
Timing Optimization

- You will get a summary of the optimization,
- Figure 1 show is an extract for that report that shows that setup timing constraints are met

Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.101	0.101	1.524	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	229	193	227	N/A	N/A	N/A

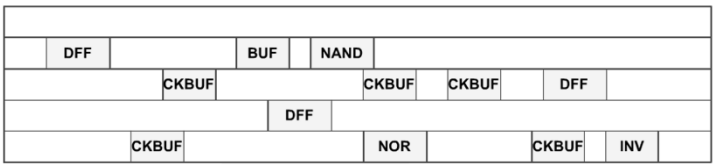
Figure 1

P&R Process

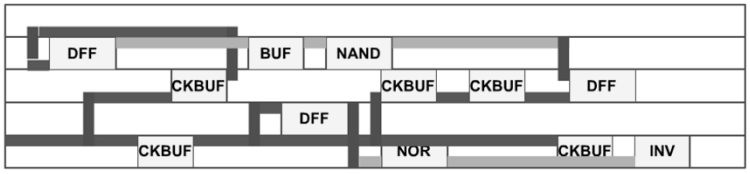


Routing

- **Routing is the step where the placed cells are connected with metal lines in a similar fashion to the Verilog netlist**



Before Routing



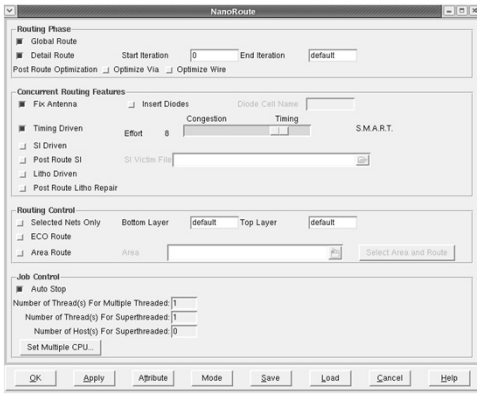
After Routing

Routing

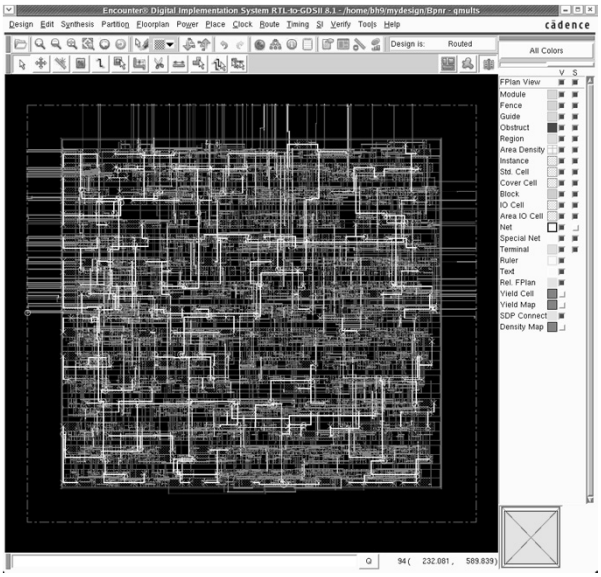
- **After the cells have been powered up, then final routing can take place**

Route > NanoRoute > Route

- **You select Timing driven so that the router will try and meet your timing constraints**
- **After it finishes you should see 0 violations and 0 fails in the shell window**



Design View after Routing



P&R Process

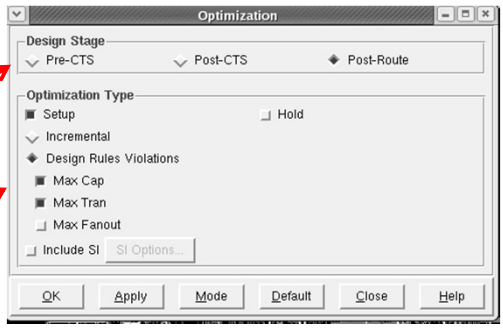
- Design Setup
- Floor Planning
- Power Planning
- Power Routing
- Place
- Timing Optimization Pre-CTS
- Clock Tree Synthesis
- Timing Optimization Post-CTS
- Route
- Timing Optimization Post-Rout
- Adding Filler
- Design Verification
- Write Out

Timing Optimization

- Disable Signal Integrity Analysis by using following command, since you don't need to concern about On-Chip-Variation:

  setDelayCalMode –engine aae –SIAware false

- **Select : Optimize > Optimize Design**
- **In the dialog box select Post-Rout**
- **Select the type of Optimization**
- **Click ok**



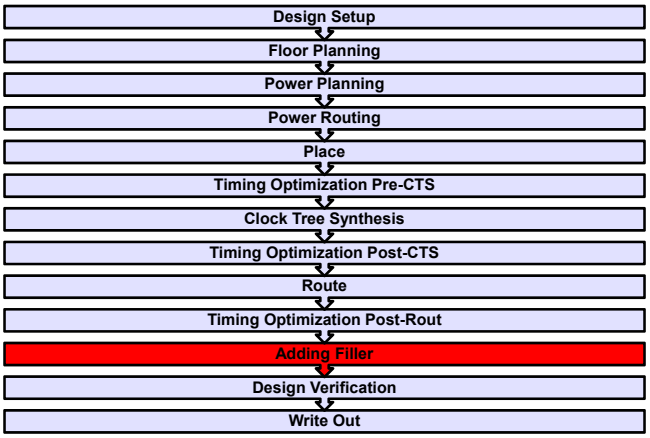
Timing Optimization

- You will get a summary of the optimization,
- Figure 1 show is an extract for that report that shows that setup timing constraints are met

Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.015	0.015	4.459	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	229	193	227	N/A	N/A	N/A

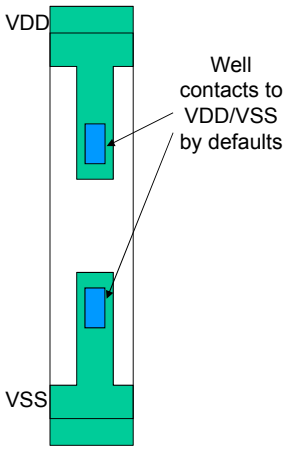
Figure 1

P&R Process



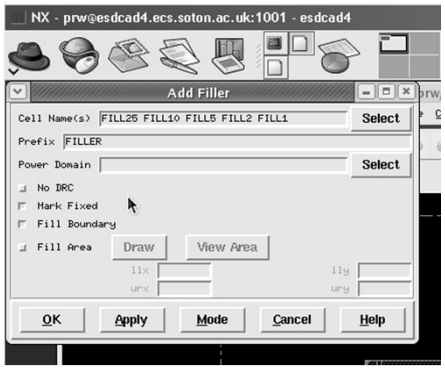
Filler Cells

- You can see gaps between the cells and these need to be filled using filler cells.
- These cells are simply standard power and ground router cells to connect the VDD, GND and nwells together
- Place >> Physical Cells >> Add Filler



Filler Cells

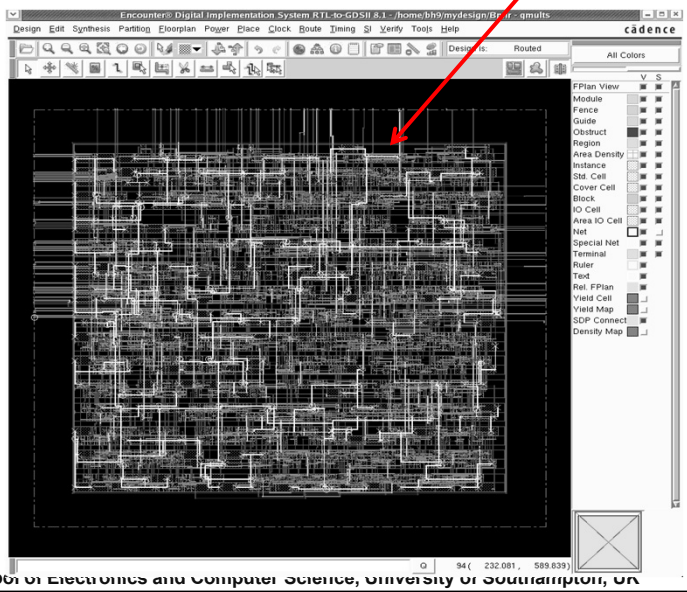
- **Select the filler cells from the list as shown**



...

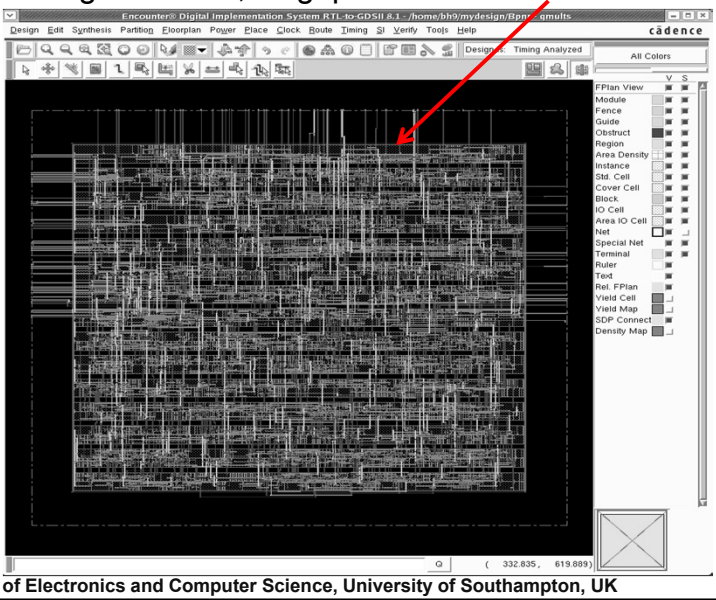
Filler Cells

Example: There is a gap in here

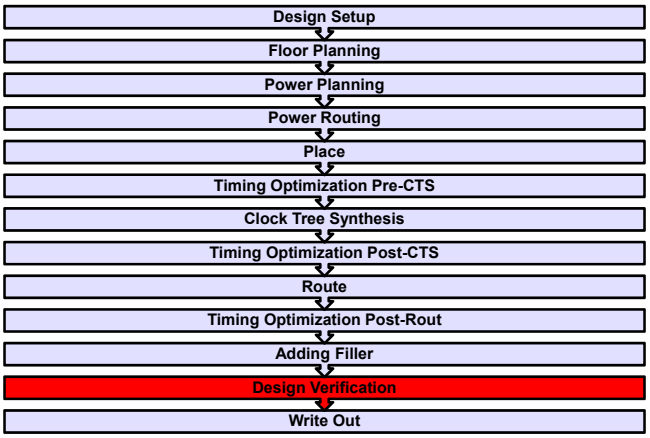


Filler Cells

After adding filler cells, all gaps will be filled



P&R Process



Verification of the Design

- **Choose Verify – Verify Connectivity to open the form and leave the default settings**
  - This form allows to detect conditions such as opens, unconnected wires, unconnected pins, loops, partial routing, and unrouted nets.
  - You will get a summary of this verification in the shell window (you should have no violations or fails)

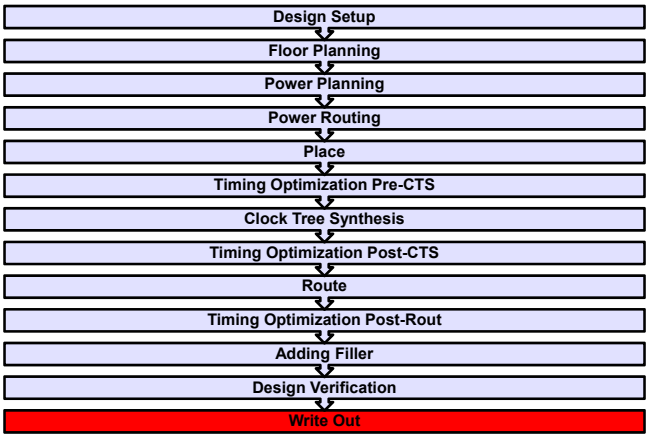
```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Wed Jul  9 17:19:06 2014

Design Name: qmults
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (643.5750, 599.9000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Wed Jul  9 17:19:06 2014
******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
```


Verification of the Design

- **Choose Verify – Verify Geometry to open the form and leave the default settings**
  - This form allows to check the physical layout of the design for DRC violations.
  - You will get a summary of this verification in the shell window (you should have no violations or fails)

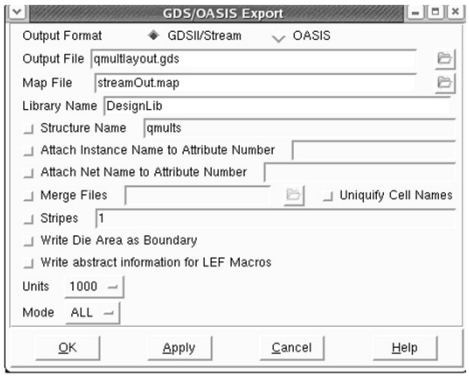
```
Velocity 1>  *** Starting Verify Geometry (MEM: 293.1) ***

  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 5600
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 2.00

Verification Complete : 0 Viols.  0 Wrngs.
```

P&R Process



Export out GDS

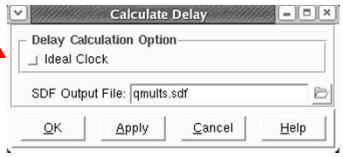
- We can export the GDSII by selecting File -> Save -> GDS/OASIS and choose the GDSII option



Export Structural Verilog and SDF files

- **For Verilog**: select **File > Save > Netlist**
- **To Export SDF file**:

1. Extract RC delay: select **Timing > Extract RC** to extract RC timings of interconnects
2. Generate SDF file: select **Timing > Write SDF** and click ok



Discussion points

1. What are the main advantages of automated place and route as opposed to manual layout
2. Assuming you have a hard IP core, at which stage of the place and route flow you should integrate it.
3. What can you do of the routing fails?
4. What should you do if you have timing violations after placement?
5. What will you do if the design is too large to be handled by the place and route tool?