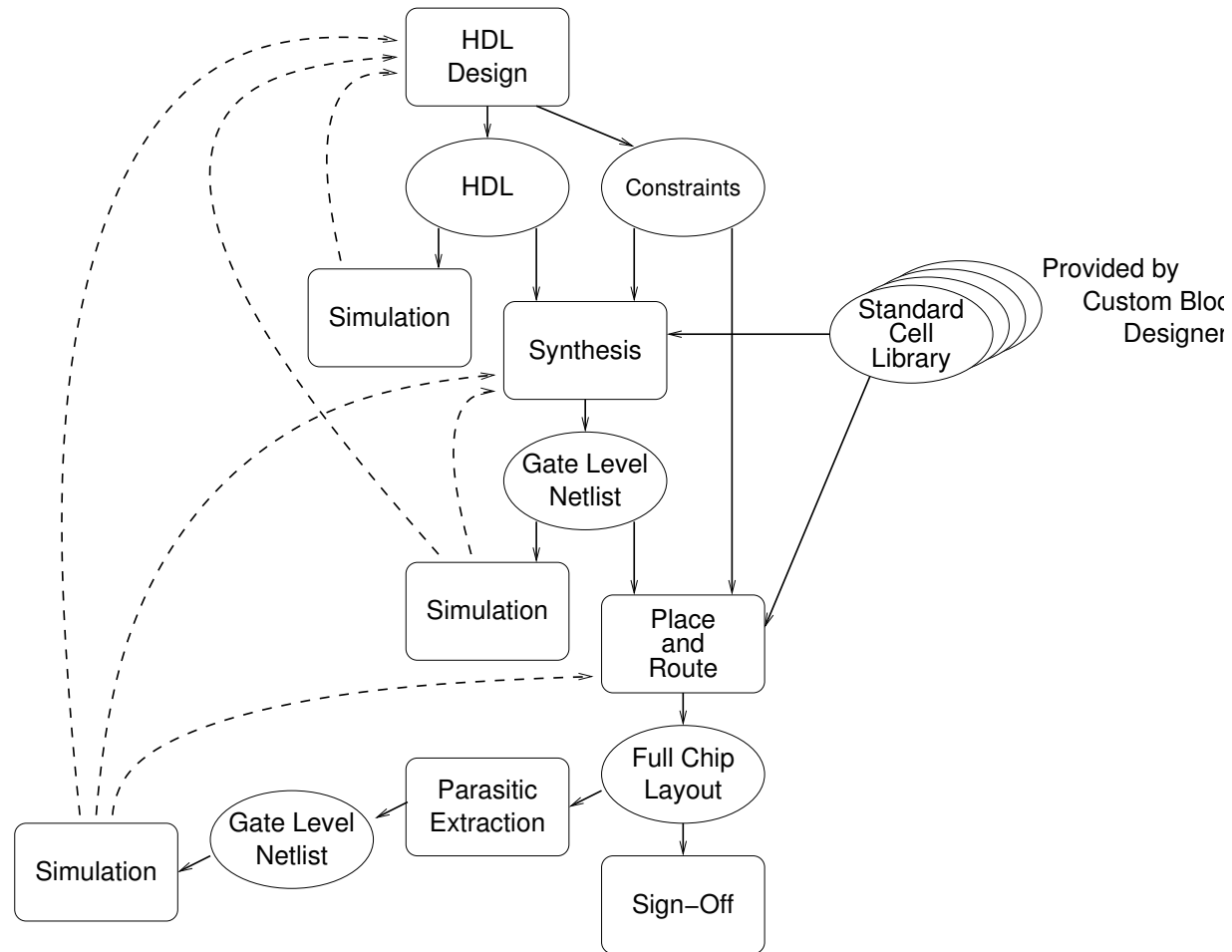


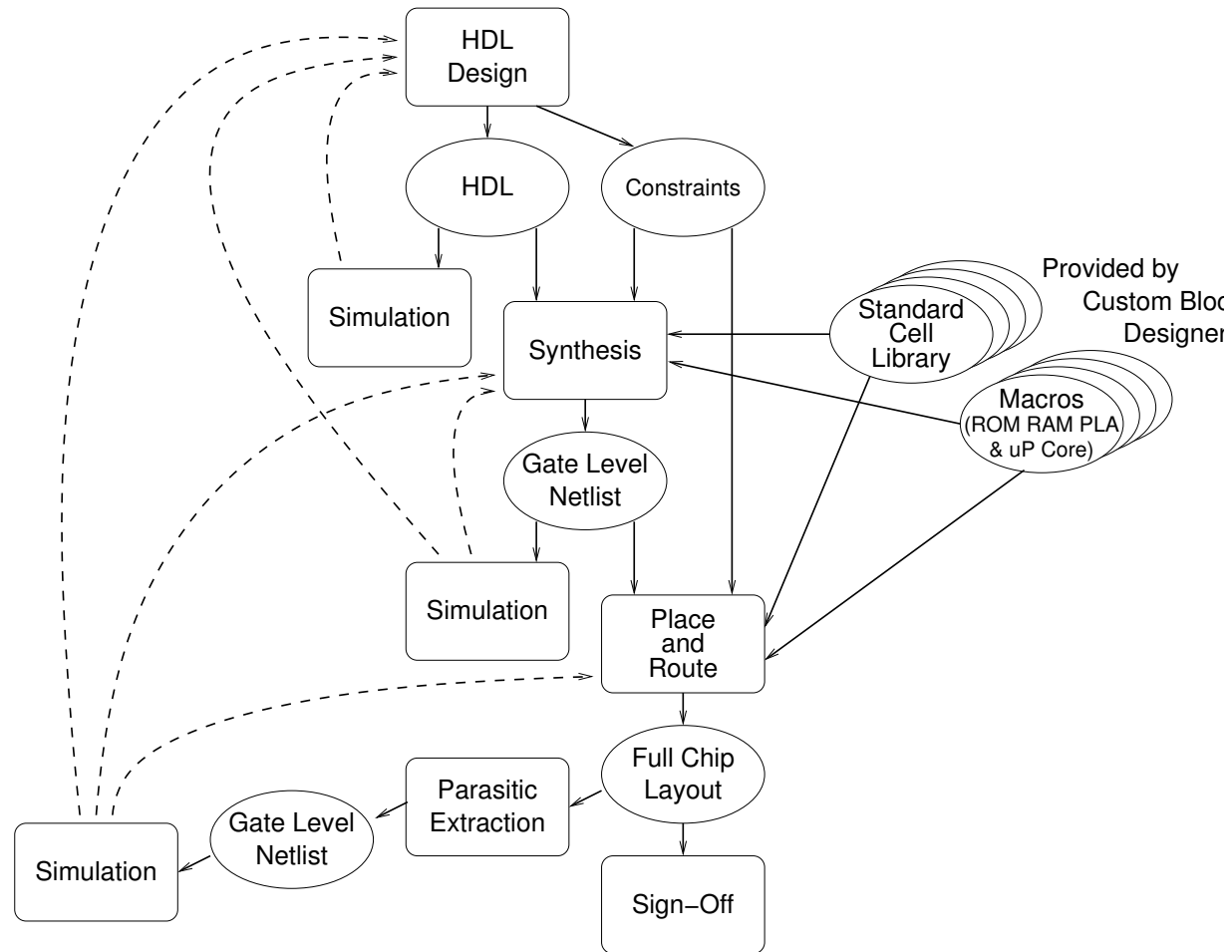
# Introduction to Synthesis

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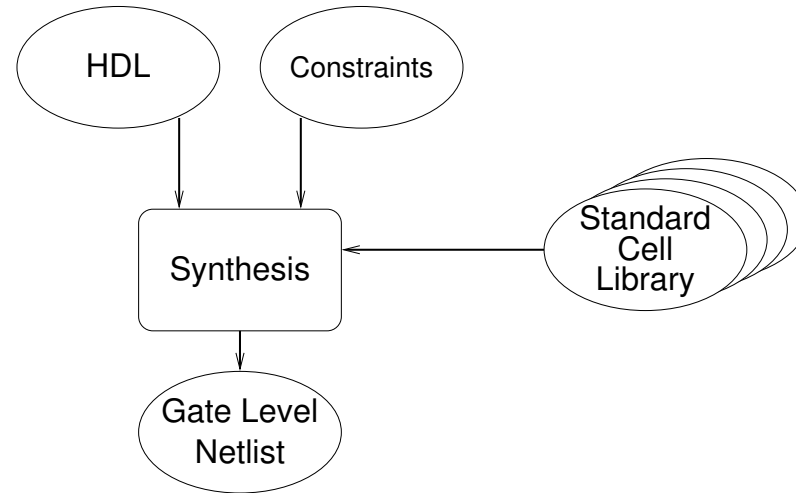
# Introduction to Synthesis

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# Introduction to Synthesis

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- HDL (Hardware Description Language)  
SystemVerilog file (.sv)
- Constraints  
Synopsys Design Constraints file (.sdc)
- Standard Cell Library  
Liberty file (.lib)

# Introduction to Synthesis

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## Timing Related Constraints

- Clock Constraints
- Input Constraints
- Output Constraints

# Introduction to Synthesis

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## Timing Related Constraints

- Clock Constraints

What the synthesis tool needs to know about the clock

- Input Constraints

- Output Constraints

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## Timing Related Constraints

- Clock Constraints

What the synthesis tool needs to know about the clock

- Input Constraints

What the synthesis tool needs to know about the inputs

- Output Constraints

# Introduction to Synthesis

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## Timing Related Constraints

- Clock Constraints

What the synthesis tool needs to know about the clock

- Input Constraints

What the synthesis tool needs to know about the inputs

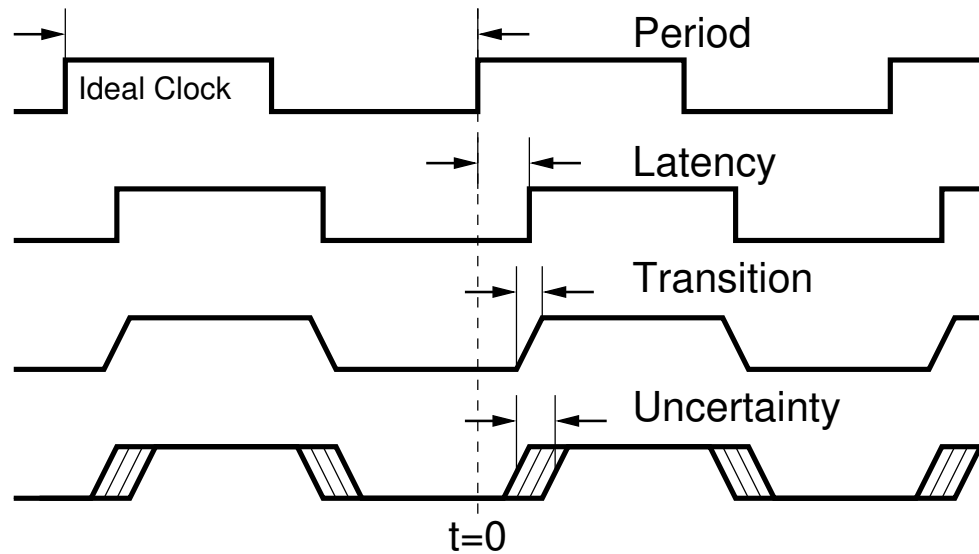
- Output Constraints

What the synthesis tool needs to know about the outputs

# Introduction to Synthesis

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## Clock Constraints



- Specify Clock Period

```
create_clock -period period_value -name clock_name clock_port
```

- Model Clock Tree  $uncertainty = skew + jitter$

```
set_clock_latency delay clock_object
```

```
set_clock_transition transition clock_object
```

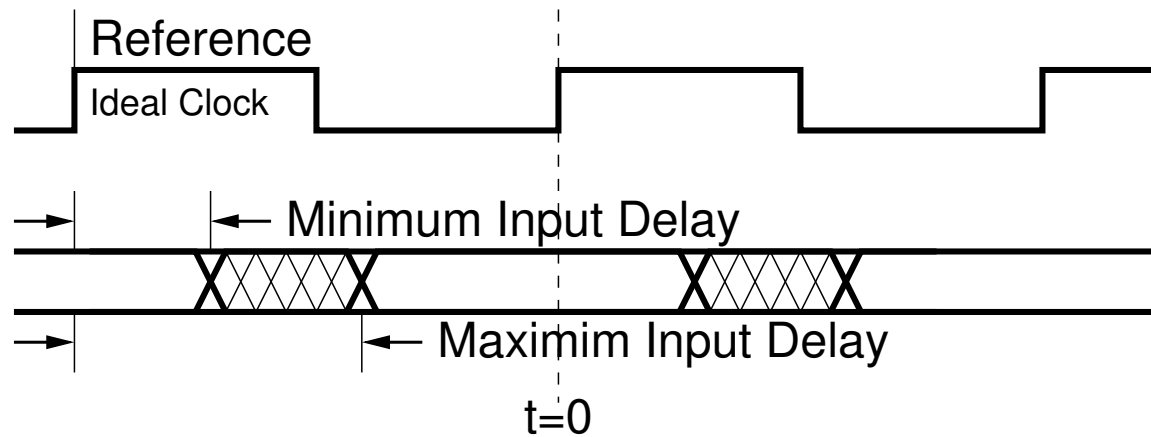
```
set_clock_uncertainty uncertainty clock_object
```



# Introduction to Synthesis

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## Input Constraints



- Specify Input Delay

```
set_input_delay max_value -max -clock clock_name port_pin_list
```

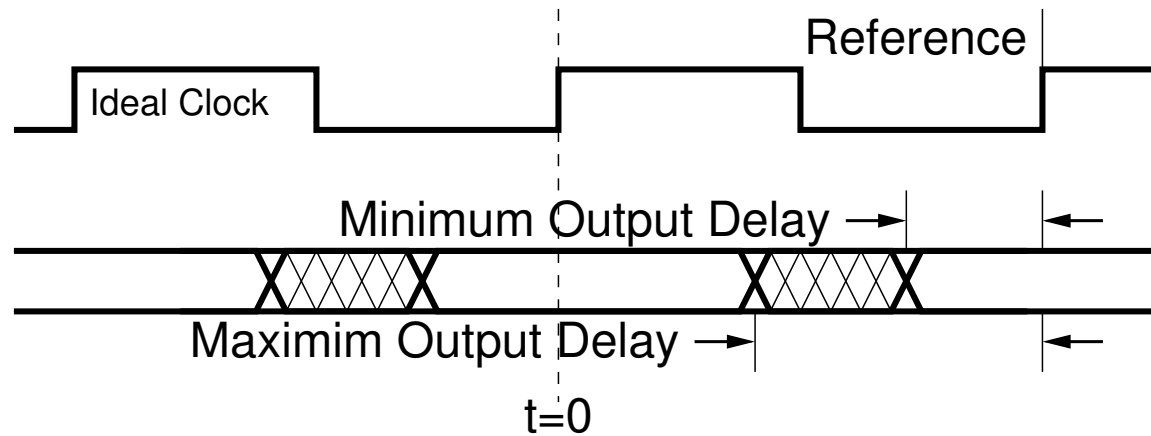
```
set_input_delay min_value -min -clock clock_name port_pin_list
```

*With a longer input delay, our circuit has less time to respond before the next clock edge.*

# Introduction to Synthesis

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## Output Constraints



- Specify Output Delay

`set_output_delay max_value -max -clock clock_name port_pin_list`

`set_output_delay min_value -min -clock clock_name port_pin_list`

*With a longer output delay, our circuit has to produce an output earlier in the clock cycle.*

# Introduction to Synthesis

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## Synthesis constraints (1)

- Specify Clock Frequency

```
create_clock -period 20 -name master_clock [get_ports Clock]
```

- Model Clock Tree  $uncertainty = skew + jitter$

```
set_clock_latency 2.5 [get_clocks master_clock]
set_clock_transition 0.5 [get_clocks master_clock]
set_clock_uncertainty 1.0 [get_clocks master_clock]
```

- Specify Input and Output Timing

```
set_output_delay 2.0 -max -network_latency_included -clock master_clock \
  [all_outputs]
```

```
set_output_delay 0.1 -min -network_latency_included -clock master_clock \
  [all_outputs]
```

```
set_input_delay 2.0 -max -network_latency_included -clock master_clock \
  [remove_from_collection [all_inputs] [get_ports Clock]]
```

```
set_input_delay 0.1 -min -network_latency_included -clock master_clock \
  [remove_from_collection [all_inputs] [get_ports Clock]]
```

# Introduction to Synthesis

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## Synthesis constraints (2)

- Specify Input Drive and Output Load

```
set_load 1.0 -max [all_outputs]  
set_load 0.01 -min [all_outputs]
```

```
set_driving_cell -max -library c35_IOLIB_WC -lib_cell BU24P -pin PAD [all_inputs]  
set_driving_cell -min -library c35_IOLIB_WC -lib_cell BU1P -pin PAD [all_inputs]
```

- Specify Timing Exclusions

```
set_ideal_network [get_ports nReset]
```

- Other constraints

```
set_max_area 0
```