

Cadence Place and Route

Version 1

Small Designs - Standard Cells Only

2001

Cadence Place and Route

Pre-requisites

- Gate-level netlist
structural Verilog (.v) file including pad instances
- Chip pinout definition file
in Encounter .io format
- Full chip constraints
as one or more Synopsys Design Constraints (.sdc) files

Cadence Place and Route

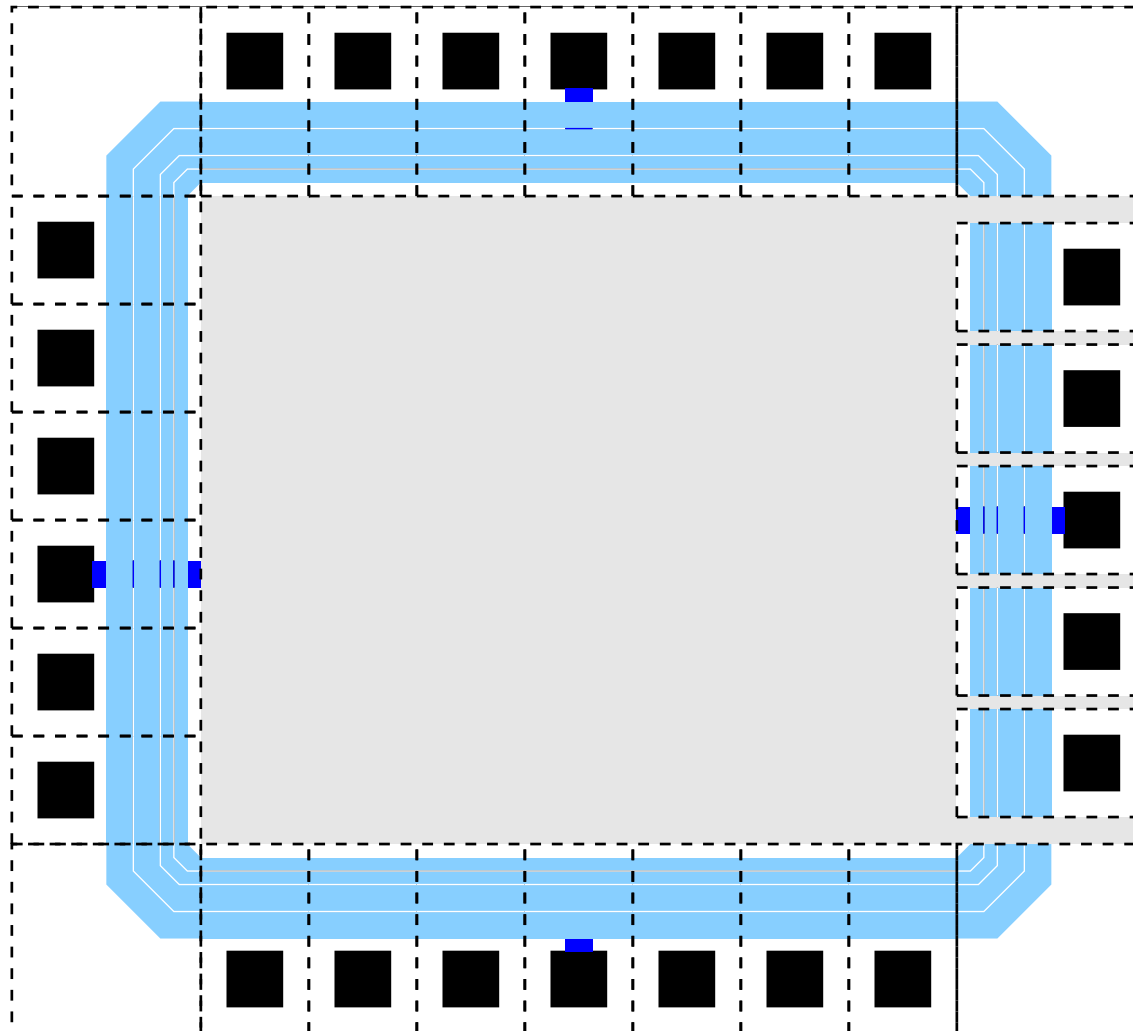
Preparation

- Run AMS HitKit script and add symbolic links to design files:
Gate-level design (.v) and Constraints (.sdc)

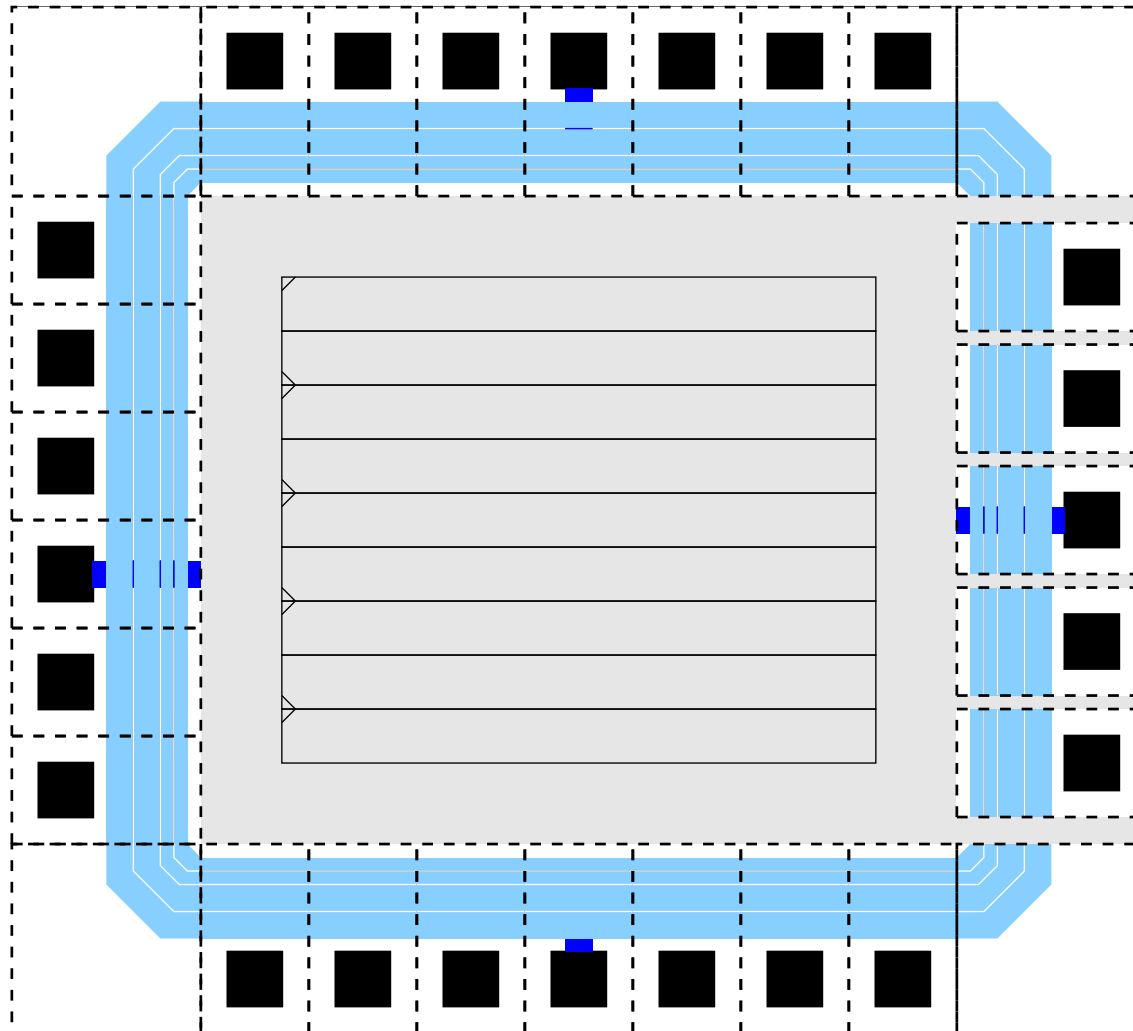
Import the Design

- Start Place-and-Route Tool
- Load Design-kit related libraries and scripts
- Load Gate-level design and Constraints

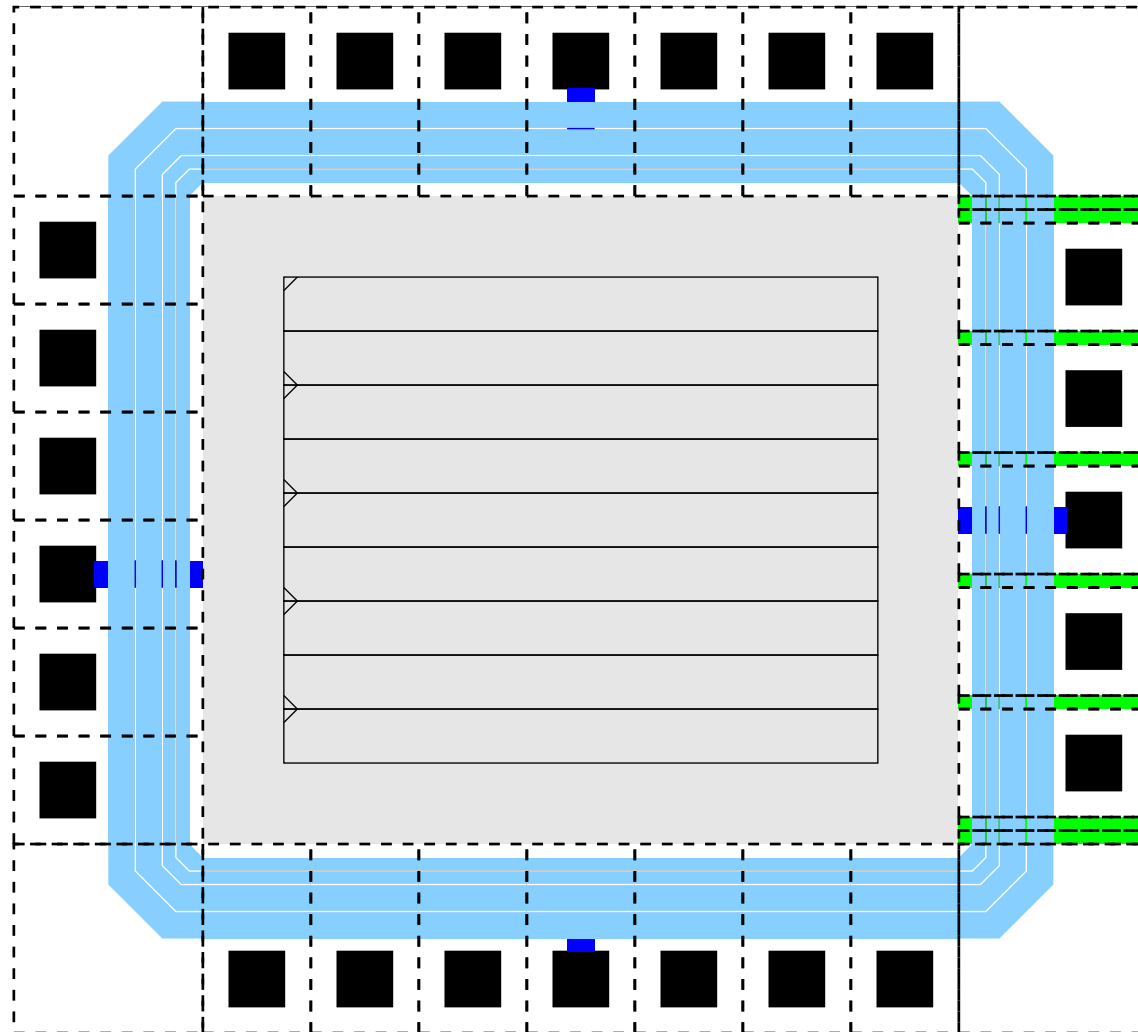
Place the Pad Cells



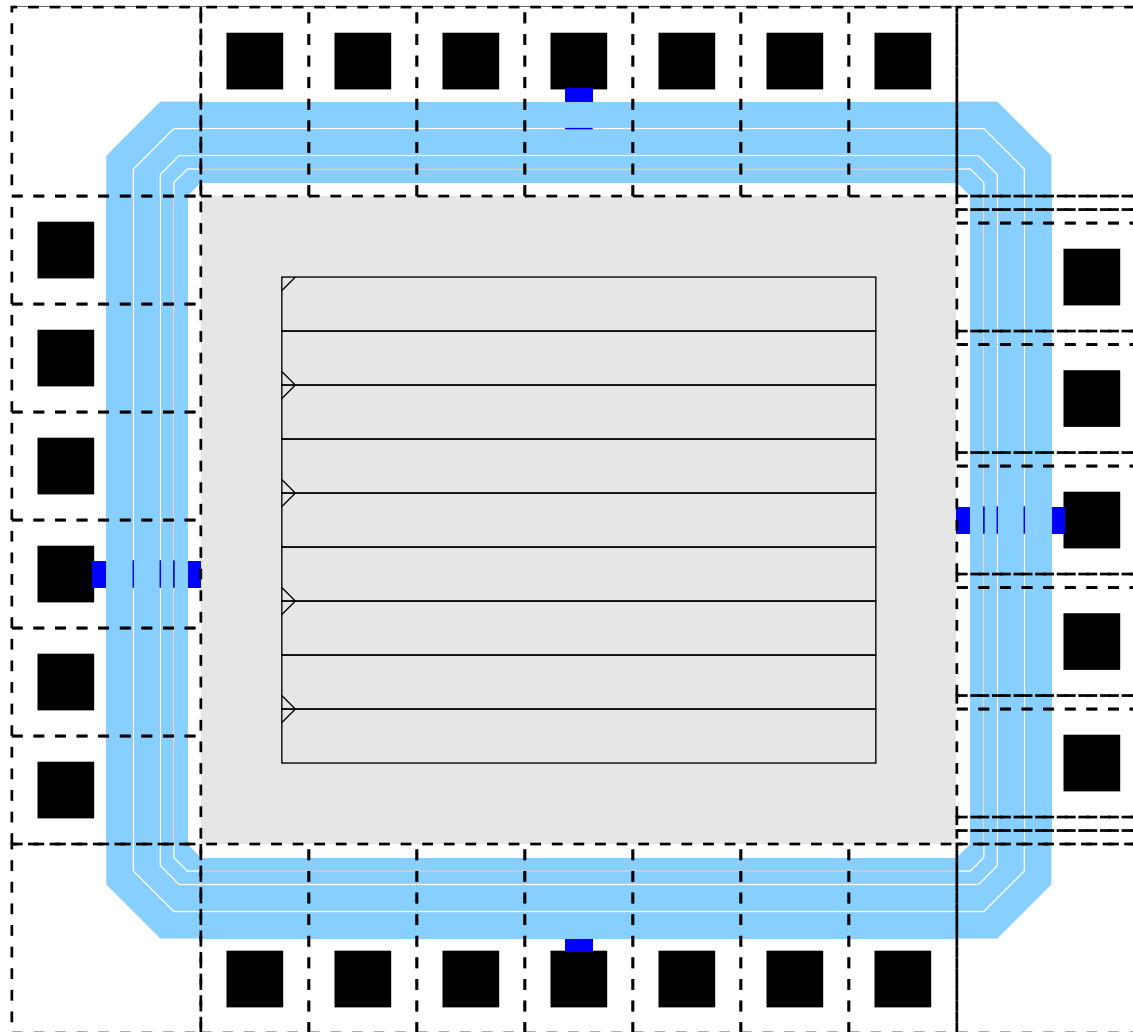
Specify Floor Plan



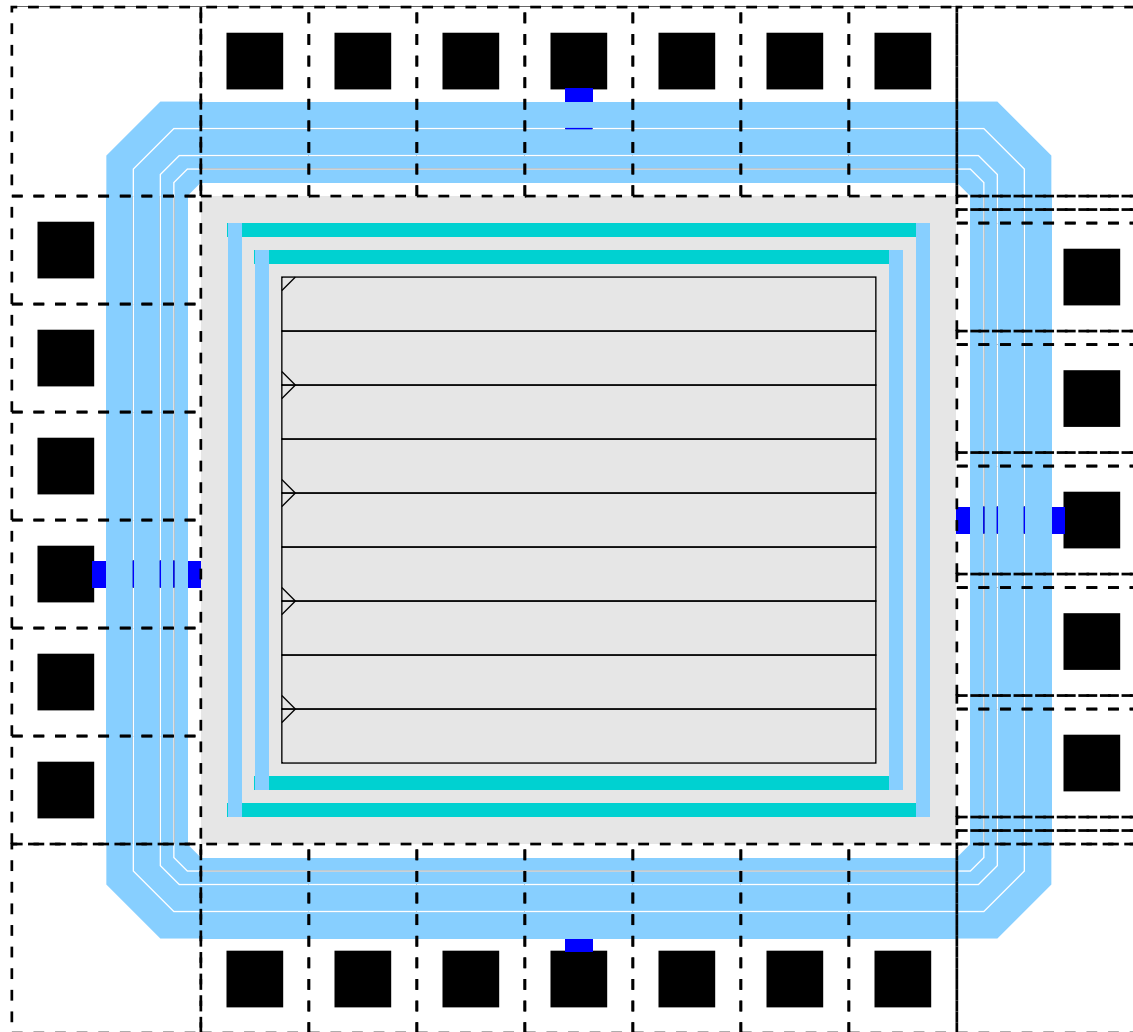
Add IO Filler Cells



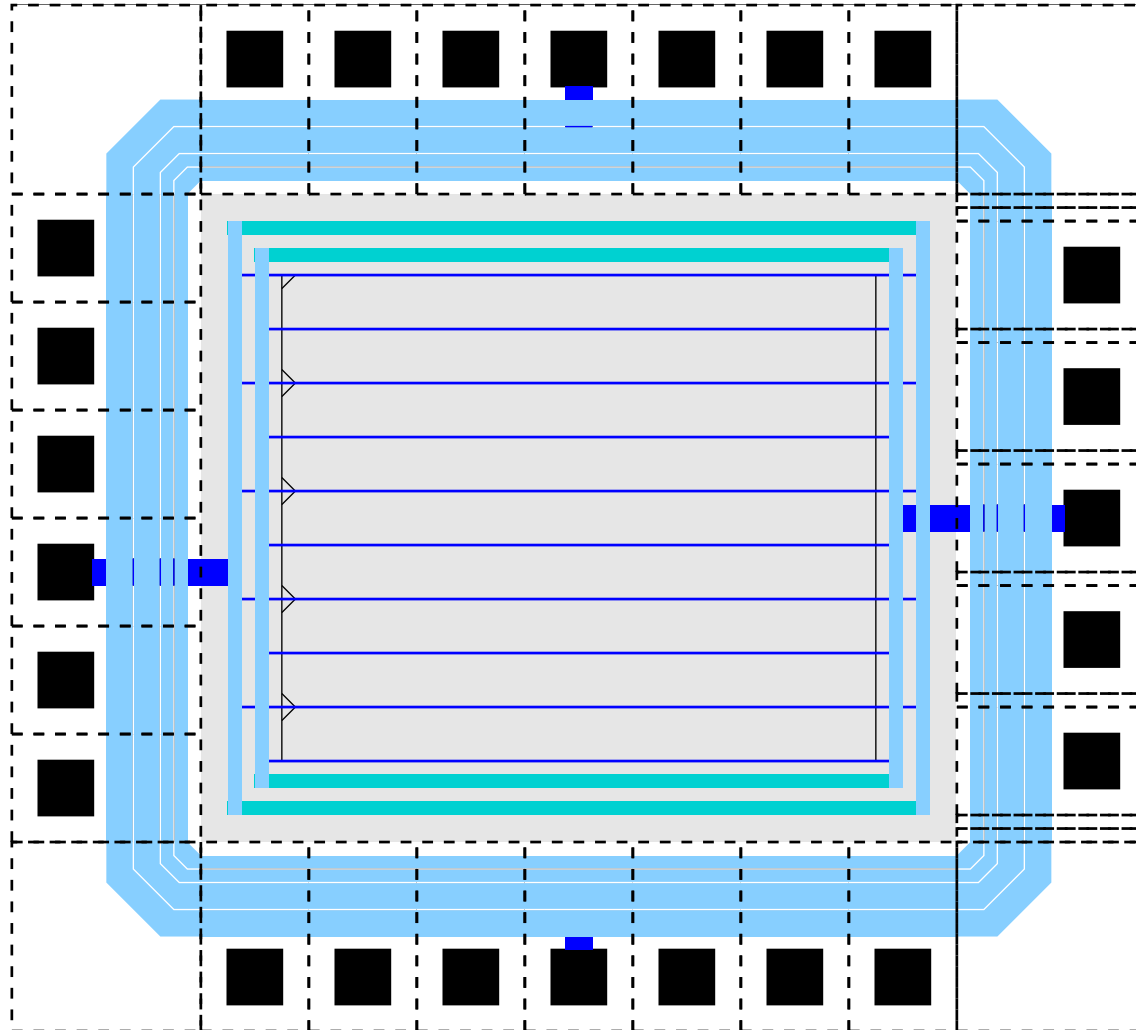
Add IO Filler Cells



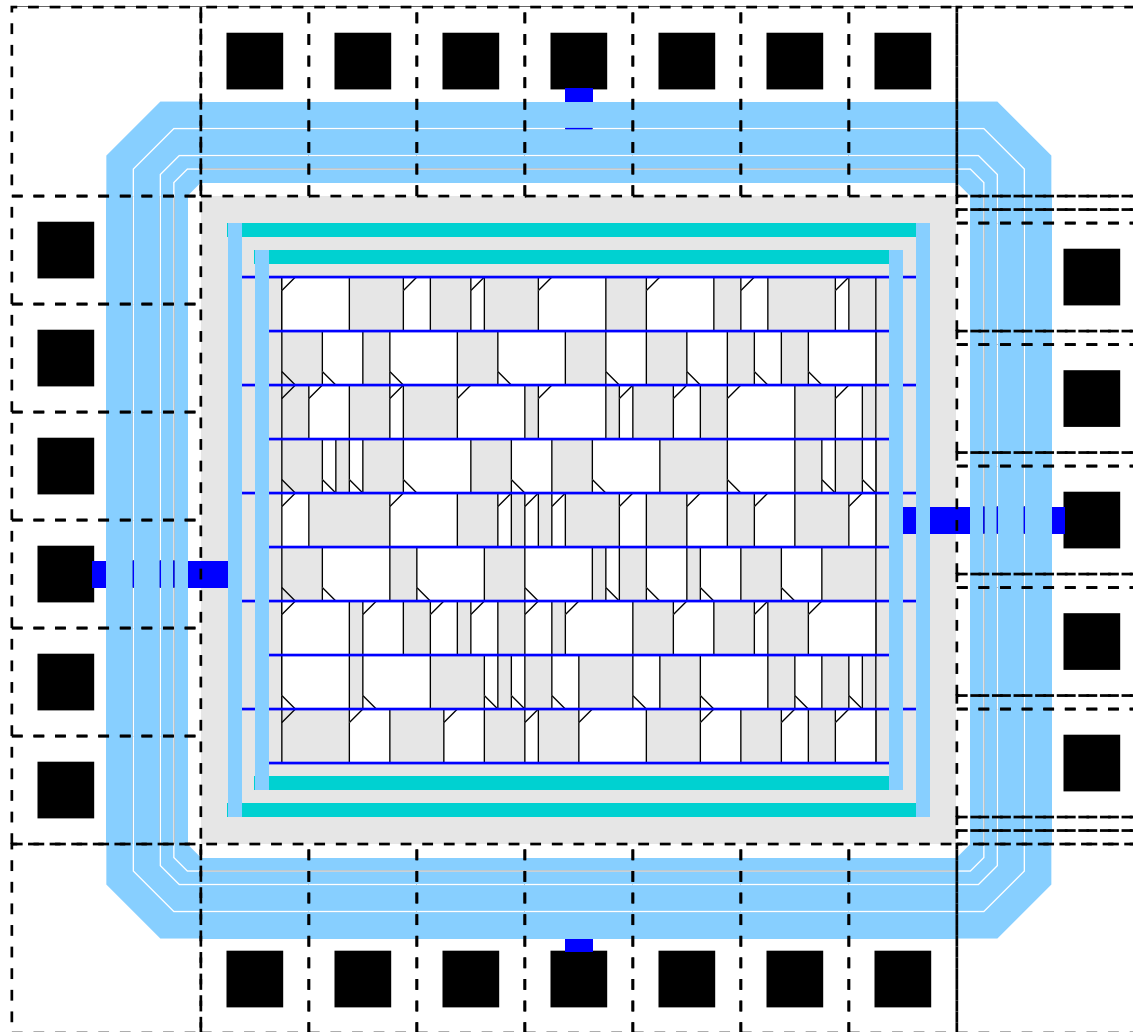
Add Core Power Rings



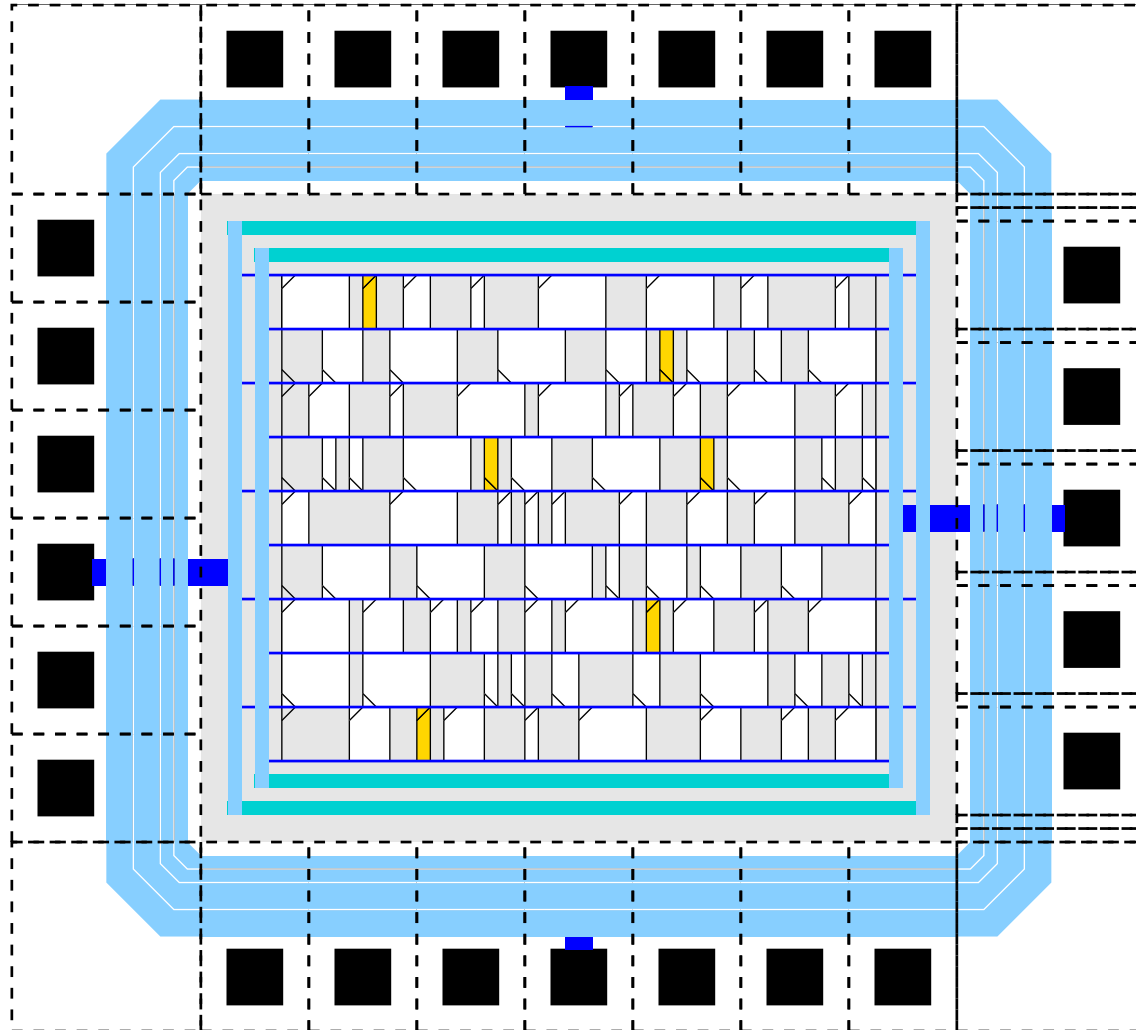
Add Power Routing



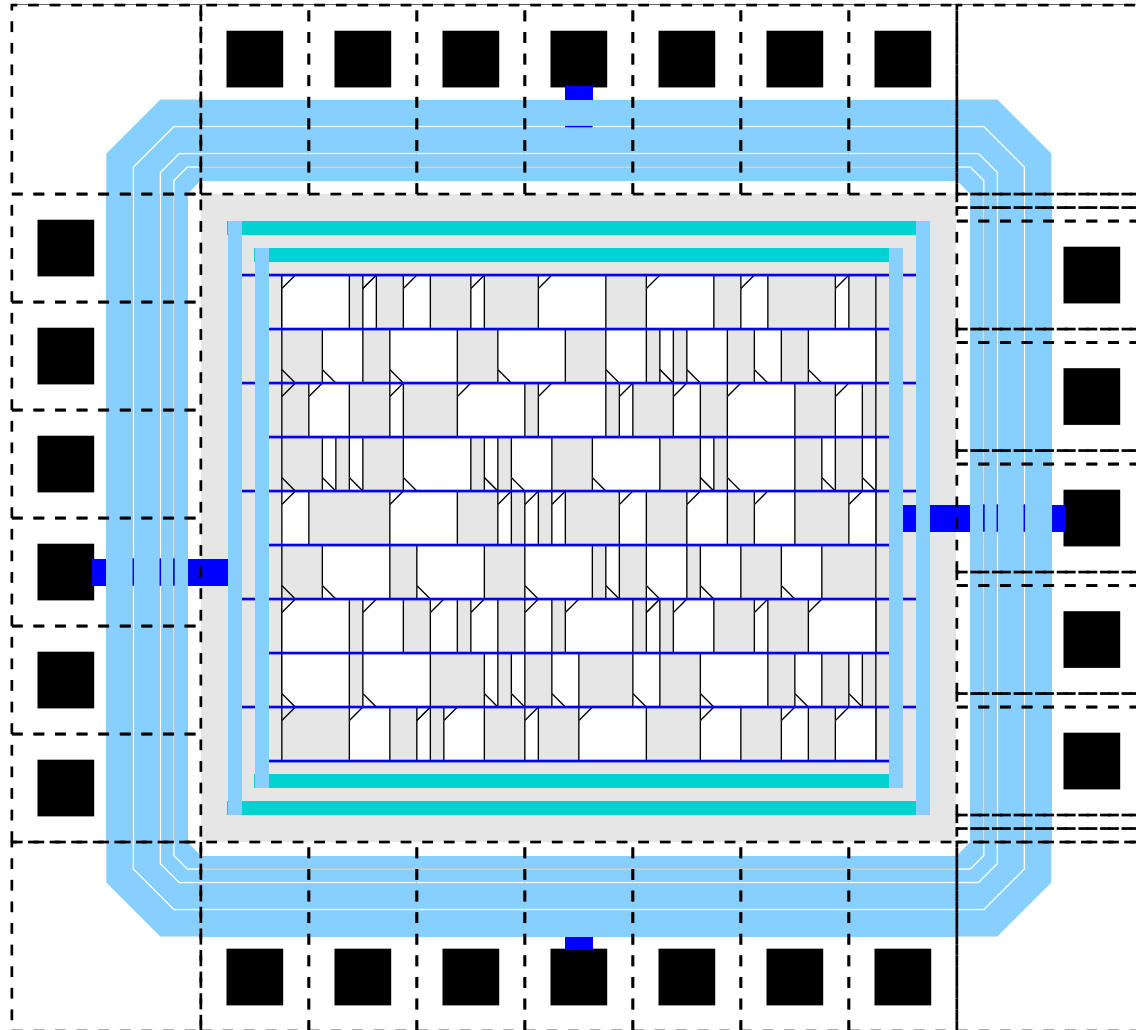
Place Cells



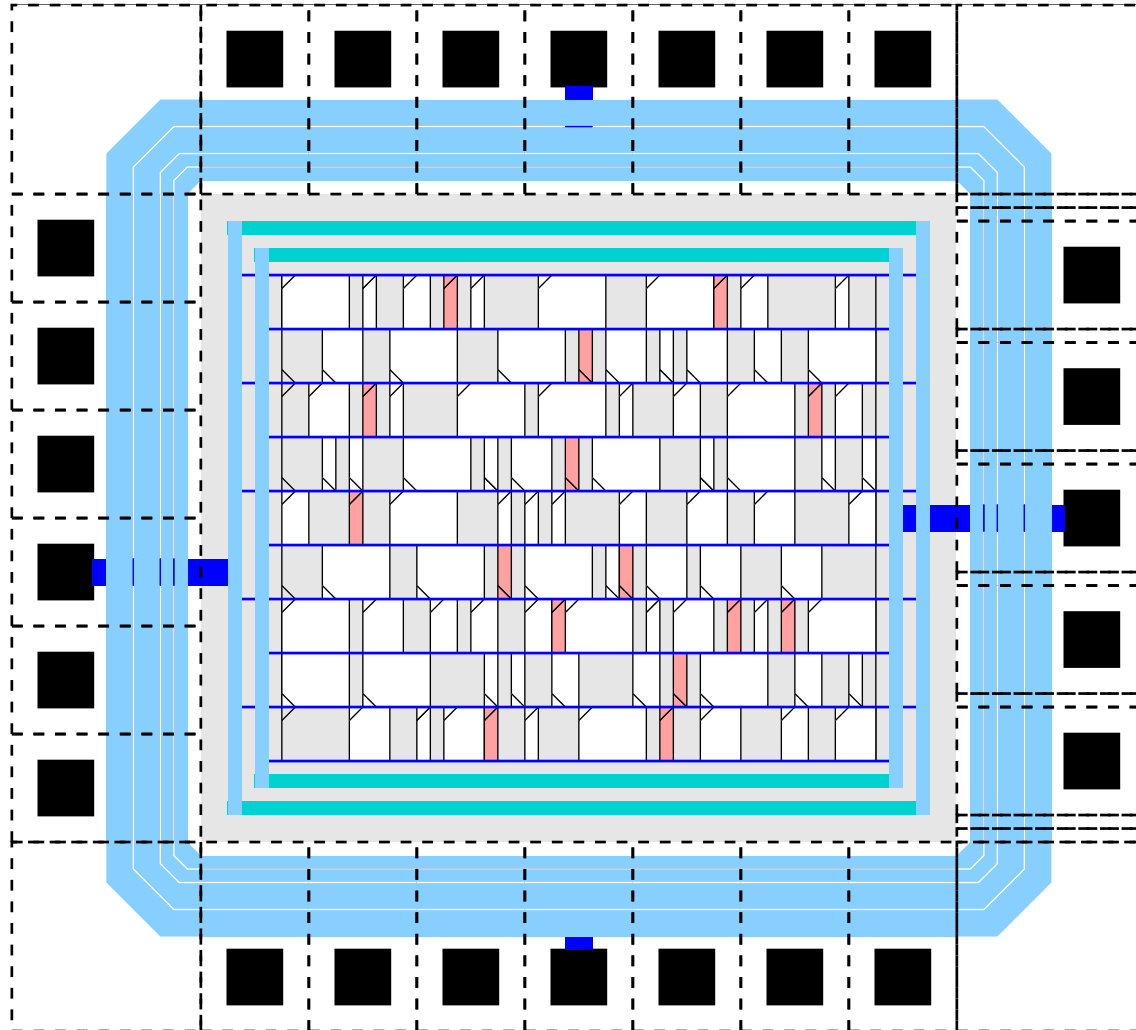
Fix Potential Problems (Pre-CTS Optimisation)



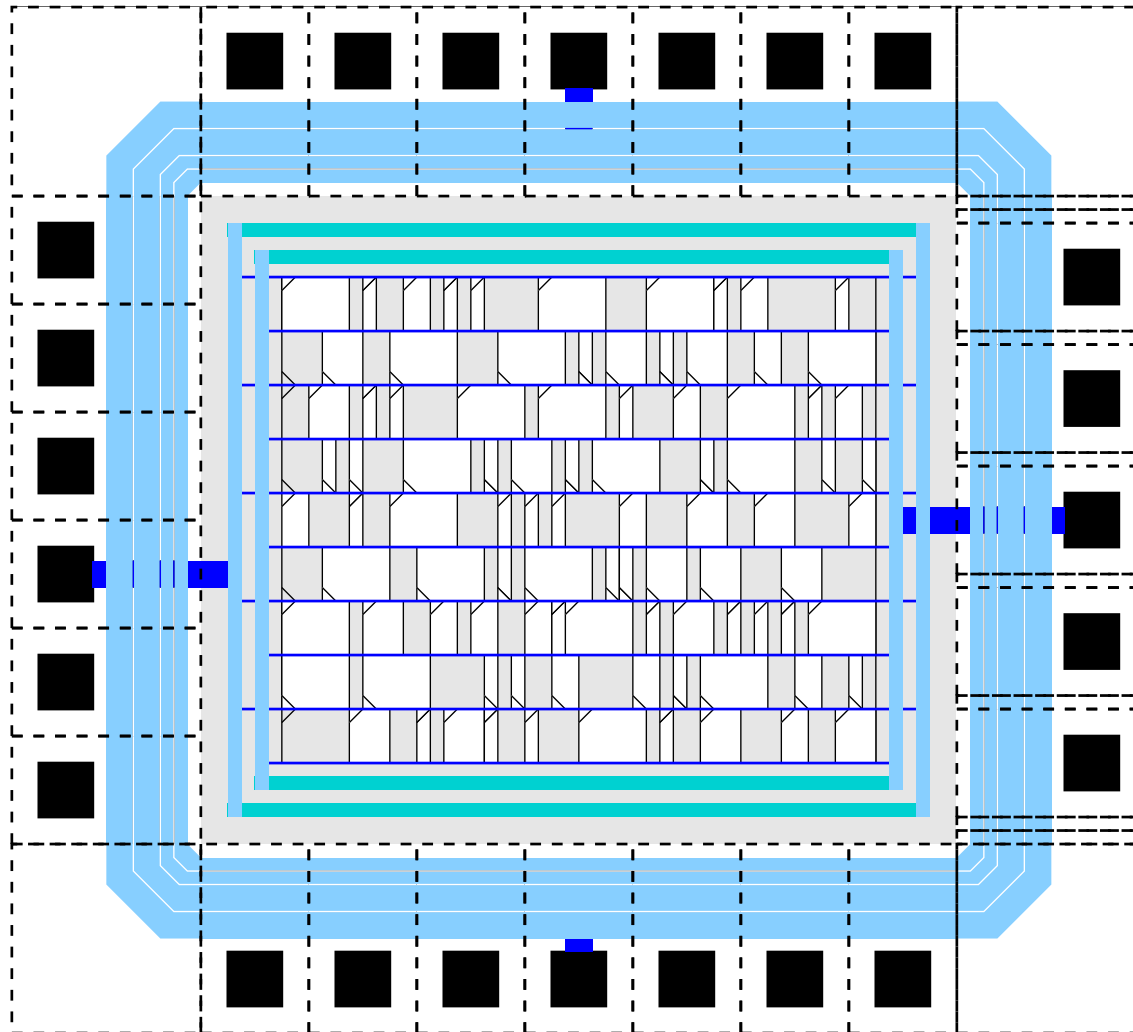
Fix Potential Problems (Pre-CTS Optimisation)



Clock Tree Synthesis



Clock Tree Synthesis

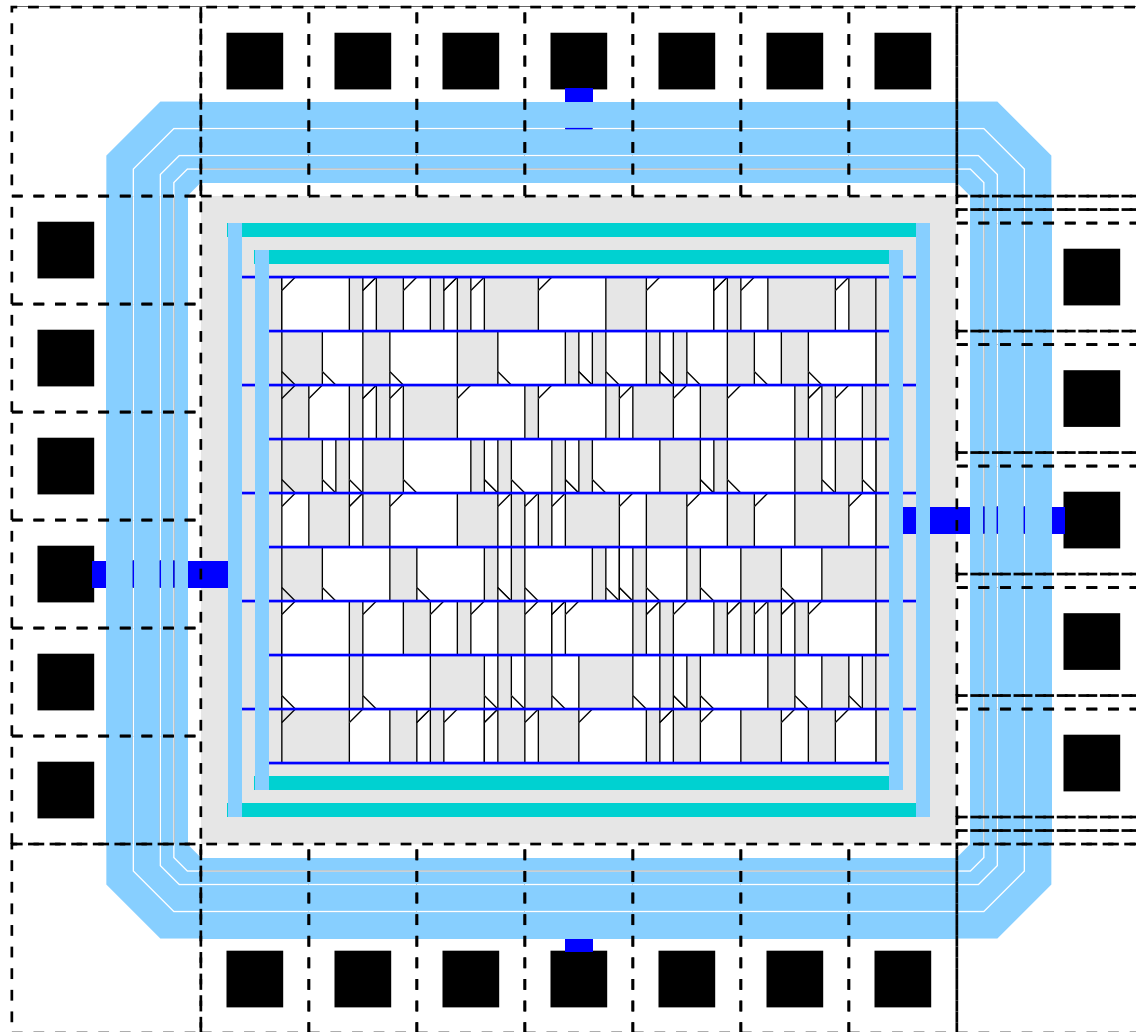


Cadence Place and Route

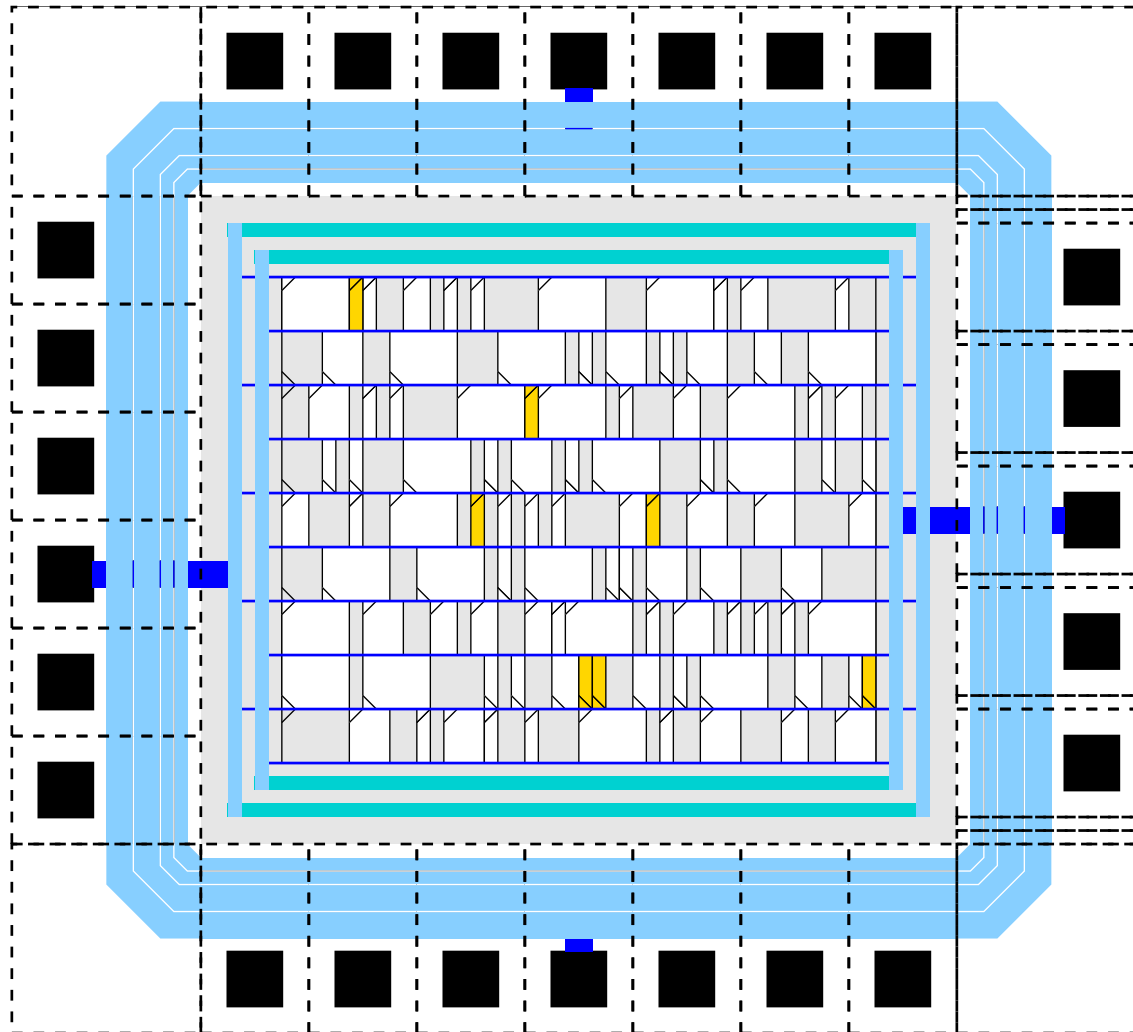
Update Constraints

- The original constraints attempt to model the delays and the clock skew introduced by the clock tree.
- Now that we have a real clock tree we need to adjust the constraints to take account of this.

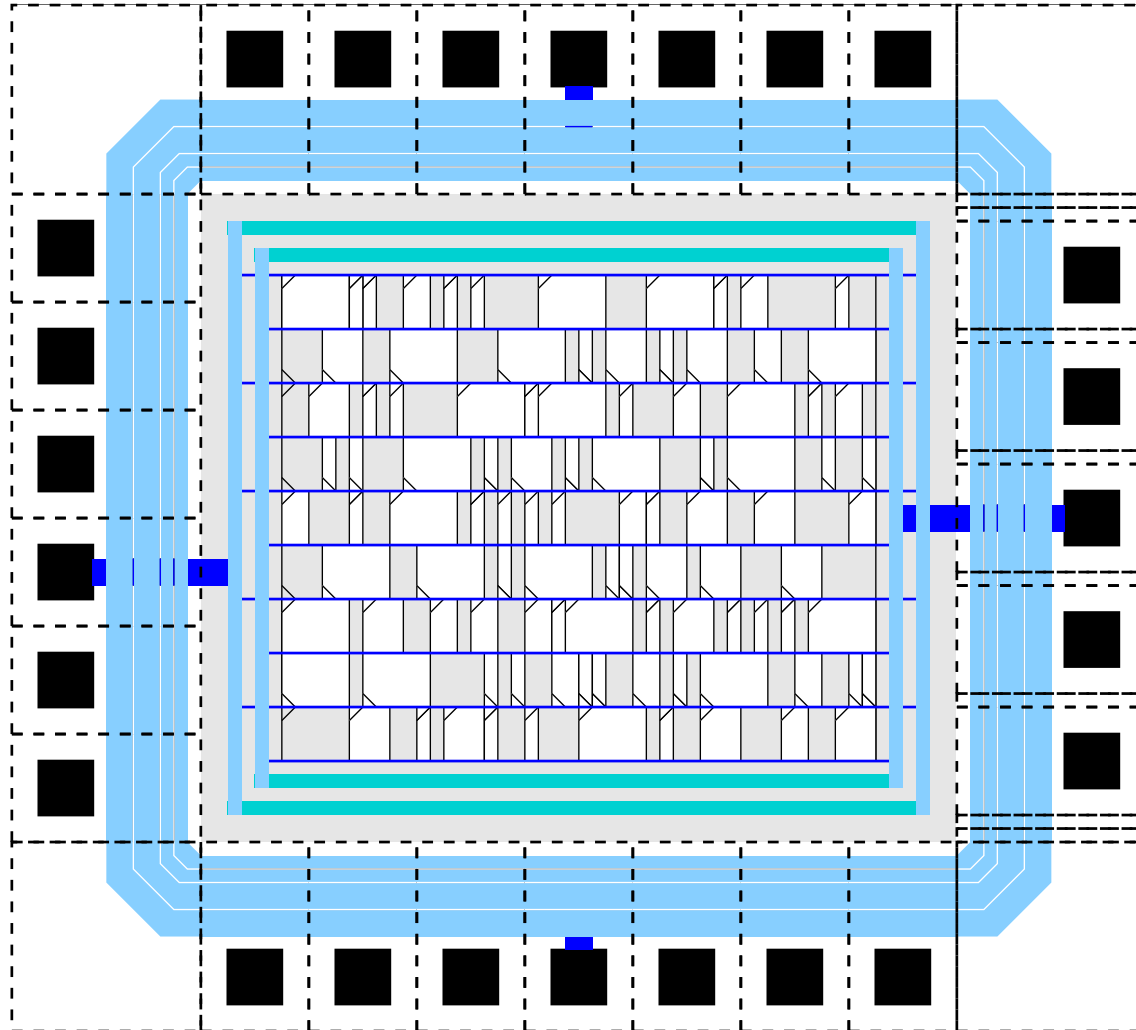
Fix Potential Problems (Post-CTS Optimisation)



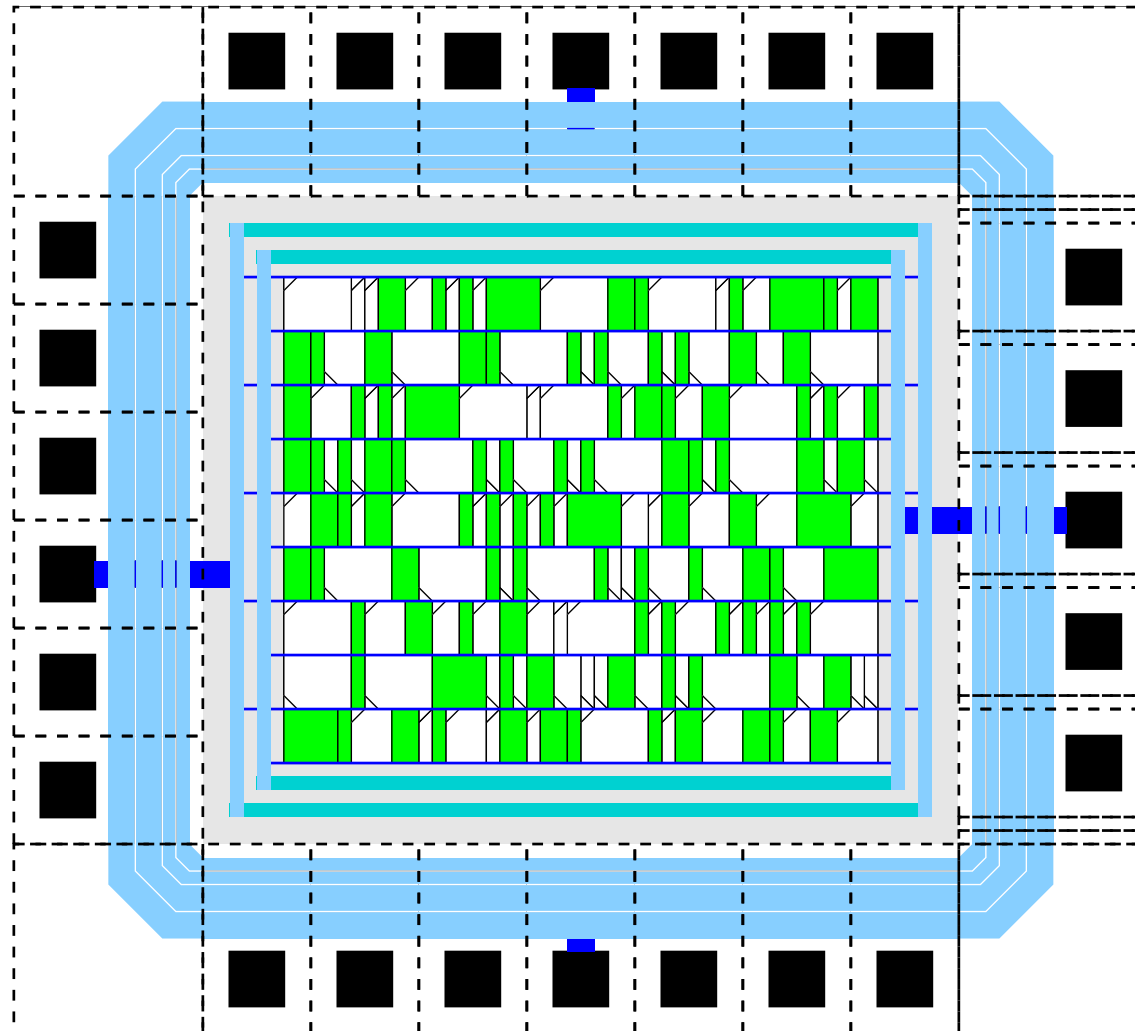
Fix Potential Problems (Post-CTS Optimisation)



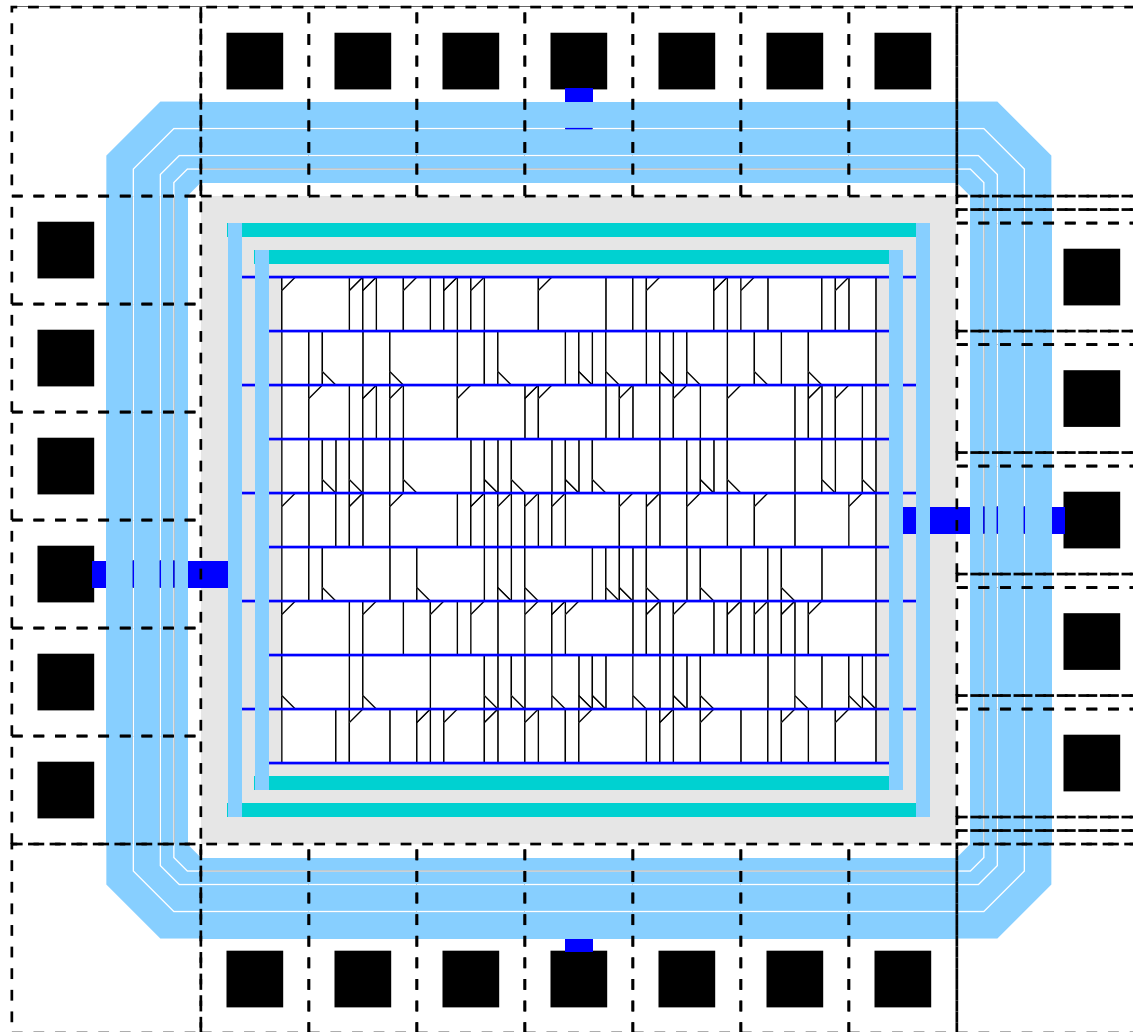
Fix Potential Problems (Post-CTS Optimisation)



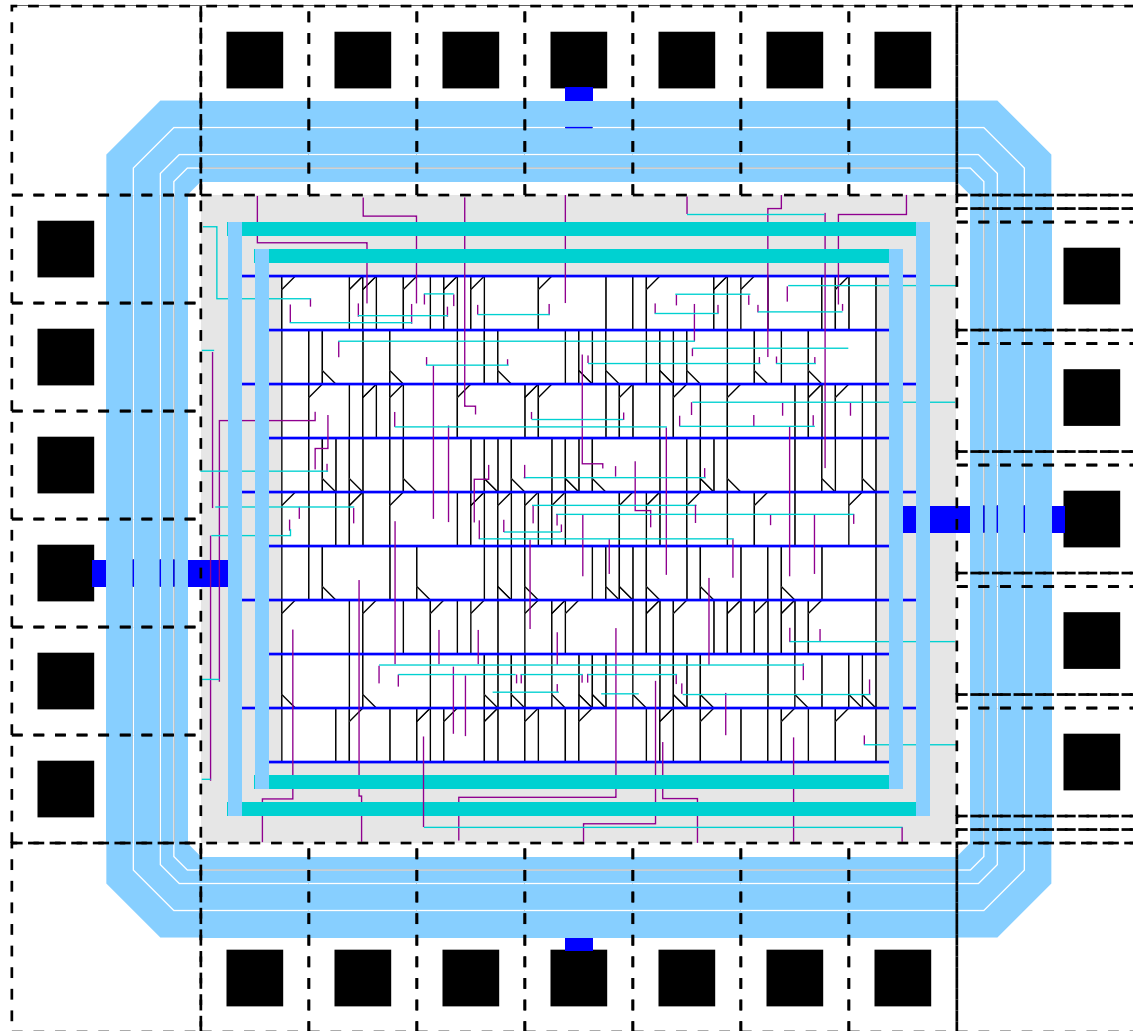
Add Filler Cells



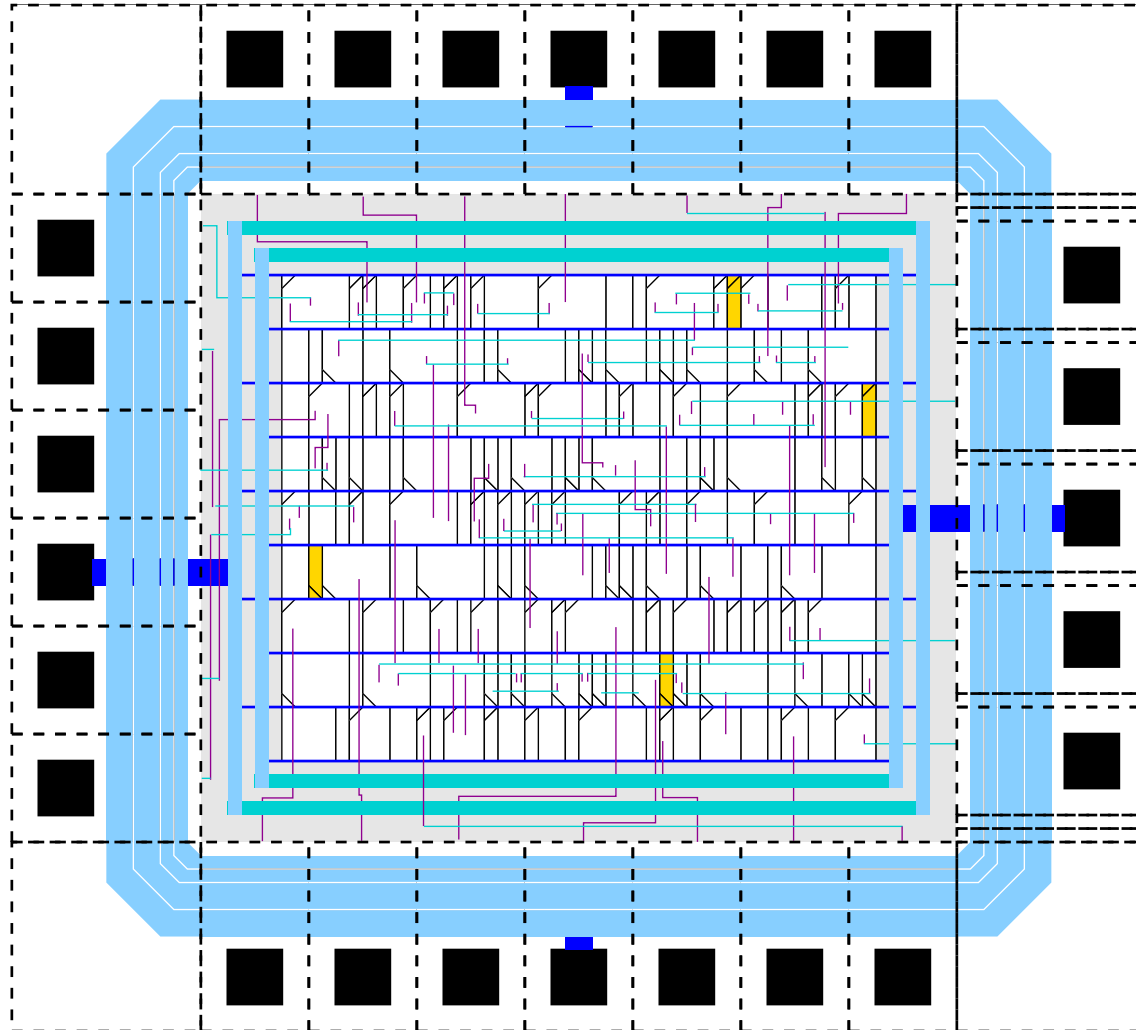
Add Filler Cells



Route Design



Fix Problems (Post-Route Optimisation)



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