

D.I.C.D.

Digital Integrated Circuit Design

Iain McNally

< 12 lectures - Tuesday Afternoons¹

12 lab sessions - **Every** Thursday Morning

¹lectures advertised via the course e-mail list

Digital IC Design

- Content

- Layout for VLSI

- Cell layout, Standard cell layout, Full and semi-custom design, Floorplanning, Bit slice design.

- Digital design using SystemVerilog

- Introduction to SystemVerilog, Design for Synthesis.

- CAD Tools & Techniques

- Magic VLSI layout editor, HSpice analogue circuit simulator, SystemVerilog Hardware Description Language and digital simulator, Cadence IC design toolset.

Digital IC Design

- **Assessment - 100% Coursework**

Desex1 10% Design and optimization of a CMOS gate using Magic

Mini design exercise (automatically marked?) – No formal write-up

Desex2 20% Design of a digital system using SystemVerilog HDL

Mini design exercise – No formal write-up

Desex3 35% Design of a standard cell library using Magic

Team exercise – Formal report

Desex4 35% Bitslice Design using Magic and SystemVerilog HDL

Individual exercise – Basic documentation (just design diagrams)

Assess 25% Ongoing laboratory assessment

Attendance + Progress + Up to date log book

$$Mark = (Desex1 + Desex2 + Desex3 + Desex4) \times \frac{75 + Assess}{100}$$

Digital IC Design

- Book

- **Integrated Circuit Design**

- a.k.a. Principles of CMOS VLSI Design - A Circuits and Systems Perspective

- Neil Weste & David Harris

- Pearson 2011

- Notes & Resources

- Lecture notes and Design Exercises

- <http://users.ecs.soton.ac.uk/bim/notes/did>

- Lab Sheets and Reference Material

- <http://users.ecs.soton.ac.uk/bim/notes/cad>