

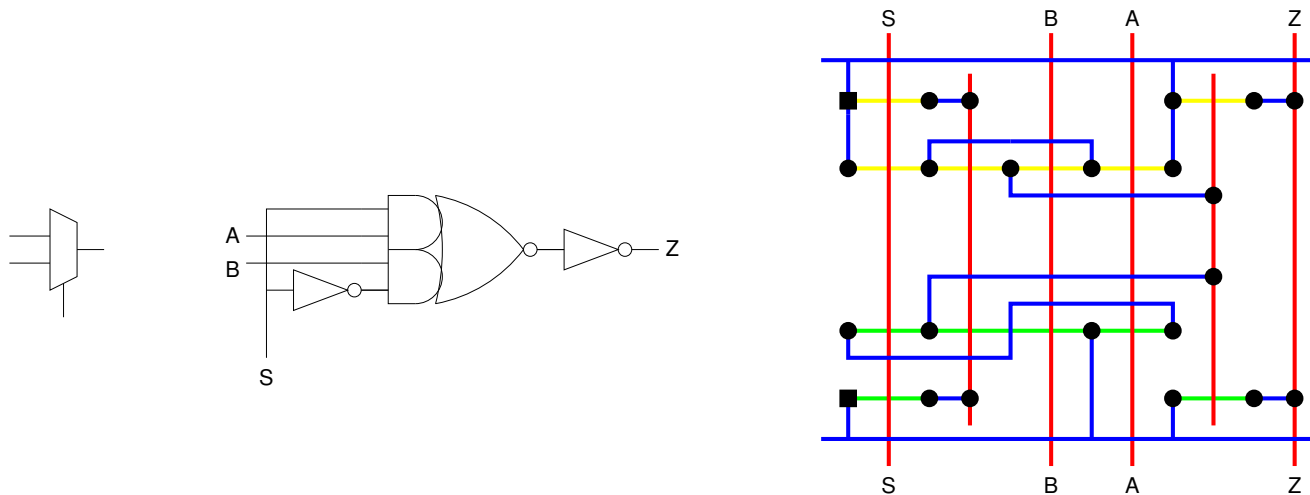
# Alternative Cell Design Strategy

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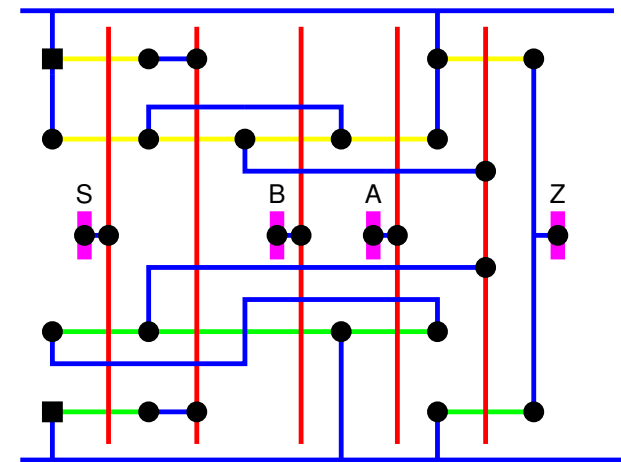
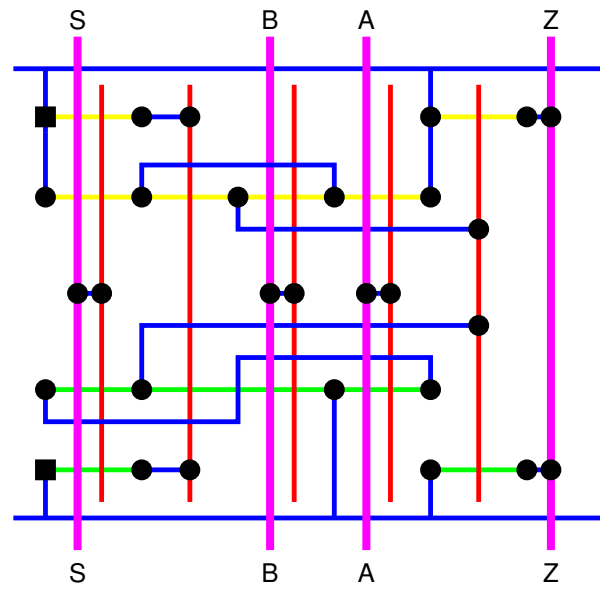
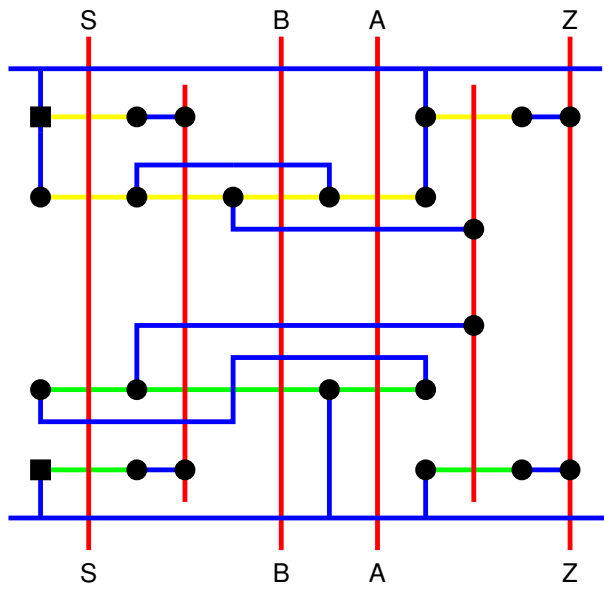
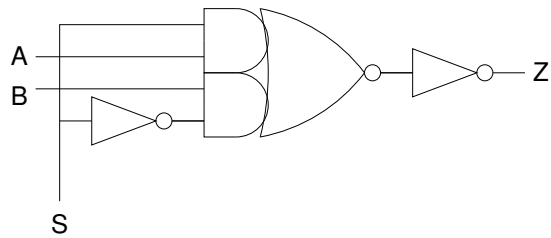
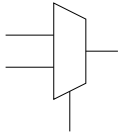
## Gate Matrix Style

The circuit is created as a matrix of intersecting transistor diffusion rows and polysilicon columns.

A simple example is the two input multiplexor we saw earlier. We align transistors on their common gate connections (as for *line of diffusion* designs), but here we allow multiple transistors to use the same polysilicon column.



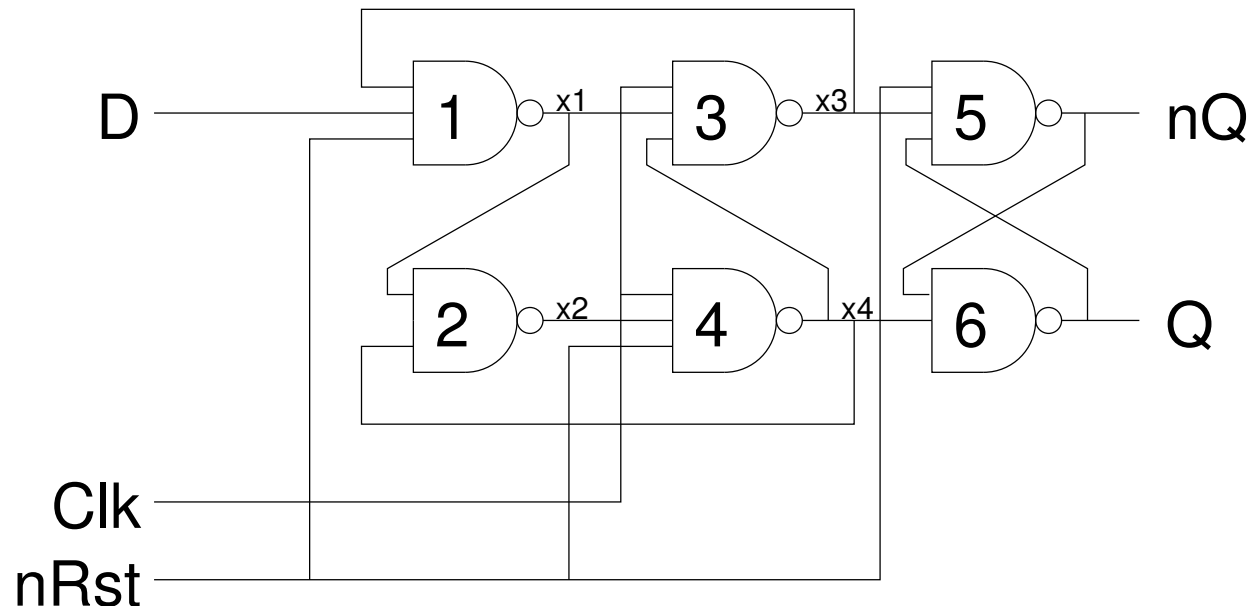
# Gate Matrix Style Mux – (for processes with one, two or three metal layers)



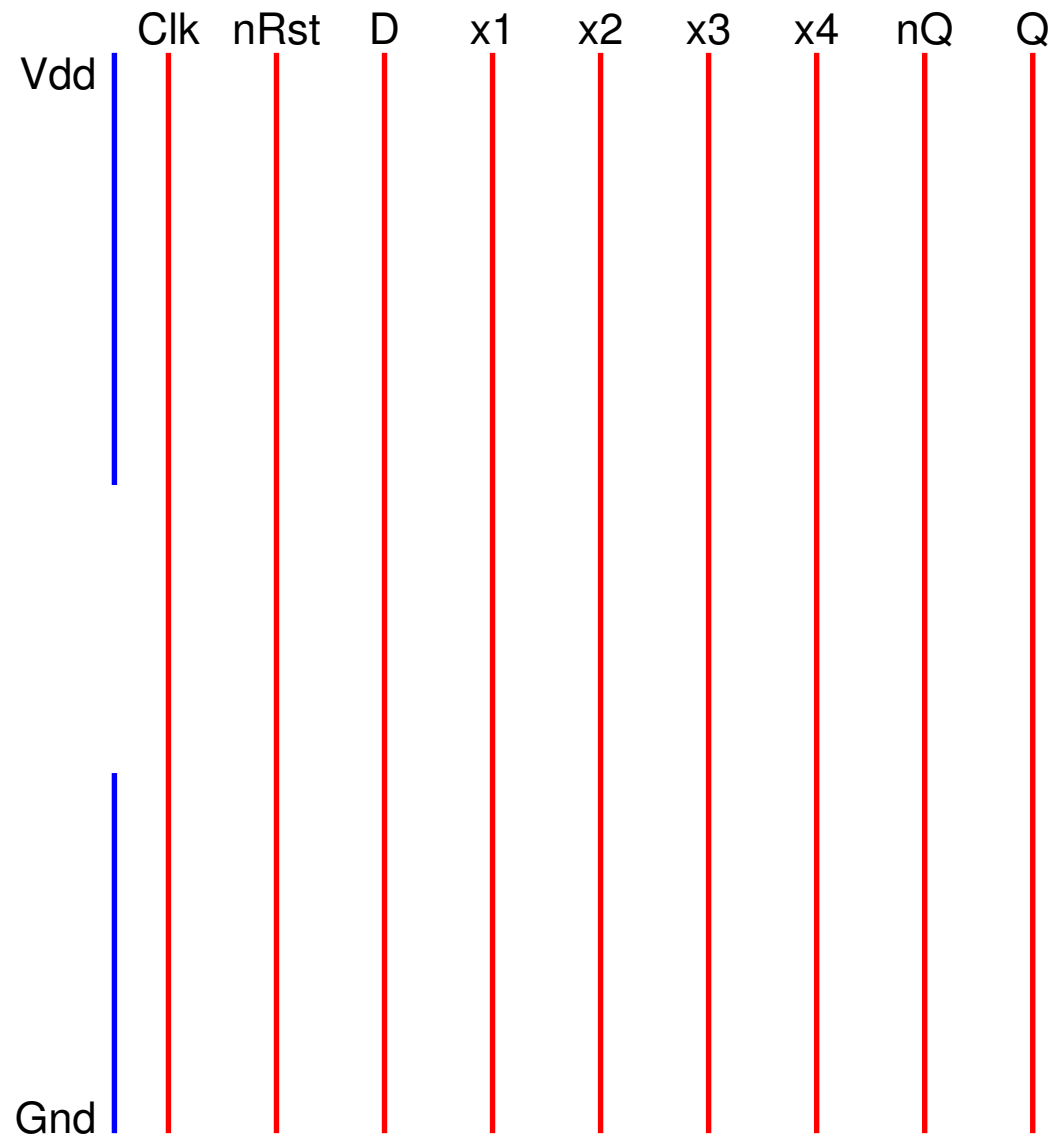
# Gate Matrix Style

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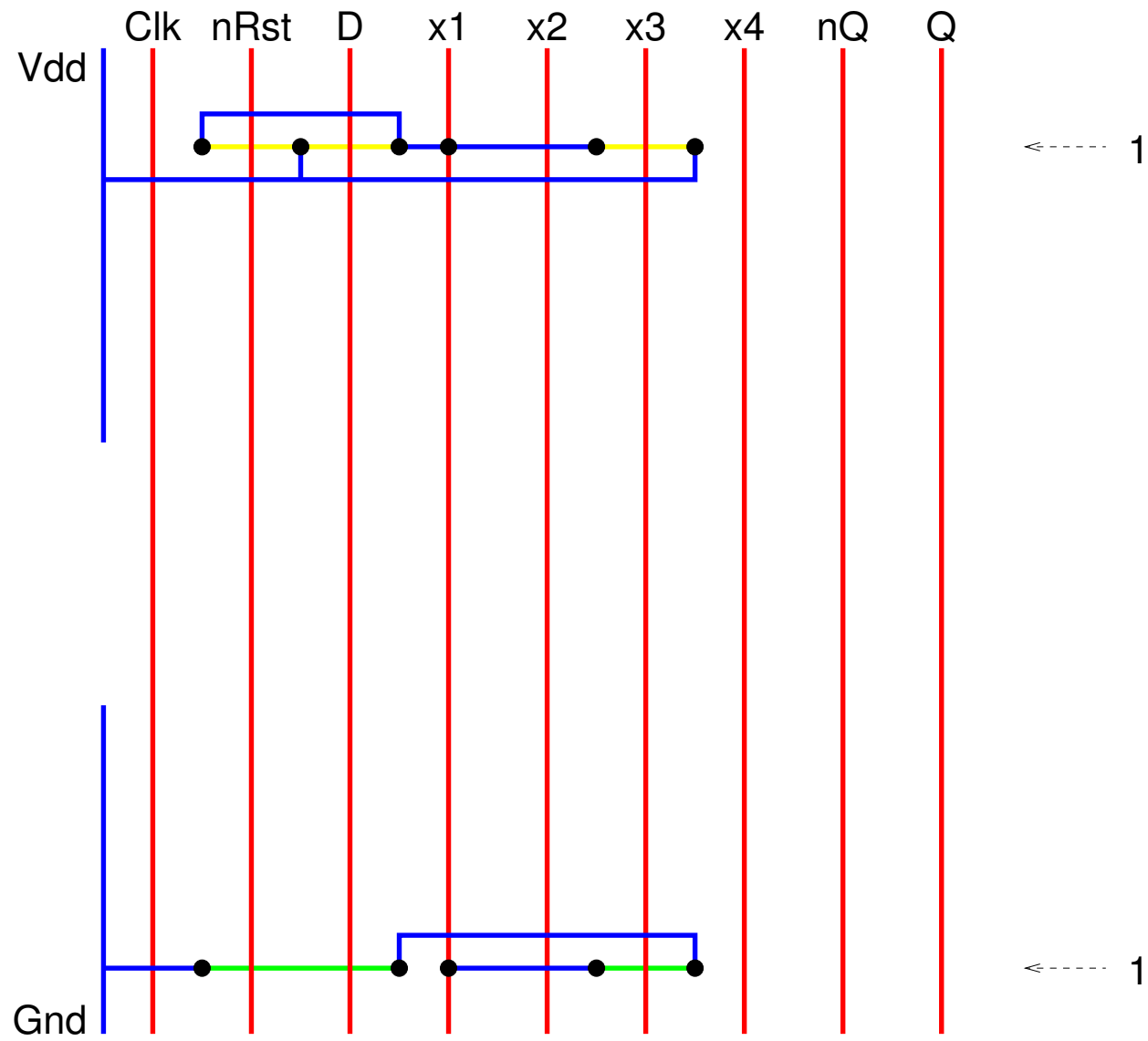
The layout of a standard six NAND gate d-type should illustrate the style more completely.

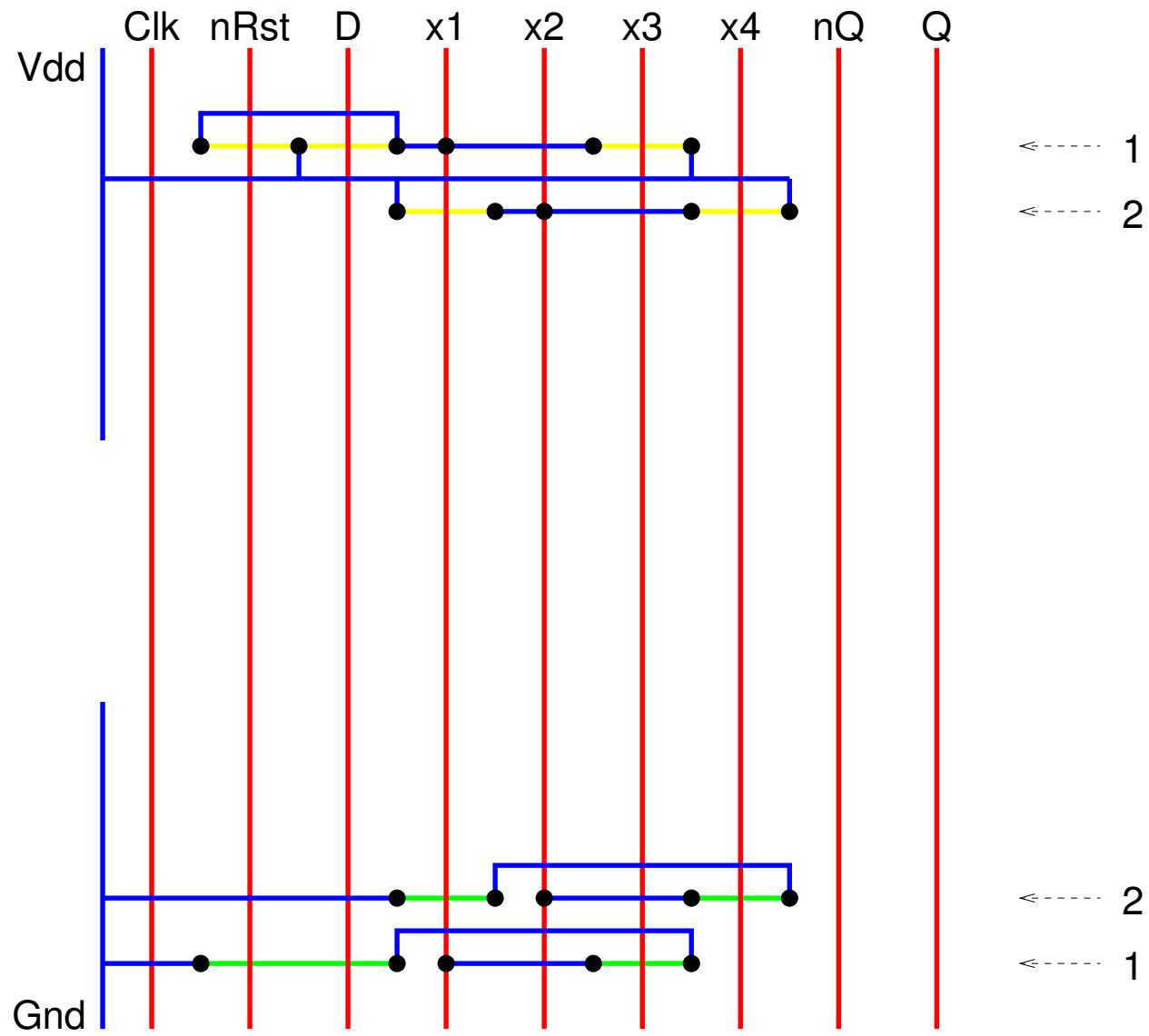


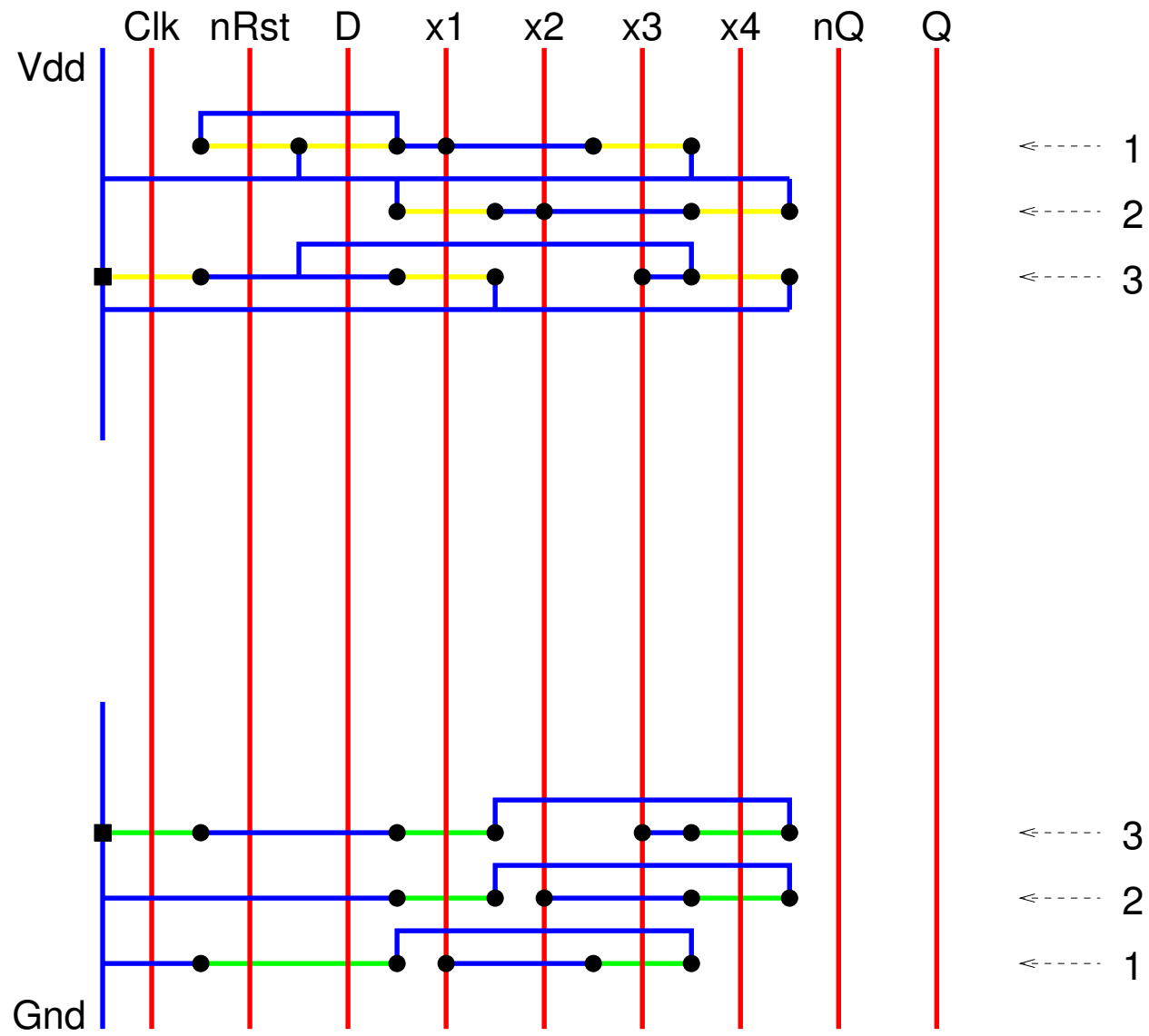
Here each NAND gate is allocated a different pair of rows in the layout (further optimization of this circuit is possible).





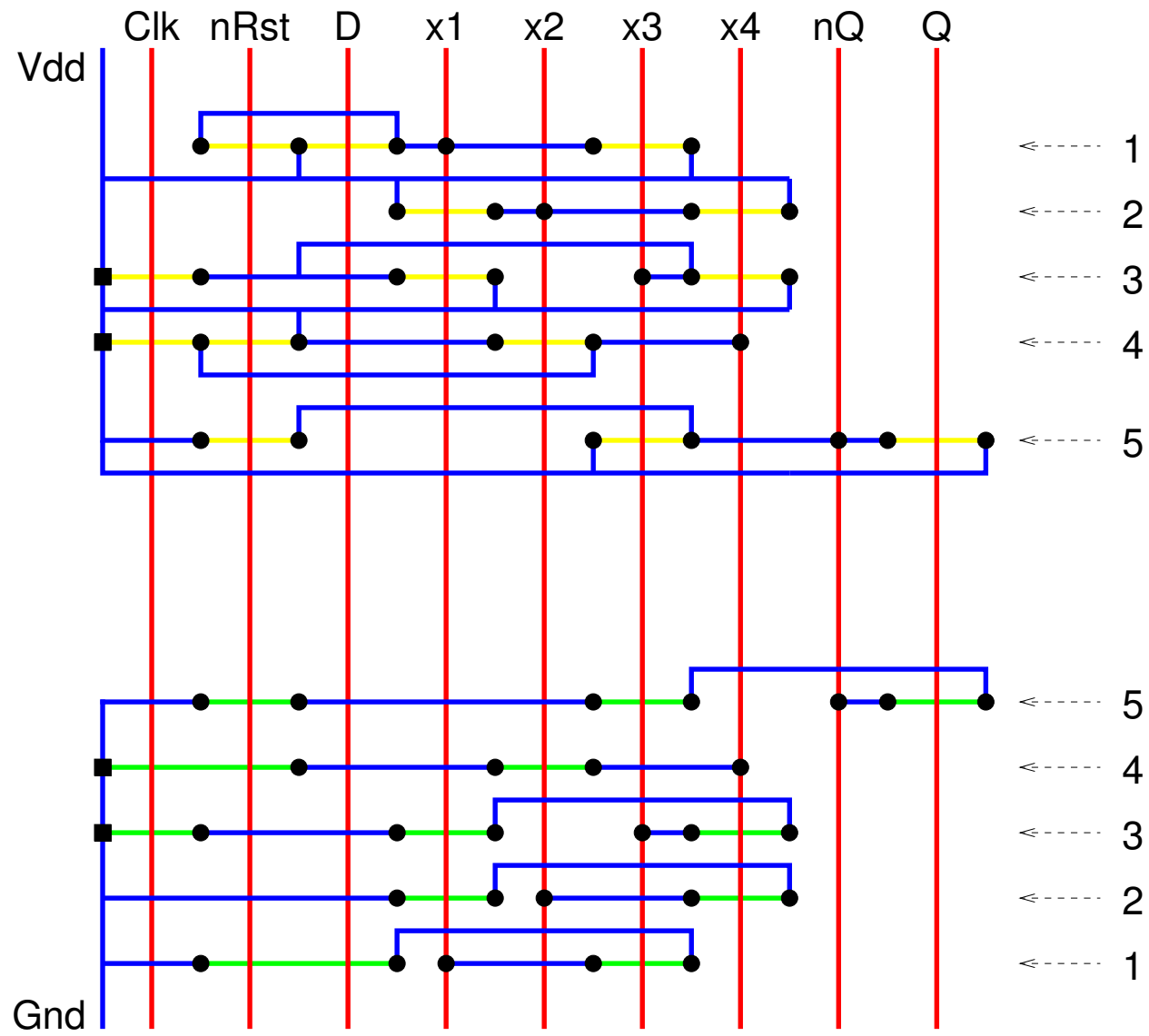


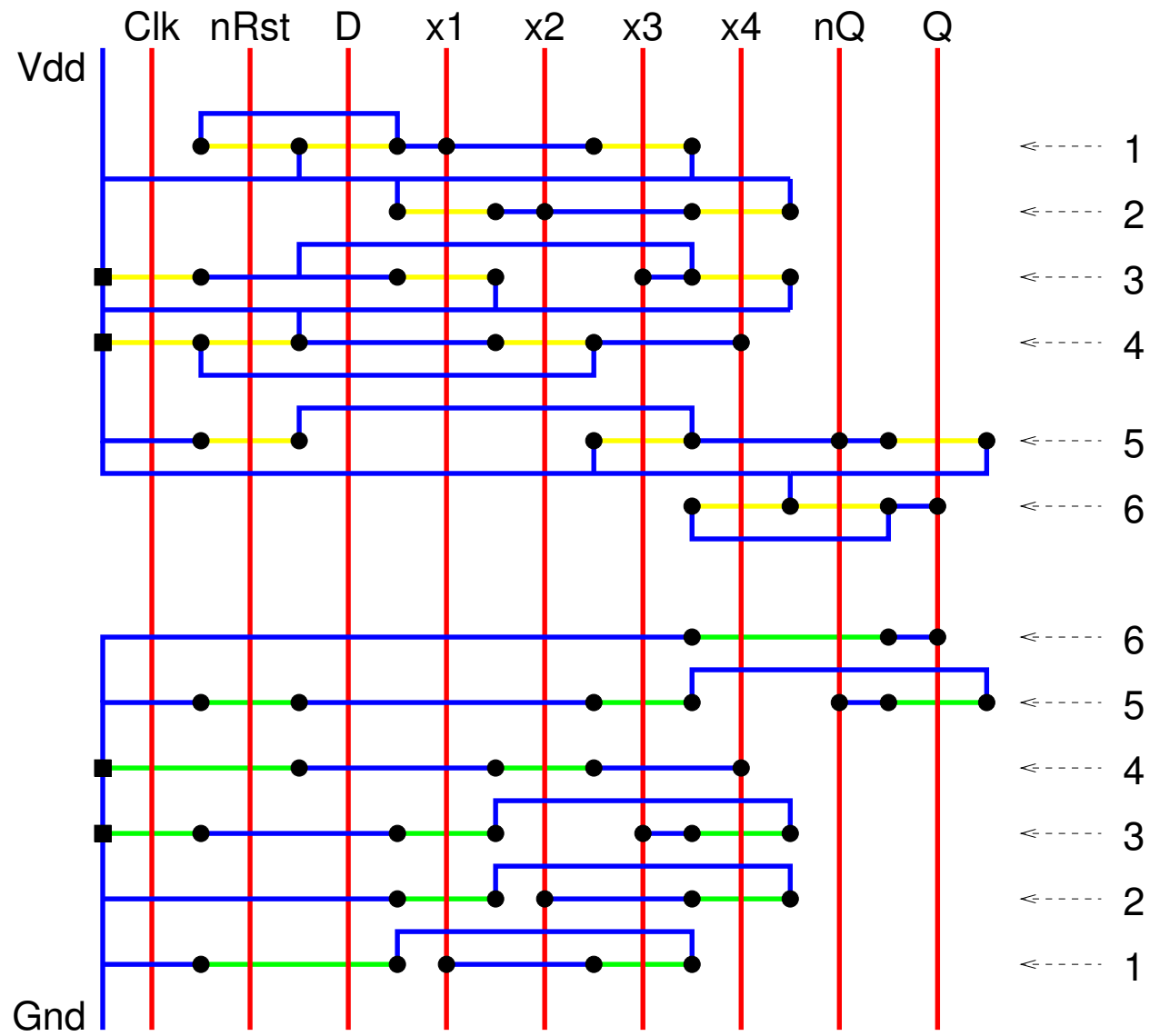


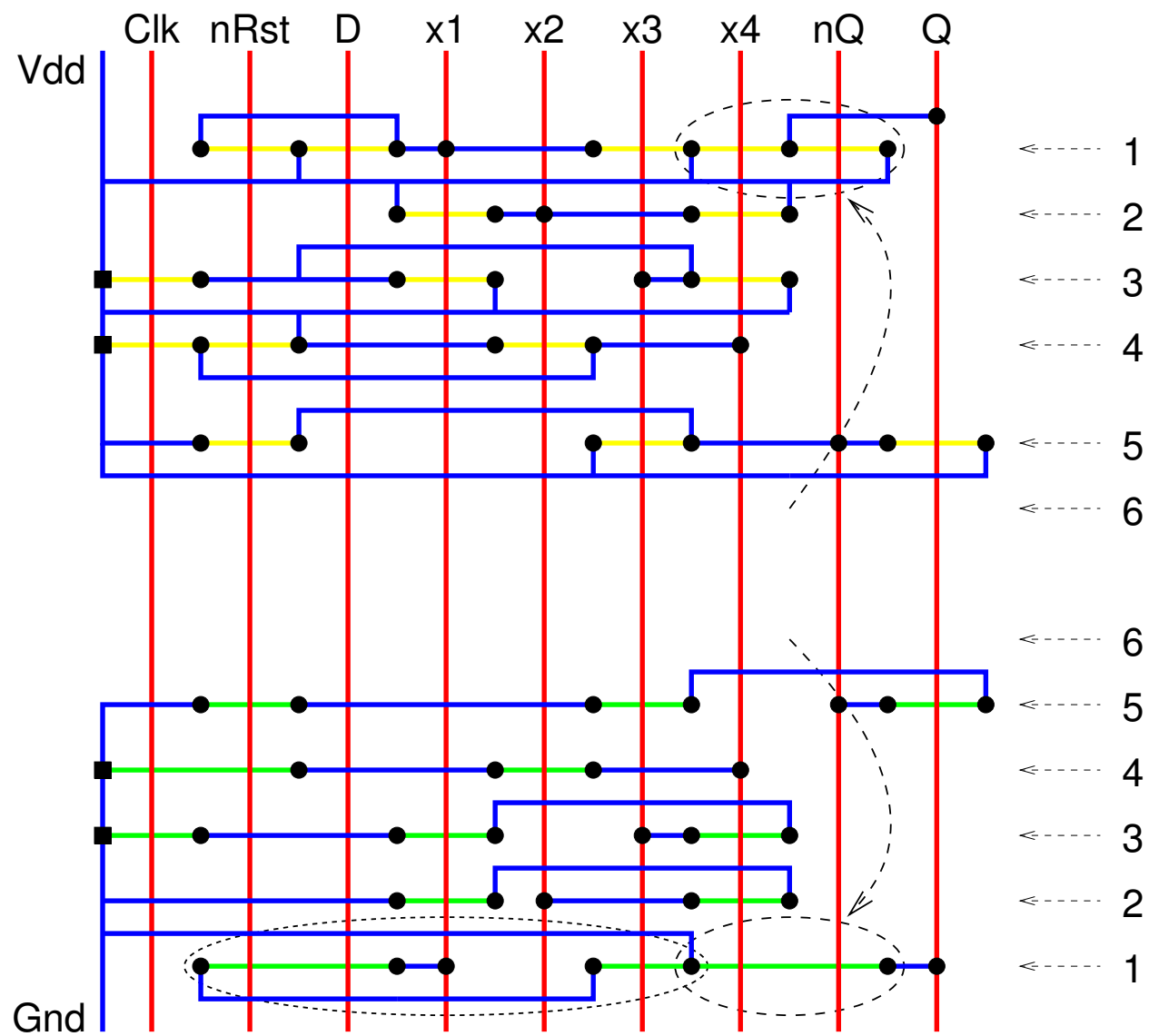












# Cell Design Choices

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- Line of Diffusion – Euler Path

The line of diffusion approach to cell design, backed up by investigation of Euler paths, leads to efficient layout of small cells.

- Gate Matrix<sup>1</sup>

Where cells are more complex and in particular when there are multiple transistors sharing a common gate connection, gate matrix design will often give more efficient use of area.

- Complex Standard Cells

- - Mux, D-Type, Full Adder etc

- consider impact of tall gate matrix cells on space efficiency in simple cells.

- Full Custom Cells

- - Efficient sub-circuit design.

- e.g. Full custom ALU bitslice.

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<sup>1</sup>note that partial Euler paths play an important part in efficient Gate Matrix design.