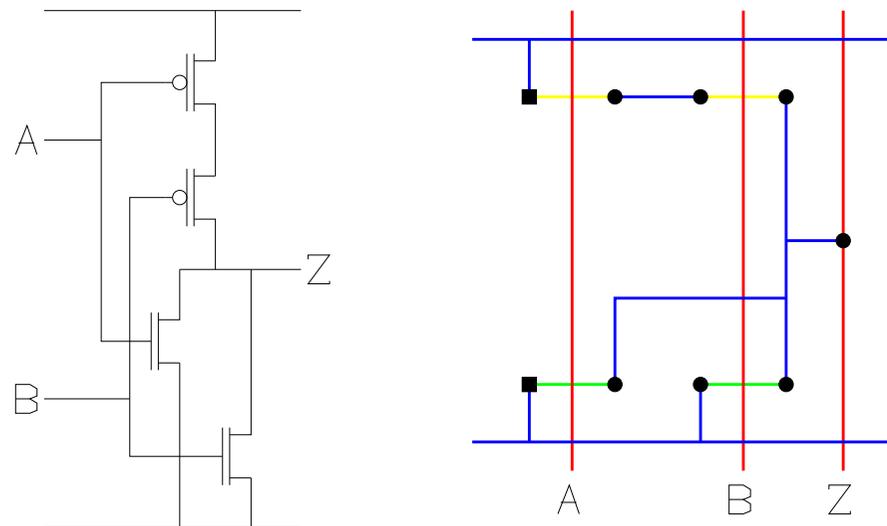


Digital CMOS Design

A logical approach to gate layout.

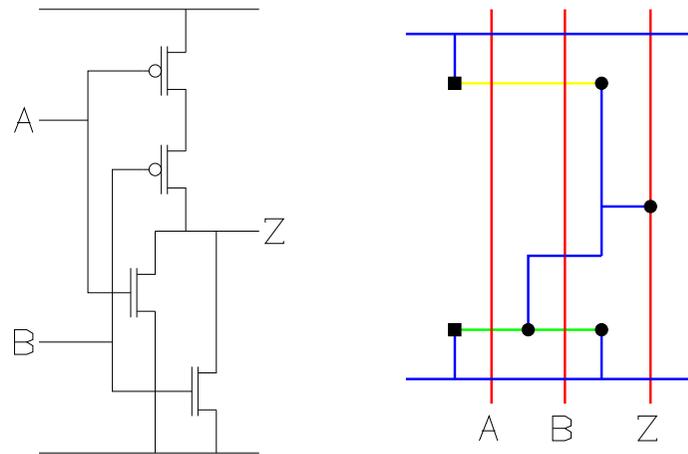
- *All complementary gates may be designed using a single row of n-transistors above or below a single row of p-transistors, aligned at common gate connections.*



Digital CMOS Design

Euler Path

- For the majority of these gates we can find an arrangement of transistors such that we can butt adjoining transistors.
 - Careful selection of transistor ordering.
 - Careful orientation of transistor source and drain.
- Referred to as *line of diffusion*.



Digital CMOS Design

Finding an Euler Path

Computer Algorithms

- It is relatively easy for a computer to consider all possible arrangements of transistors in search of a suitable Euler path.

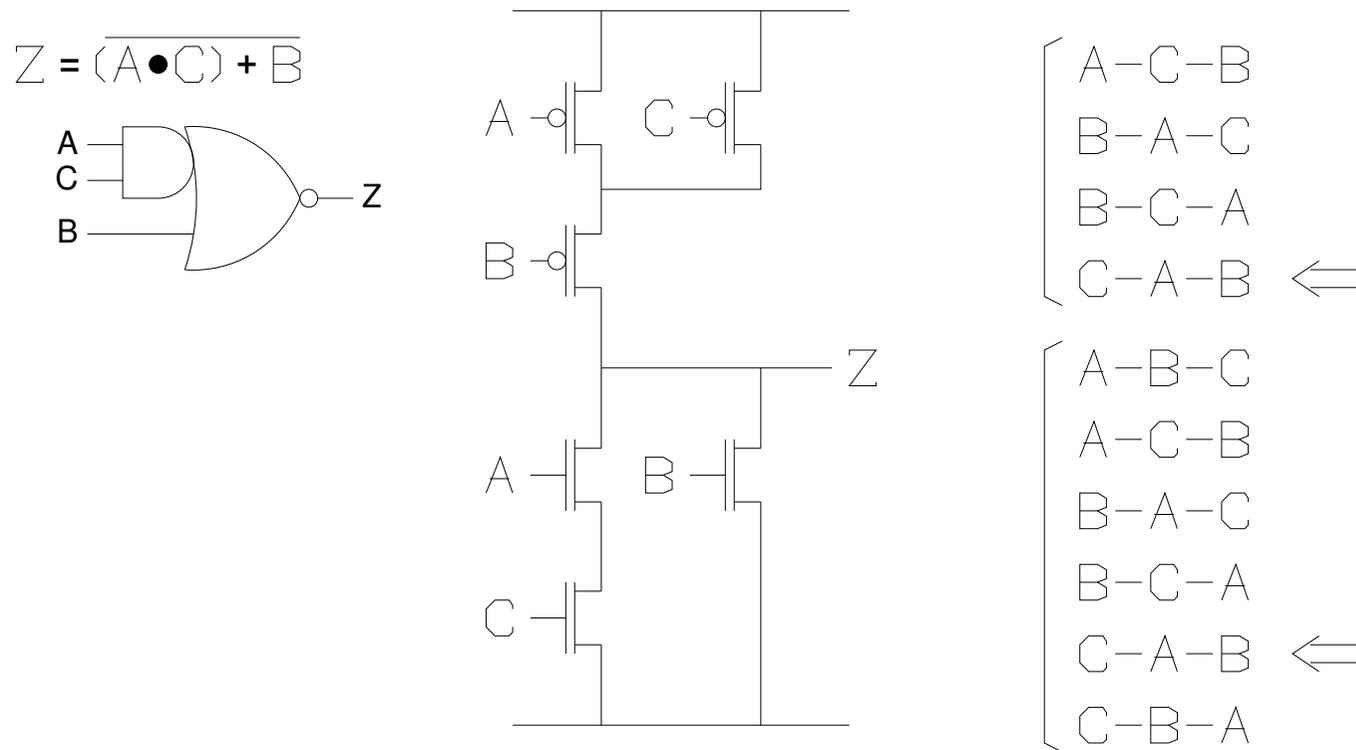
This is not so easy for the human designer.

One Human Algorithm

- Find a path which passes through all n-transistors exactly once.
- Express the path in terms of the gate connections.
- Is it possible to follow a similarly labelled path through the p-transistors?
 - Yes – you've succeeded.
 - No – try again (you may like to try a p path first this time).

Digital CMOS Design

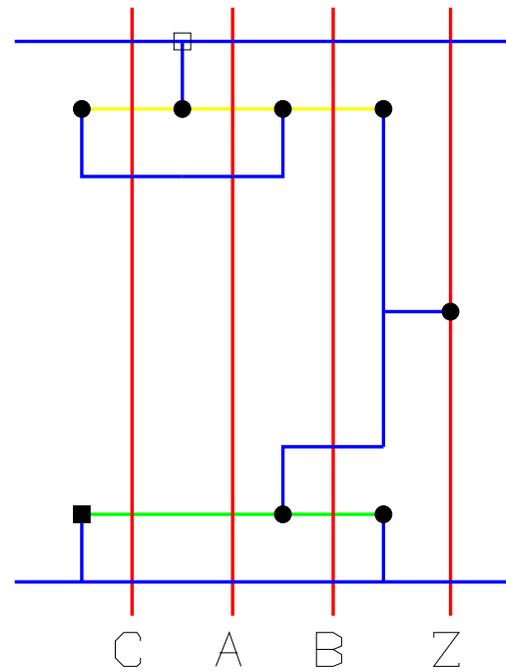
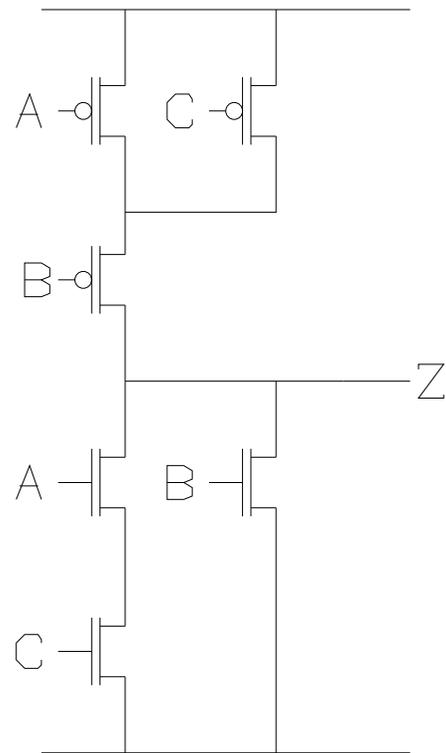
Finding an Euler Path



Here there are four possible Euler paths.

Digital CMOS Design

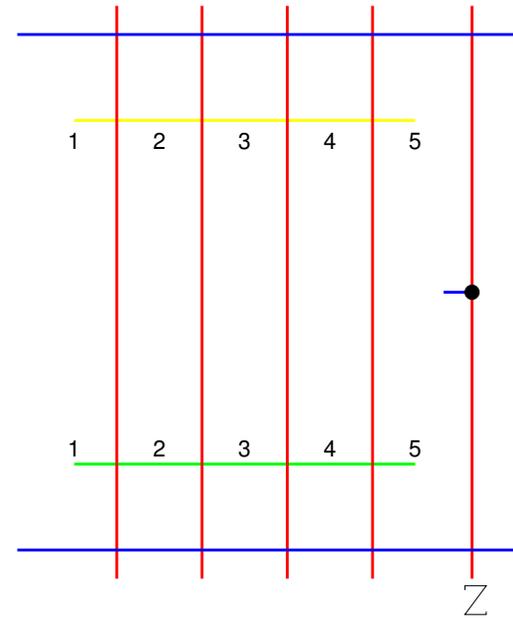
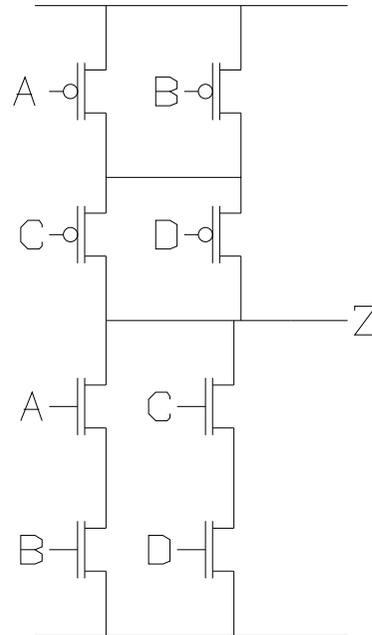
Finding an Euler Path



Digital CMOS Design

Euler Path Example

$$Z = \overline{(A \bullet B) + (C \bullet D)}$$



1. Find Euler path
2. Label poly columns
3. Route power nodes
4. Route output node
5. Route remaining nodes
6. Add taps¹ for PMOS and NMOS

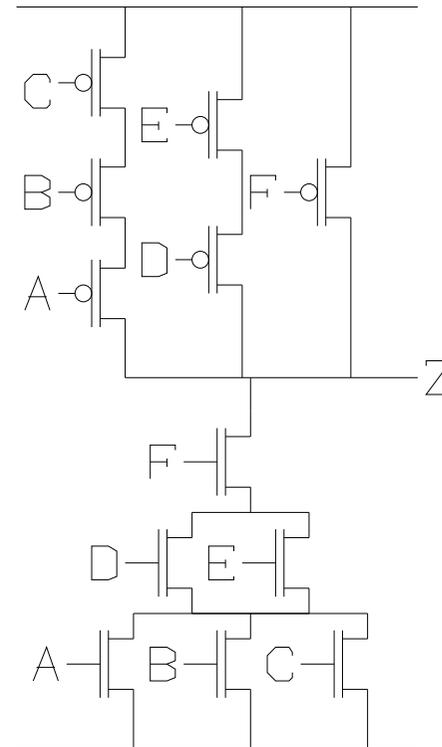
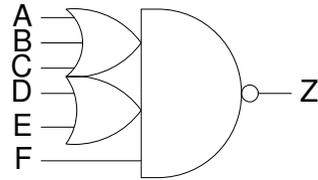
A combined contact and tap, \blacksquare , may be used only where a power contact exists at the end of a line of diffusion. Where this is not the case a simple tap, \blacksquare , should be used.

¹1 tap is good for about 6 transistors – insufficient taps may leave a chip vulnerable to latch-up

Digital CMOS Design

Finding an Euler Path

$$Z = \overline{(A+B+C) \cdot (D+E) \cdot F}$$

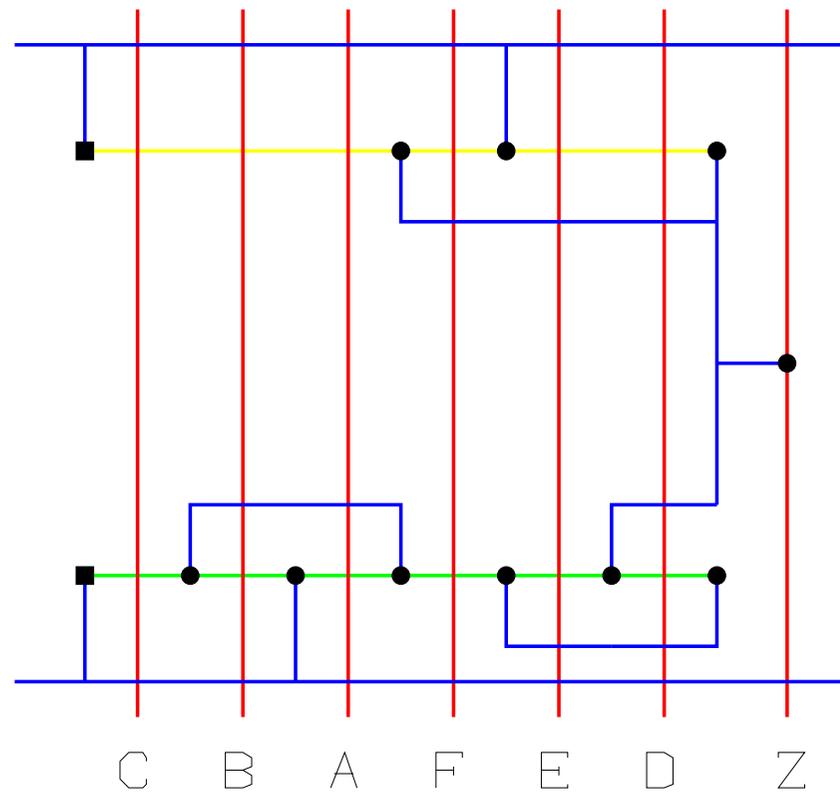
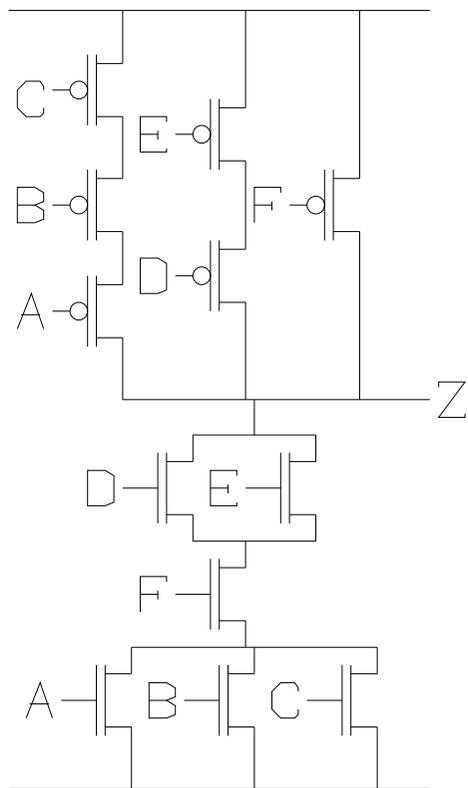


No possible path through n-transistors!

Digital CMOS Design

Finding an Euler Path

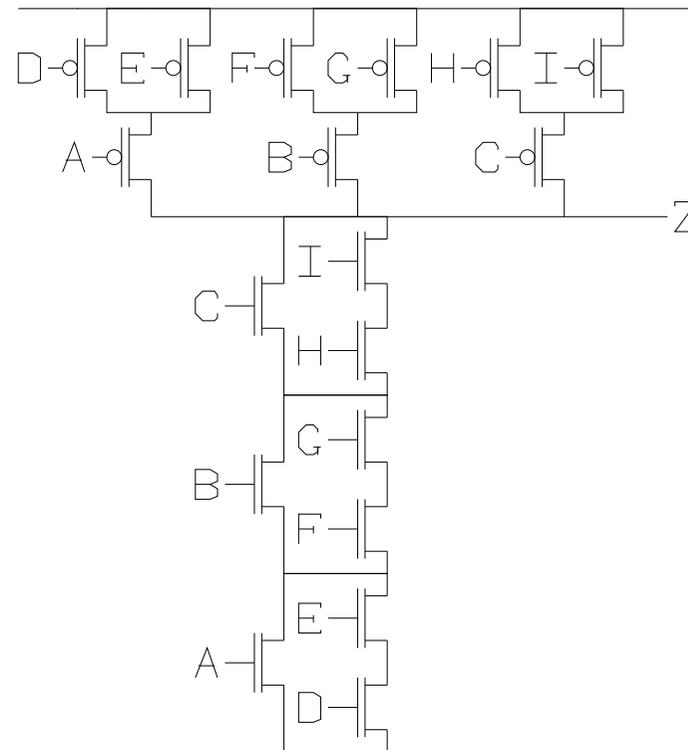
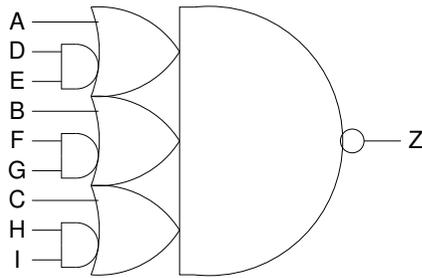
$$Z = \overline{(A+B+C)} \bullet (D+E) \bullet \overline{F}$$



Digital CMOS Design

Finding an Euler Path

$$Z = \overline{(A + (D \cdot E)) \cdot (B + (F \cdot G)) \cdot (C + (H \cdot I))}$$



No possible path through p-transistors.
No re-arrangement will create a solution!