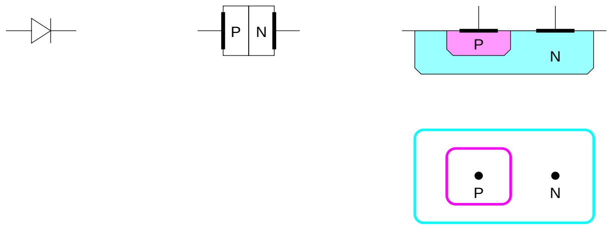
Diodes and Bipolar Transistors

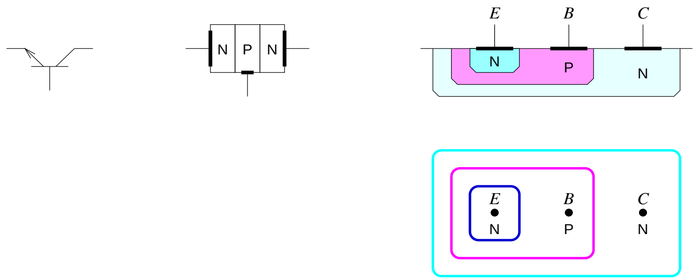
Diode



- Ideal structure - 1D
- Real structure - 3D
- Depth controlled implants.

Diodes and Bipolar Transistors

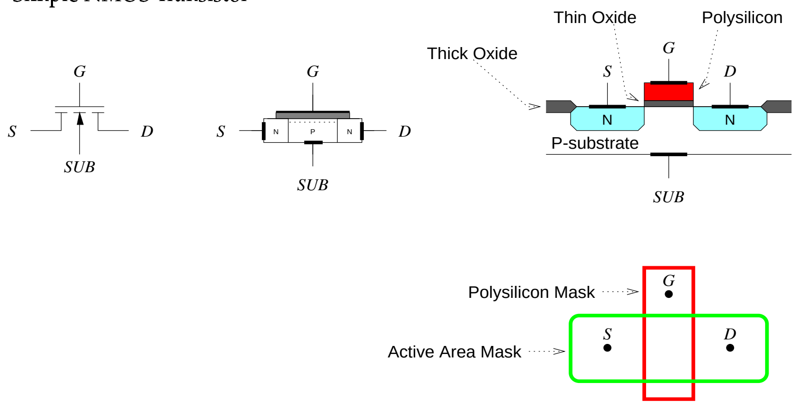
NPN Transistor



- Two n-type implants.

MOS Transistors

Simple NMOS Transistor

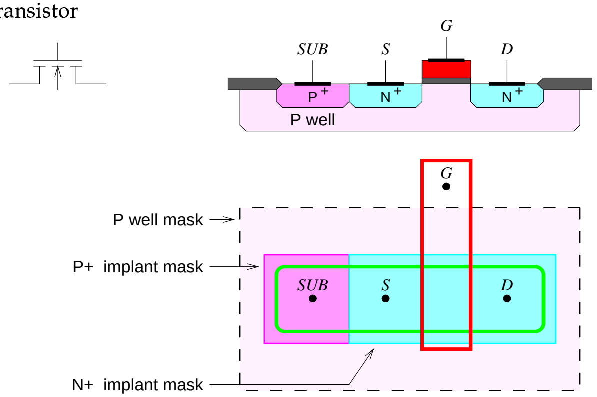


Simple NMOS Transistor

- Active Area mask defines extent of *Thick Oxide*.
- Polysilicon mask also controls extent of *Thin Oxide* (alias *Gate Oxide*).
- N-type implant has no extra mask.
  - It is blocked by thick oxide and by polysilicon.
  - The implant is *Self Aligned*.
- Substrate connection is to bottom of wafer.
  - All substrates to ground.
- Gate connection not above transistor area.
  - Design Rule.

MOS Transistors

NMOS Transistor

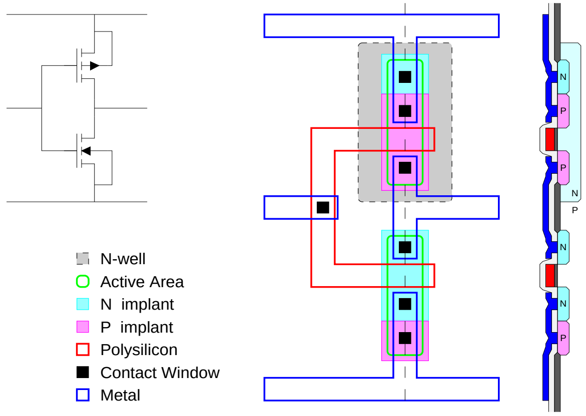


NMOS Transistor

Where it is not suitable for substrate connections to be shared, a more complex process is used.

- Five masks must be used to define the transistor:
  - P Well
  - Active Area
  - Polysilicon
  - N+ implant
  - P+ implant
- P Well, for isolation.
- Top *substrate* connection.
- P+/N+ implants produce good *ohmic* contacts.

CMOS Inverter

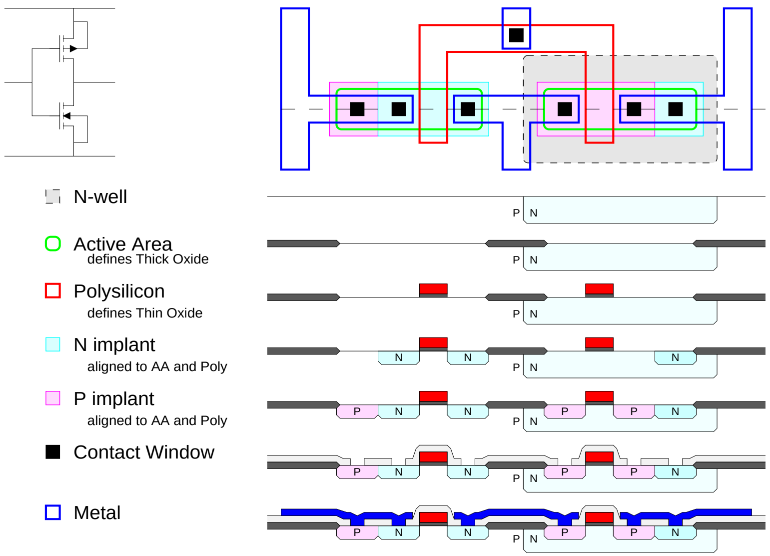


CMOS Inverter

- The process described here is an *N Well process* since it has only an N Well.

  P Well and Twin Tub processes also exist.
- Note that the P-N junction between chip substrate and N Well will remain reverse biased.

  Thus the transistors remain isolated.
- N implant defines NMOS source/drain and PMOS substrate contact.
- P implant defines PMOS source/drain and NMOS substrate contact.


N-well
Active Area
defines Thick Oxide
Polysilicon
defines Thin Oxide
N implant
aligned to AA and Poly
P implant
aligned to AA and Poly
Contact Window
Metal

3009