System Design Choices

- Programmable Logic
  - PLD
    e.g. PAL 22V10, ICT PEEL22CV10, Lattice ispGAL22V10
  - Field Programmable Gate Array (FPGA)
    e.g. Xilinx XC4013, Altera Cyclone EP1C12
- Semi-Custom Design
  - Mask Programmable Gate Array
    e.g. ECS CMOS Gate Array
    Altera HardCopy II structured ASICs
  - Standard Cell Design
    e.g. Alcatel Mietec MTC45000 0.35μm cell library
- Full Custom Design

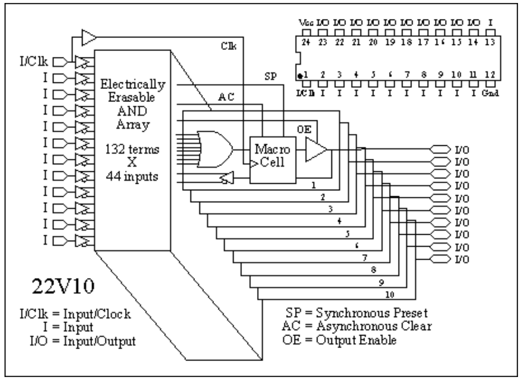
System Design Choices

START HERE

- Programmable Logic
  - Best possible design turnaround time
  - Cheapest for prototyping
  - Best time to market
  - Minimum skill required
- Semi-Custom Design
- Full Custom Design
  - Cheapest for mass production
  - Fastest
  - Lowest Power
  - Highest Density[1]
  - Most skill required

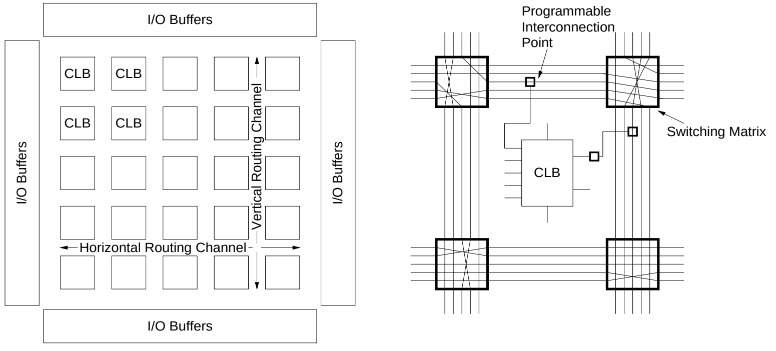
[1]optimization limited by speed/power/area trade off

Programmable Logic



- One time use - Fuse programmable.
- Reprogrammable - UV/Electrically Erasable.

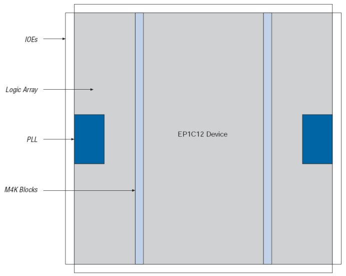
Field Programmable Gate Array – Xilinx XC4000

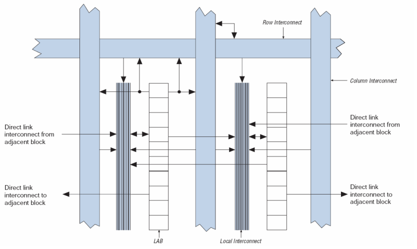


- Configurable Logic Blocks & I/O Blocks[2]
- Programmable Interconnect

[2]Xilinx XC4013 has 576 (24×24) CLBs and up to 192 (4×48) user I/O pins.

Field Programmable Gate Array – Altera Cyclone

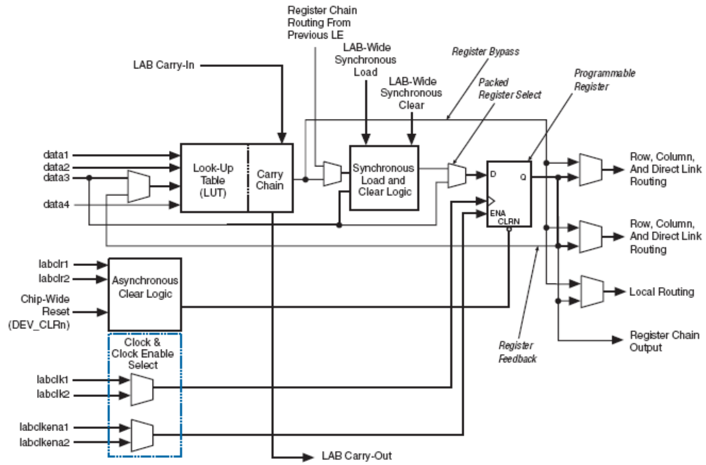




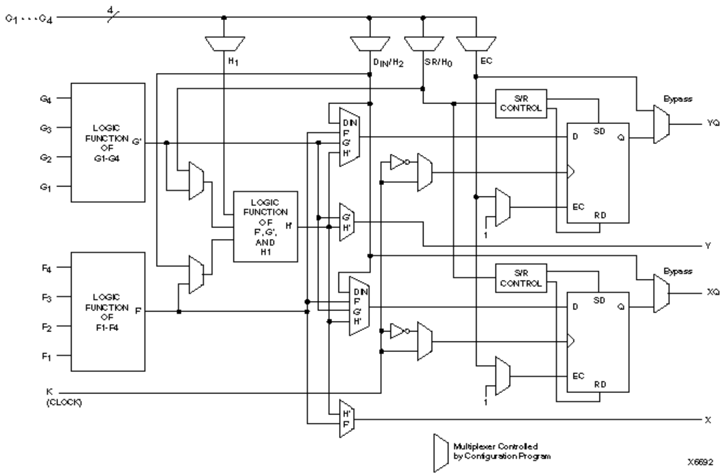
- Logic Array Blocks, M4K Ram Blocks & I/O Elements[3]
- Programmable Interconnect

[3] Altera Cyclone EP1C12 has 12060 Logic Elements (arranged as 1206 Logic Array Blocks) and and up to 249 user I/O pins.

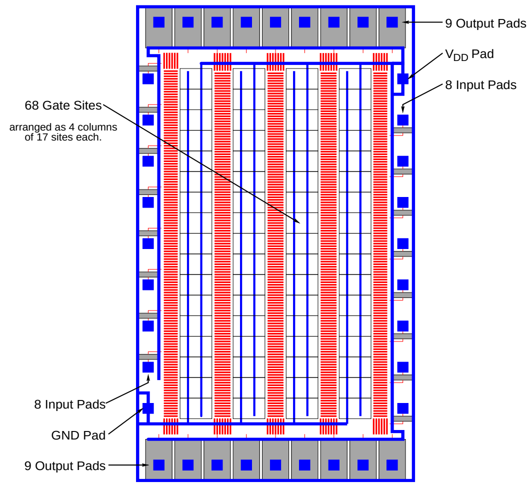
Field Programmable Gate Array – Altera Cyclone LE



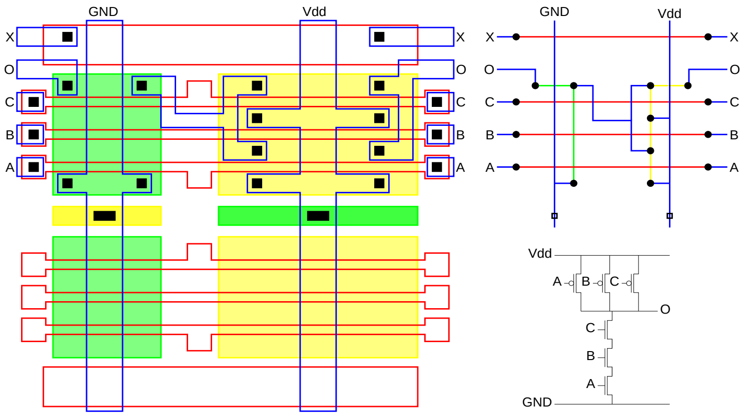
Field Programmable Gate Array – Xilinx XC4000 CLB



Mask Programmable Gate Array



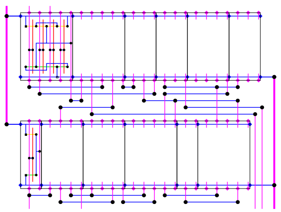
Mask Programmable Gate Array



- Customize Metal and Contact Window masks only.

Standard Cell Design

- Logic Functions



- Auto Generated Macro Blocks
  - PLA
  - ROM
  - RAM
- System Level Blocks
  - Microprocessor core[4]

[4]Will support System On Chip applications.

Full Custom

All design styles need full custom designers

- to design the base programmable logic chips
- to design building blocks for semi-custom

Where large ASICs use full custom techniques they are likely to be used alongside semi-custom techniques.

e.g. Hand-held computer game chip

- Full custom bitslice datapath
  hand crafted for optimum area efficiency and low power consumption
- Standard cell controller
- Macro block RAM, ROM