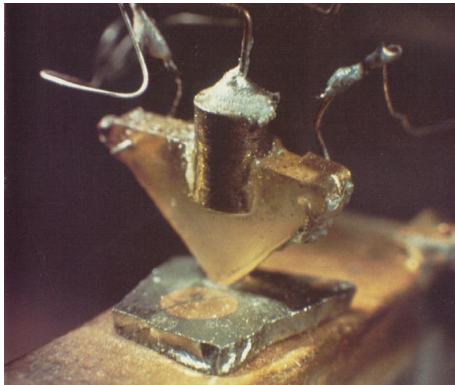
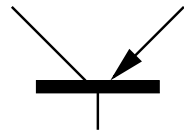


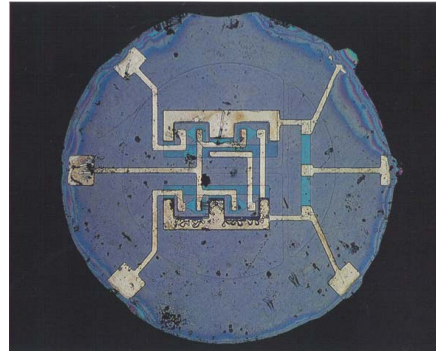
1947 Point Contact transistor



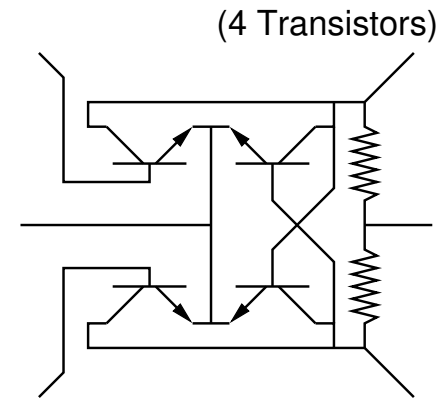
Source: Bell Labs



1961 Fairchild Bipolar RTL RS Flip-Flop

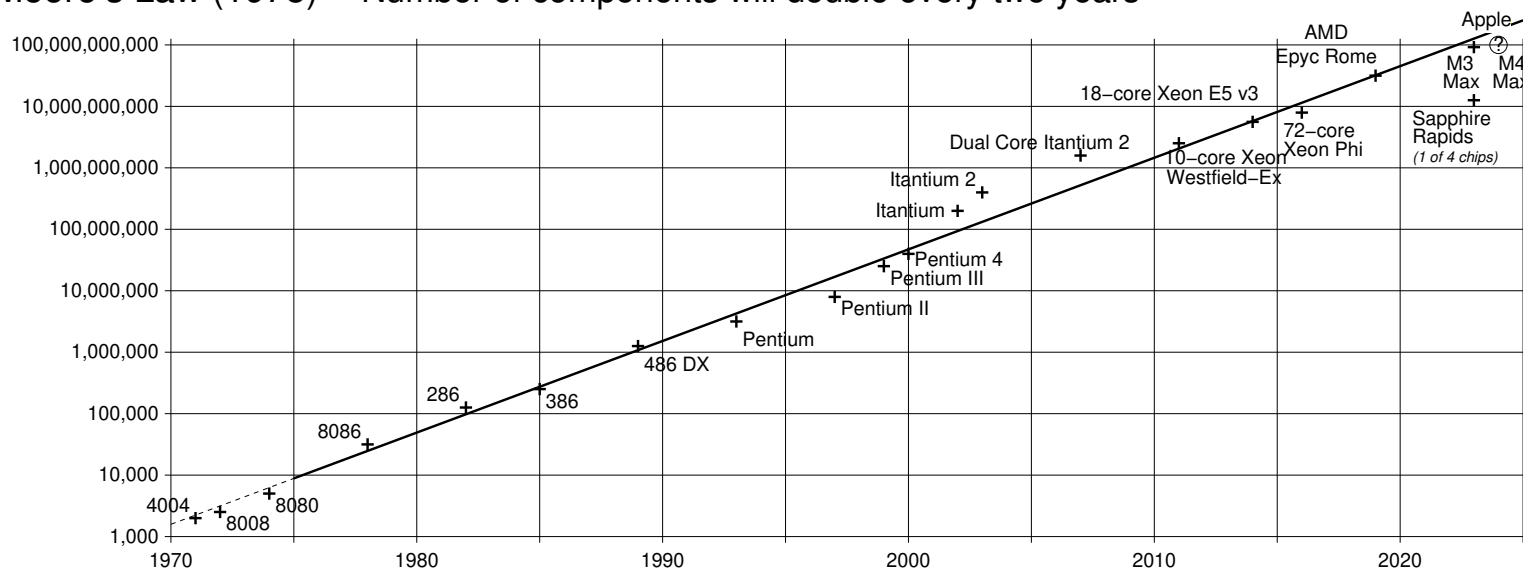


Source: Fairchild



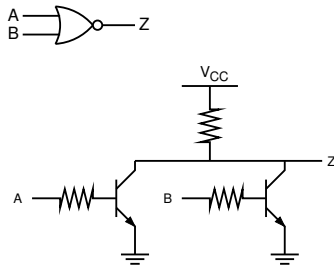
Moore's Law (1965) Number of components has doubled every year and will continue to do so until 1975

Moore's Law (1975) Number of components will double every two years

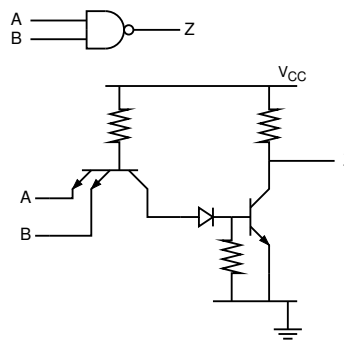


Self-fulfilling
Prophecy

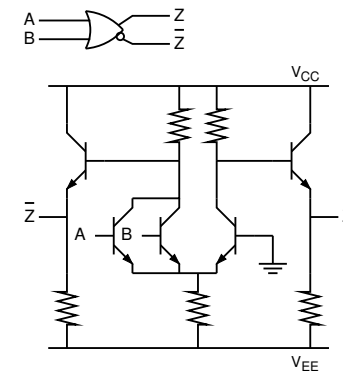
RTL NOR Gate



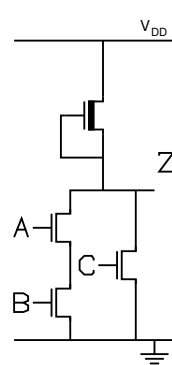
TTL NAND Gate



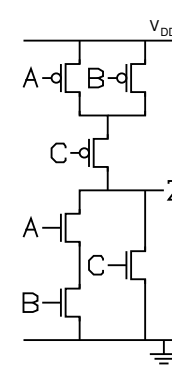
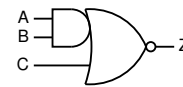
ECL OR/NOR Gate



NMOS Compound Gate



CMOS Compound Gate



- Bipolar Transistors with Resistors - MSI/LSI

RTL - NOR

TTL - NAND

ECL - OR/NOR

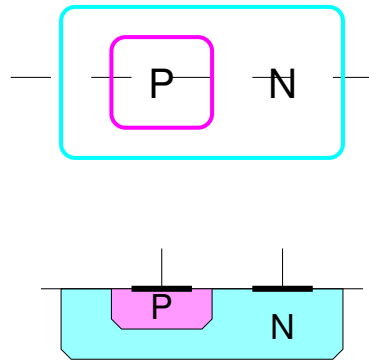
- MOS Transistors (no resistors) - VLSI

NMOS

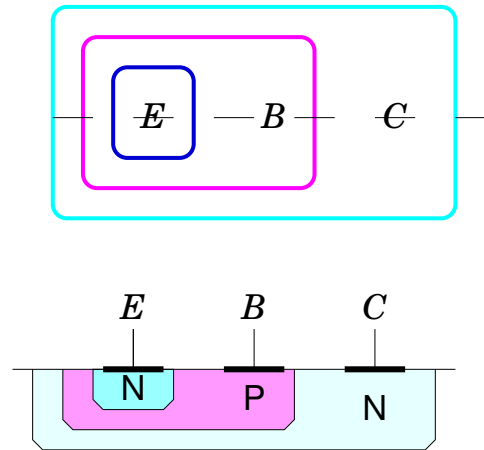
CMOS - No static power!

Both allow construction of NOR, NAND & Compound gate (always inverting)

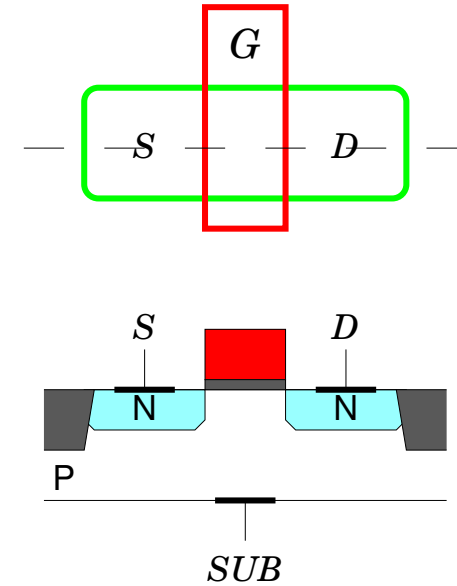
Diode



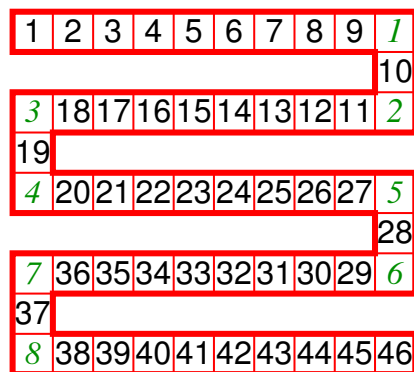
NPN Transistor



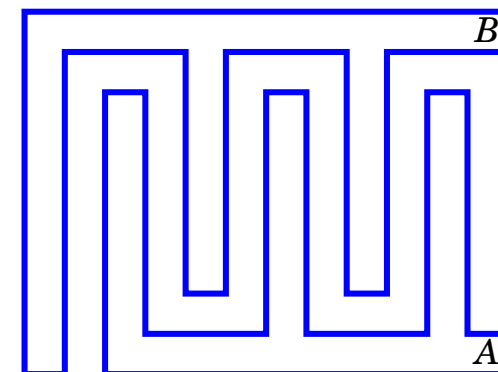
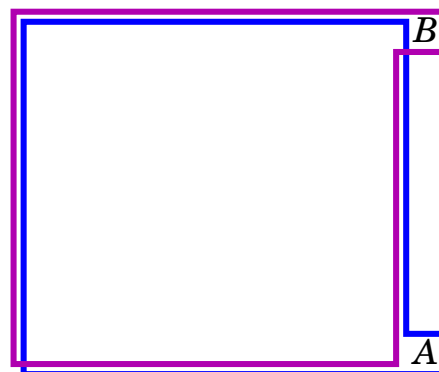
NMOS Enhancement transistor
NMOS Process



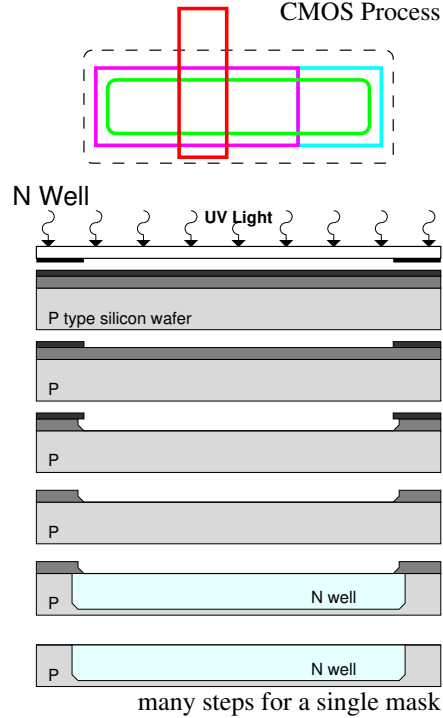
Resistor



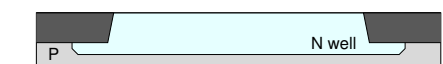
Capacitors



PMOS Enhancement transistor
CMOS Process



Active Area



Polysilicon



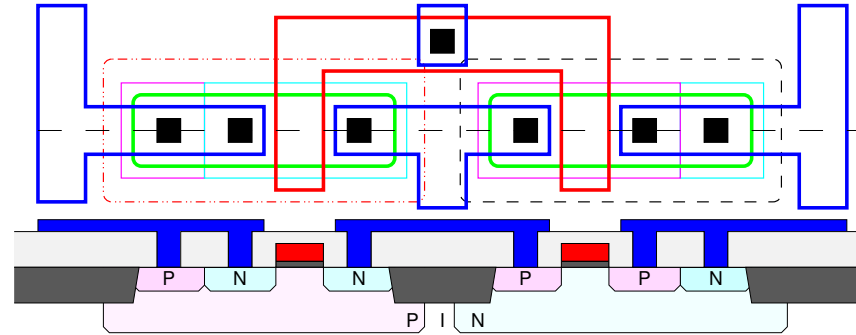
P+ Implant



N+ Implant

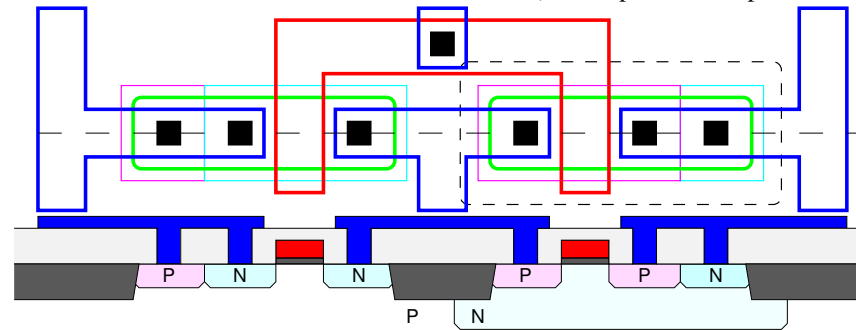


CMOS Inverter



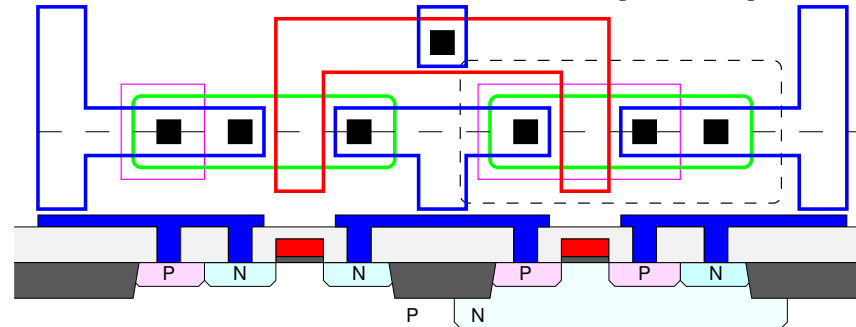
Twin Tub CMOS Process

CMOS Inverter



N-Well CMOS Processes (with explicit N+ implant mask)

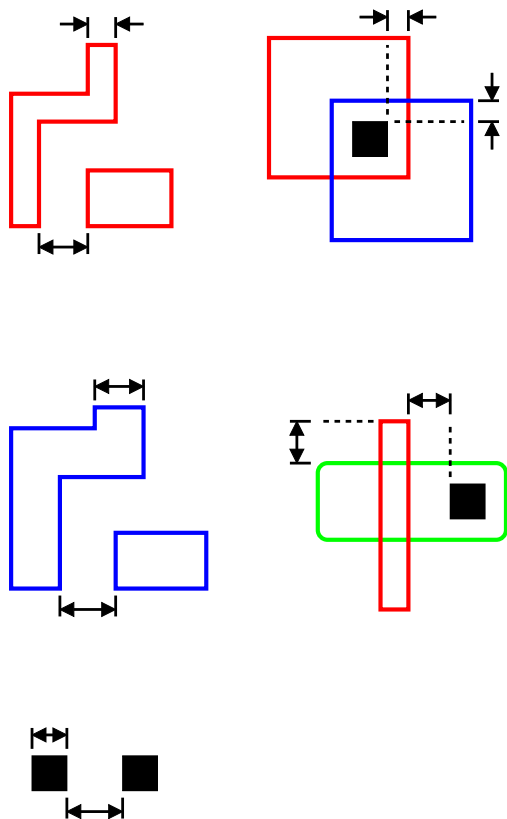
CMOS Inverter



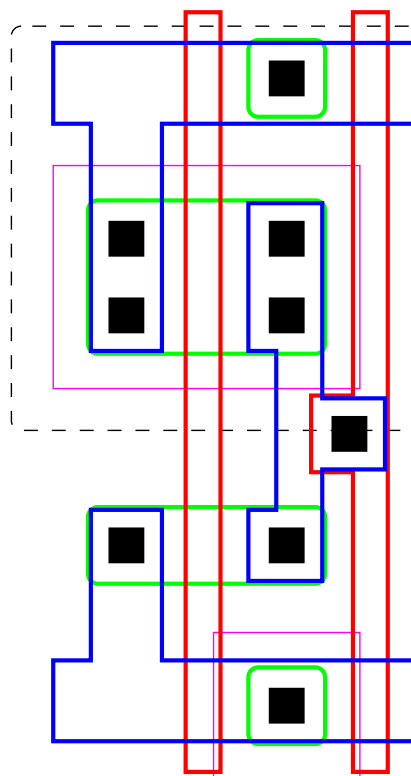
N-Well CMOS Processes (without explicit N+ implant mask)

Features may be determined by a number of masks
e.g. NMOS source drain: ActiveArea AND NOT(NWell OR Poly OR PImplant)

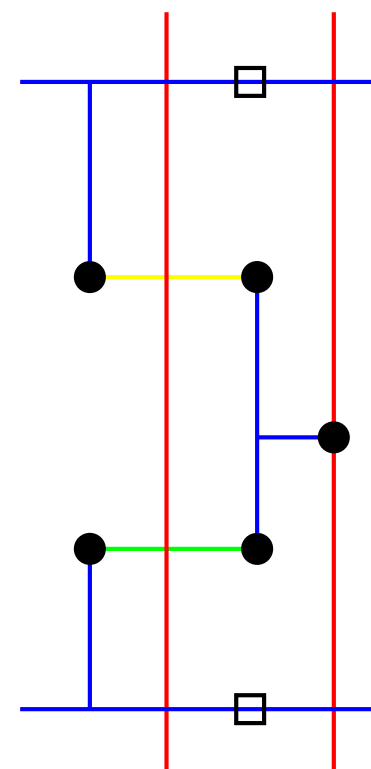
Design Rules – width, separation, overlap



Optimised Mask Layout

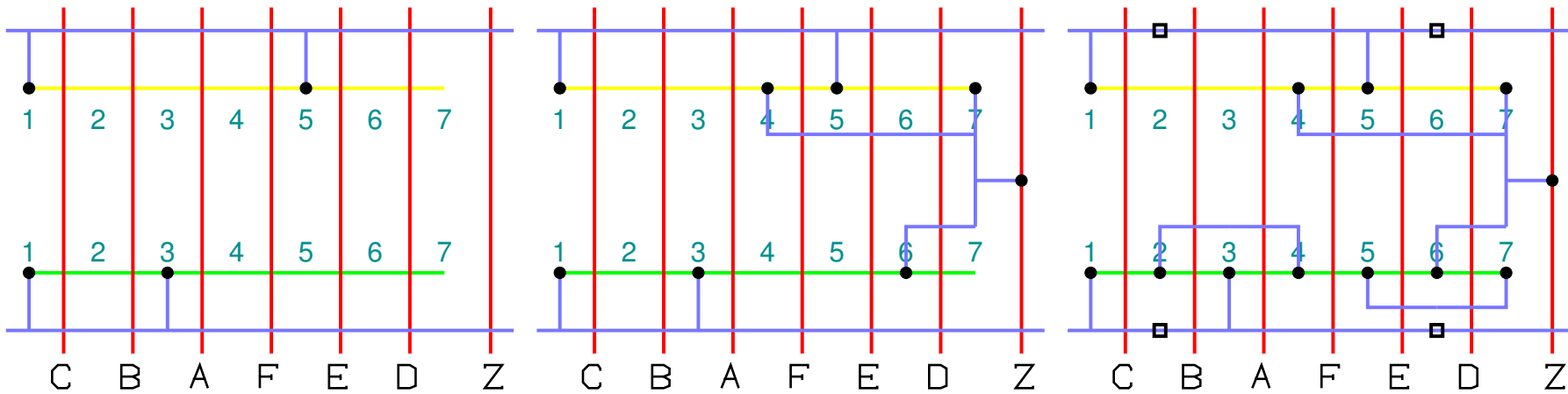
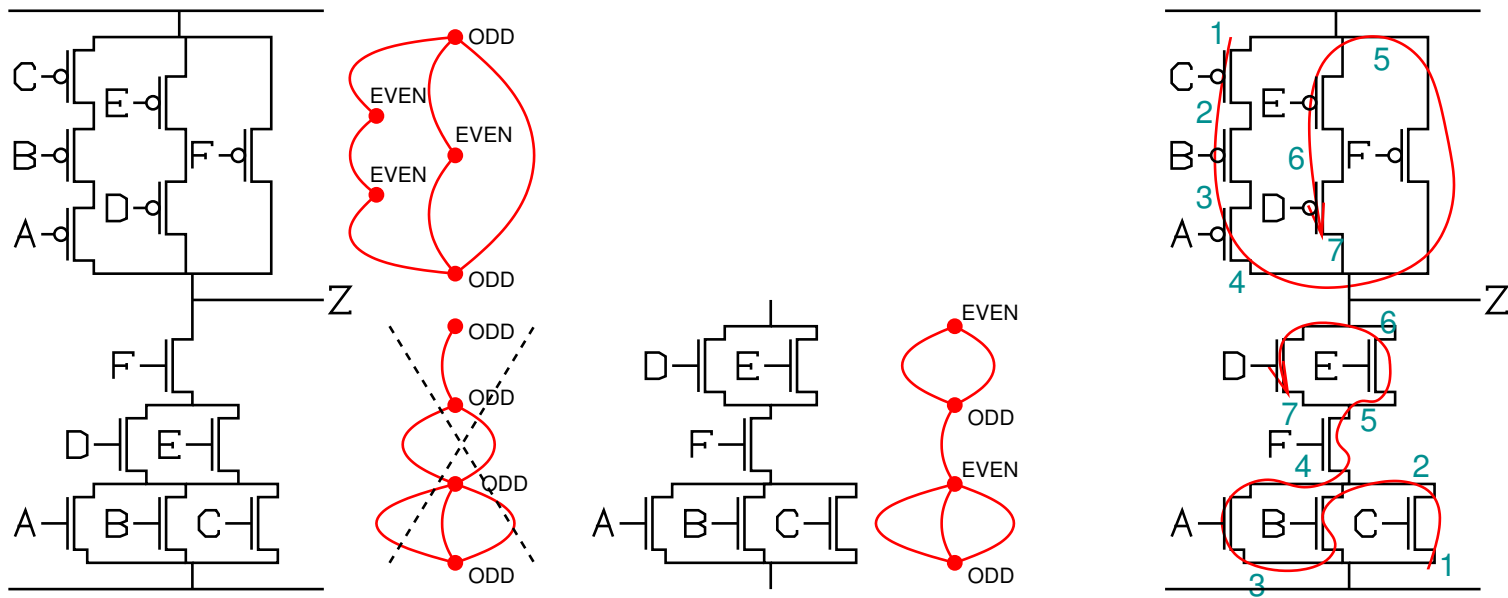


Equivalent Stick Diagram



- Metal
- Polysilicon
- N+
- P+
- Contact
- Tap
- Combined contact & tap

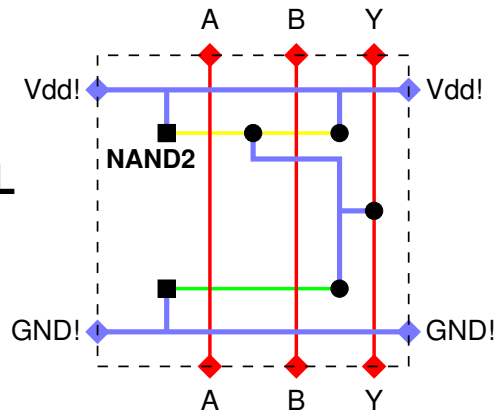
Investigation of Euler paths leads to more efficient layout*



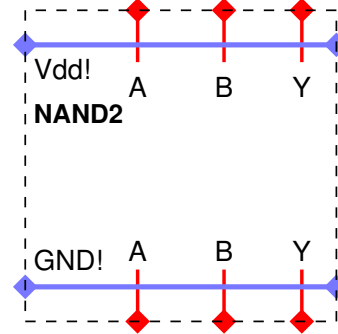
*not all gates will support a common Euler path for both PMOS and NMOS

1 METAL LAYER

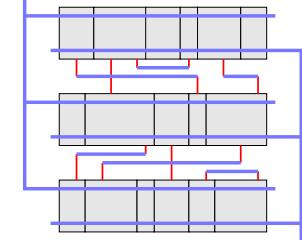
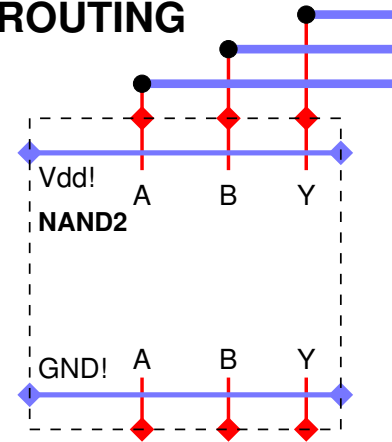
LAYOUT



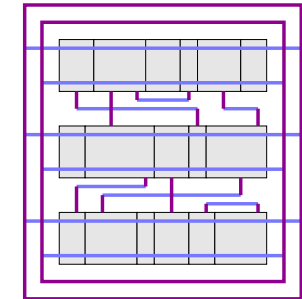
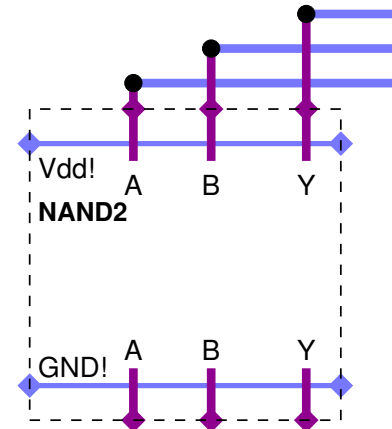
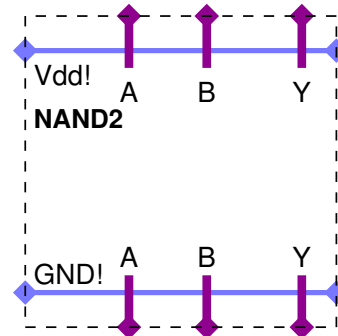
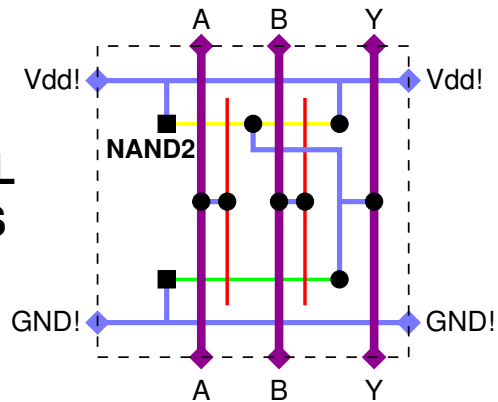
ABSTRACT



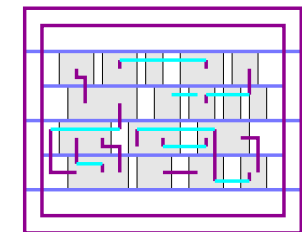
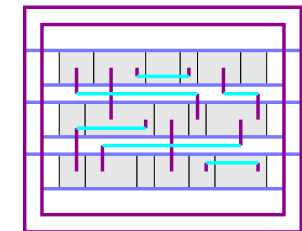
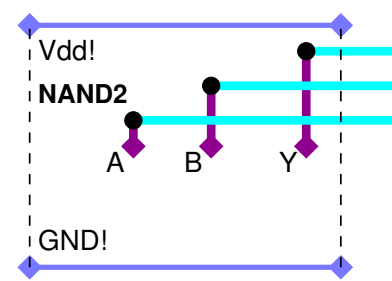
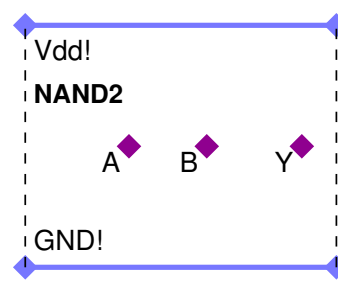
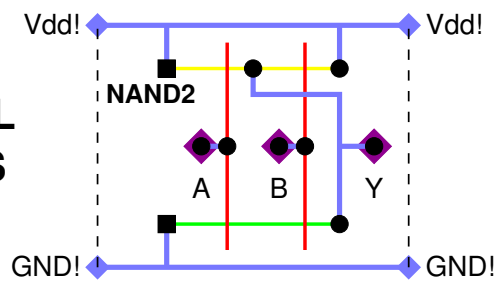
ROUTING



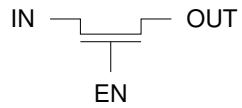
2 METAL LAYERS



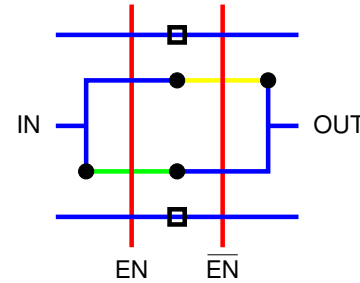
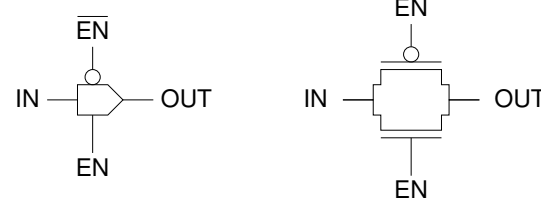
3 METAL LAYERS



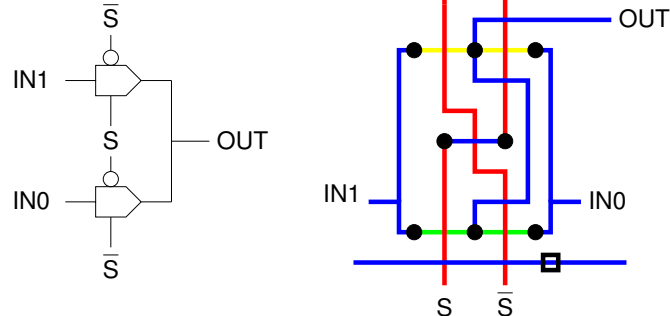
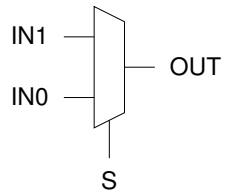
Pass Transistor



CMOS Transmission Gate



Transmission Gate Multiplexor

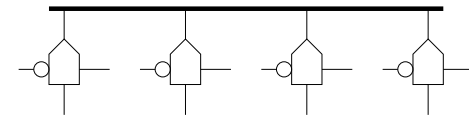


*note distinctive polysilicon crossover

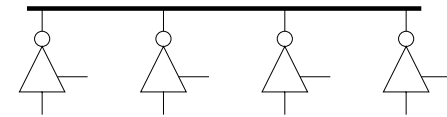
Tri-state gates are used for Multiplexing

Distributed Multiplexing

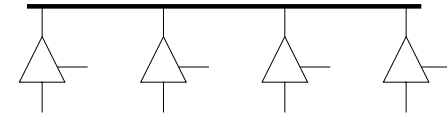
using transmission gates



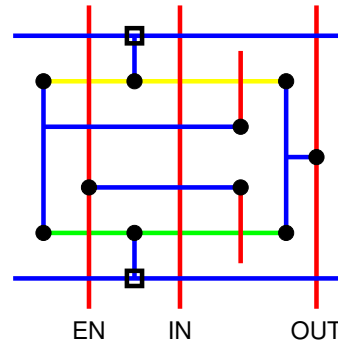
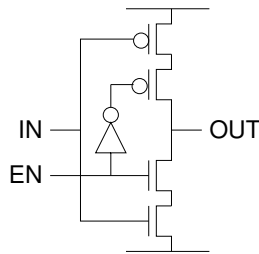
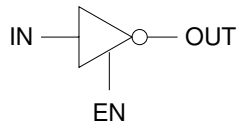
using tri-state inverters



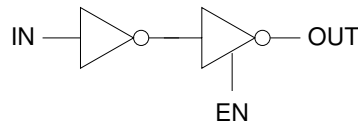
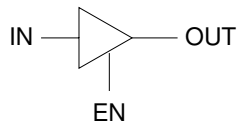
using tri-state buffers



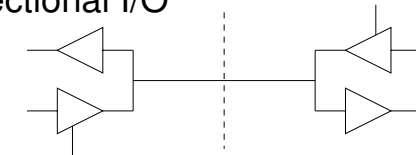
Tri-state Inverter



Tri-state Buffer

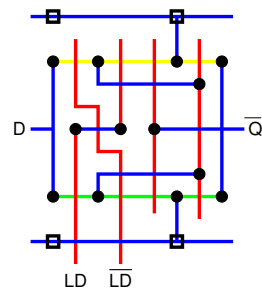
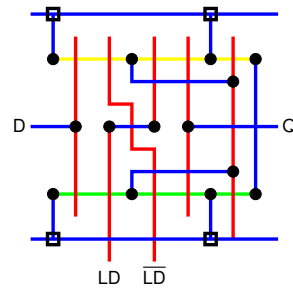
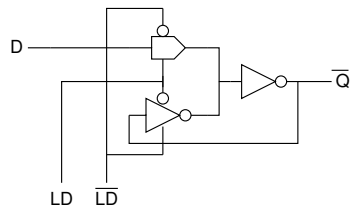
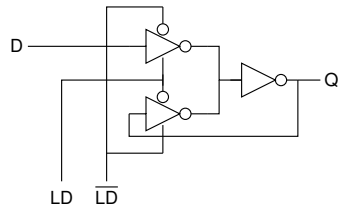


Bi-directional I/O

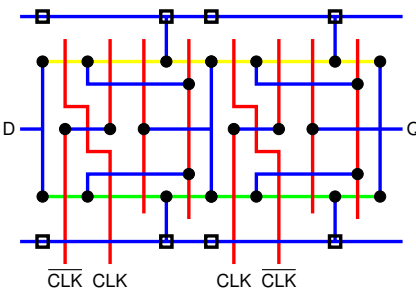
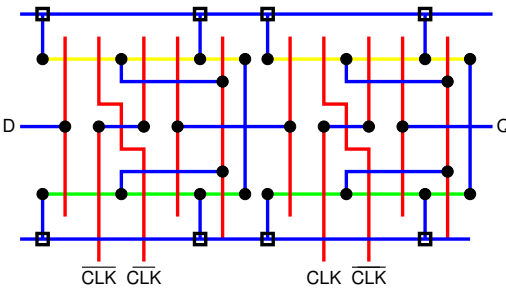
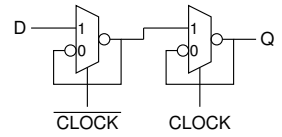
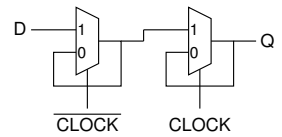


*this is another form of multiplexing

Latch

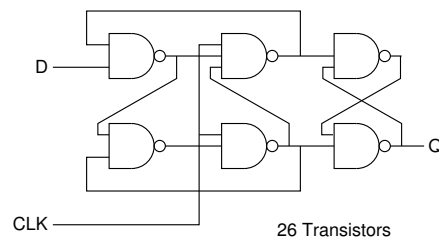


Master Slave D-Type Flip-Flop

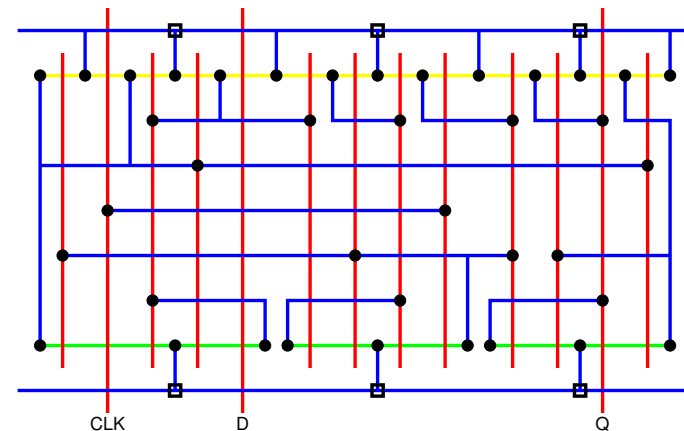


*multiplexor based latches and flip-flops include distinctive polysilicon crossover

Edge Triggered D-Type Flip-Flop

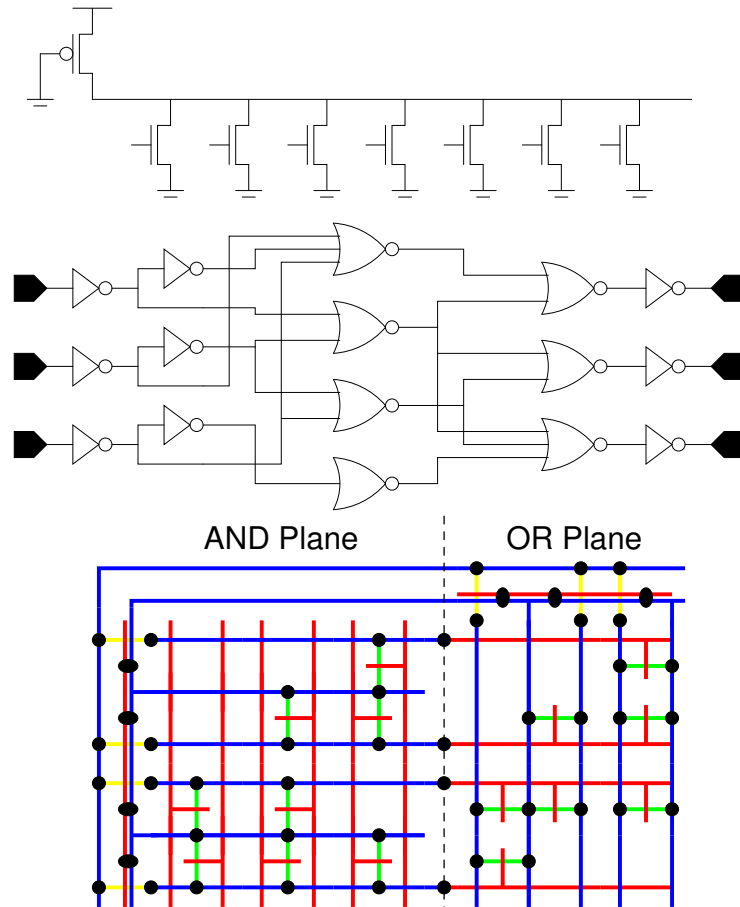


26 Transistors



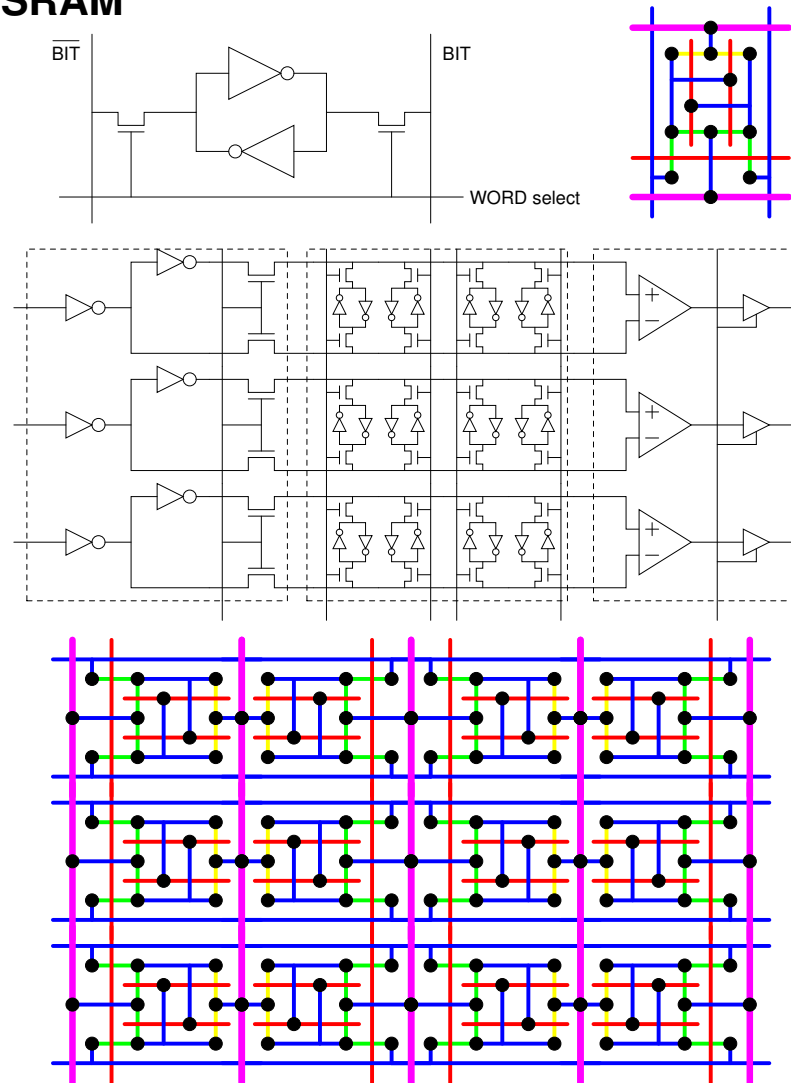
Euler path analysis is applied creatively to these multi-gate cells – gates are often linked via the common gnd/pwr node
Final layouts will be more complex where clock buffers, reset circuitry and metal 2 i/o are included

PLA and ROM



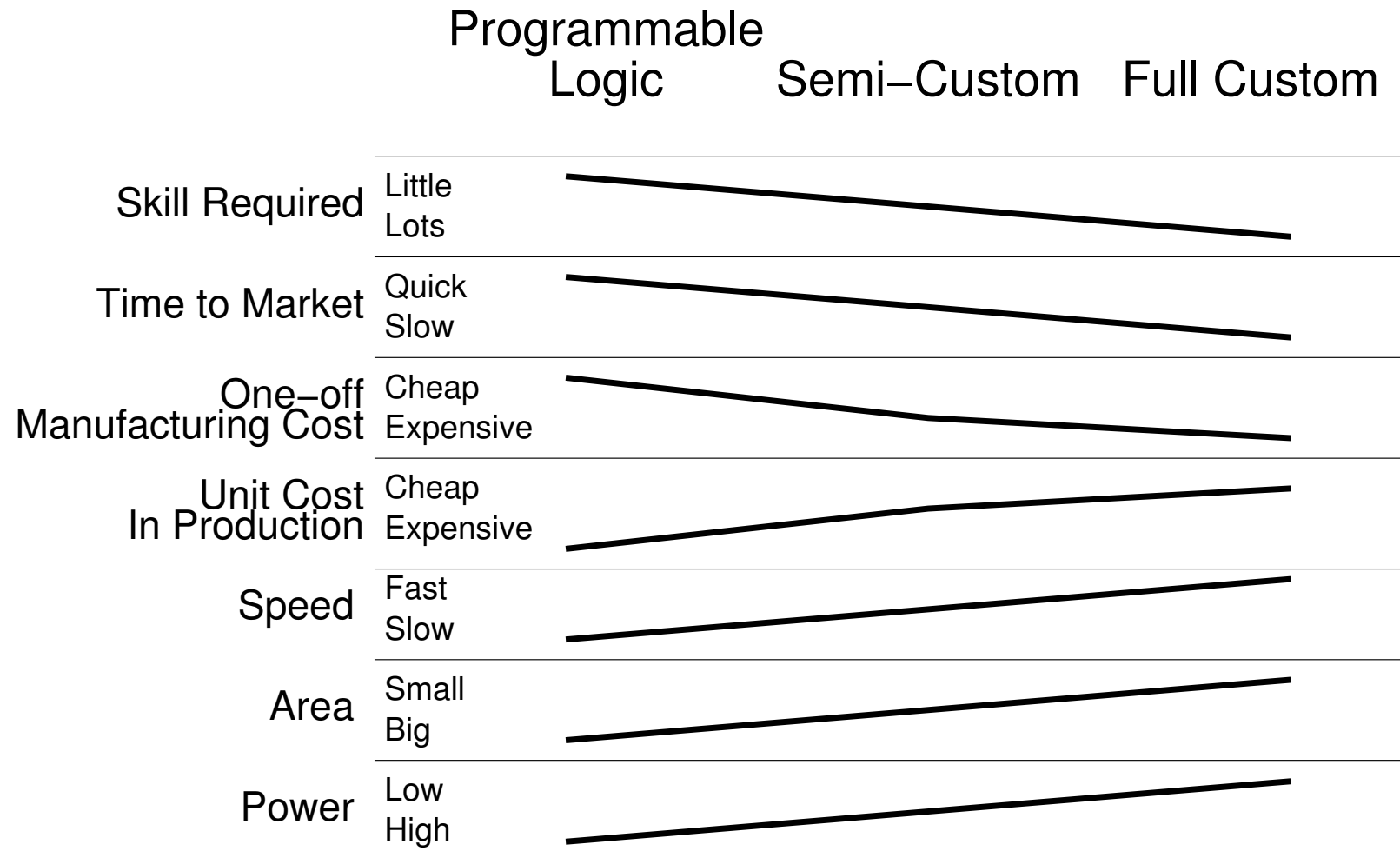
ROM is PLA with
fixed AND (decoder) plane
programmable OR (data) plane

SRAM



Cells are designed to butt together in two dimensions leading to efficient layout

PLA layout efficiency will depend on the actual function implemented (e.g. number of common product terms)



All design styles need full custom designers

A large ASIC (especially SoC) may mix Semi-Custom and Full Custom