

Digital CMOS Design

Taps

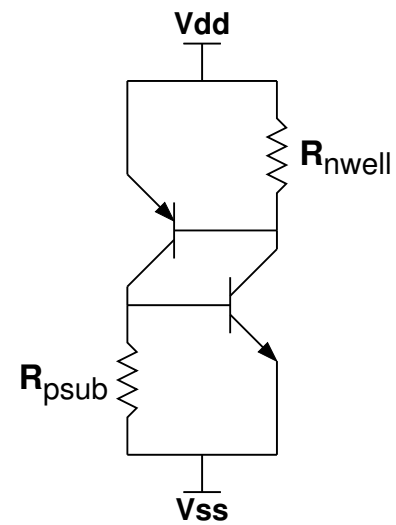
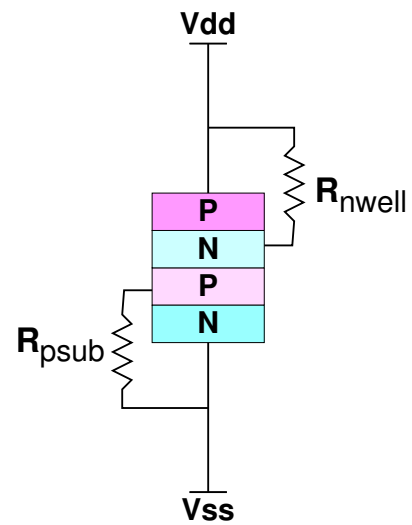
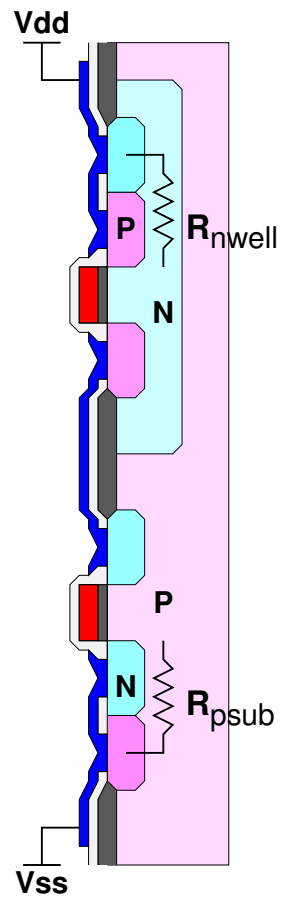
For simple functionality we require only one tap per N well and a single tap for the whole wafer substrate.¹ Unfortunately CMOS circuits can fail due to *Latch-up*, a condition in which the whole chip acts as a thyristor (PNPN) device in order to short Vdd to Vss.

The following (process independent) guidelines should be considered when deciding on a cell layout.

- Every well must have an appropriate tap.
- Every tap must be connected to a supply pad via unbroken metal.
- Taps should be placed as close to source connections as possible.
- Empirical rule: one tap for every 5-10 transistors.
- Layout N devices packed towards Vss and P devices packed towards Vdd.

¹Assuming an N well process.

Latch-up

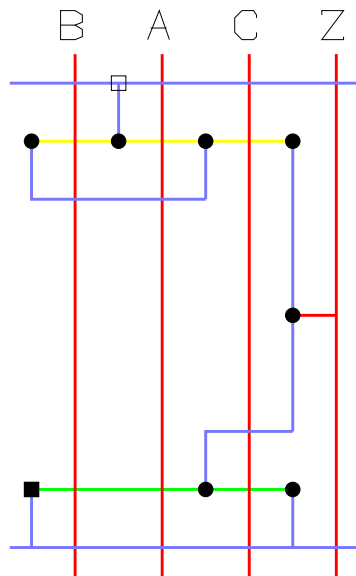


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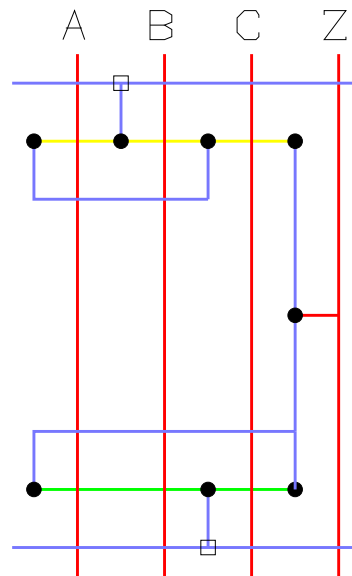
Choosing a Layout

Frequently there are several possible Euler paths for the same gate. Given that all cells must have taps, the position of the taps may effect your choice.

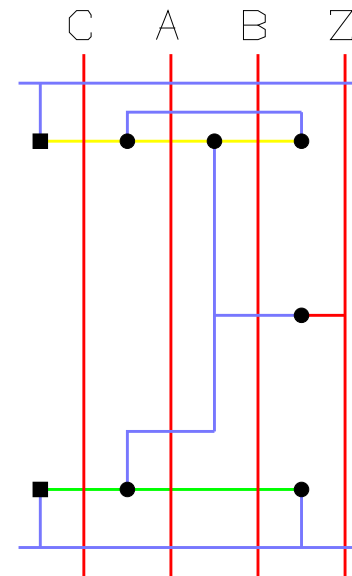
$$Z = \overline{(A \bullet B)} + C$$



(1)



(2)



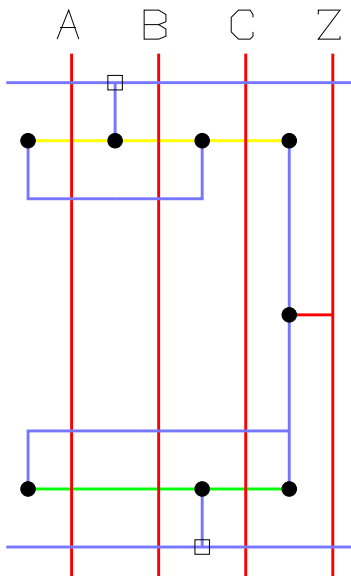
(3)

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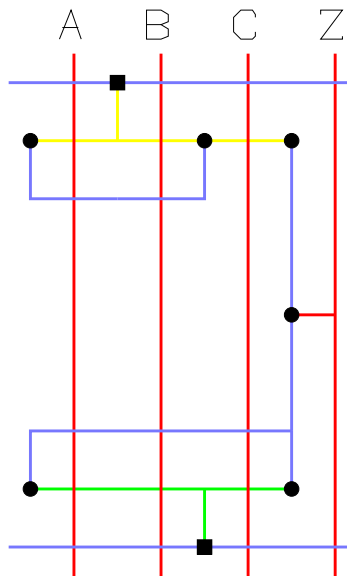
Choosing a Layout

Given an identical Euler path we still have choices such as tap location.

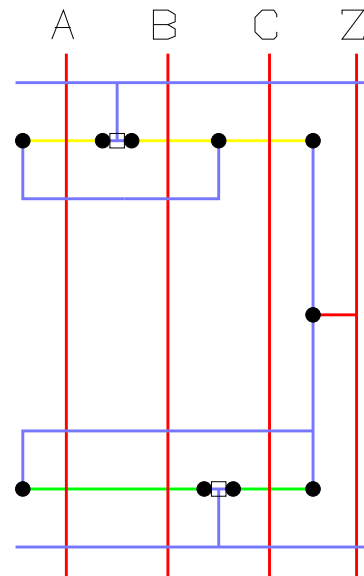
$$Z = \overline{(A \bullet B) + C}$$



(2)



(2a)



(2b)

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Choosing a Layout

There is no best layout for any cell.

There are always other considerations:

- Performance:
 - Minimum source-drain capacitance.
 - Ratio of P and N device sizes.
 - Ratio of series device sizes.
- Co-existence:
 - Geometry of other cells.
 - Routing Considerations.