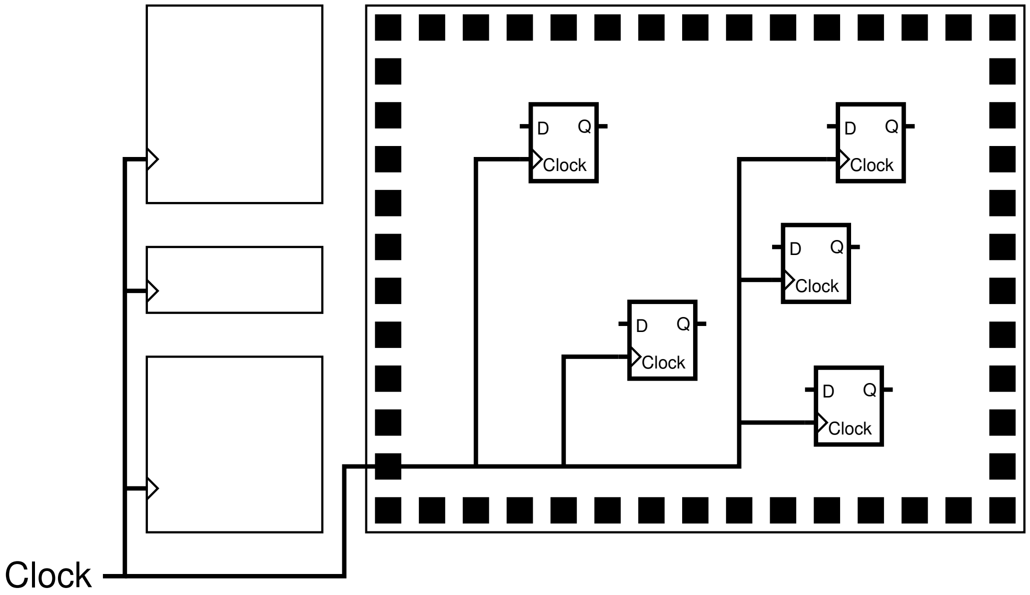
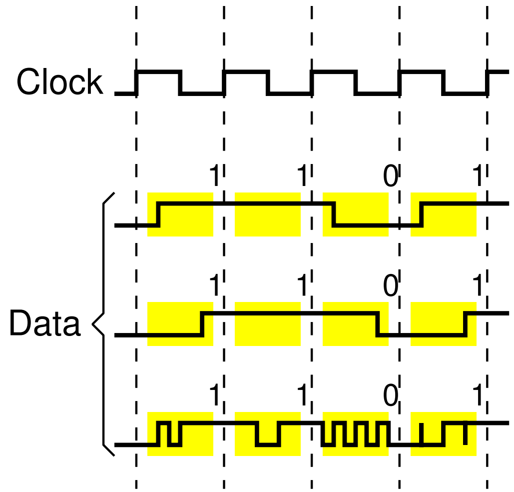
Synchronous Systems

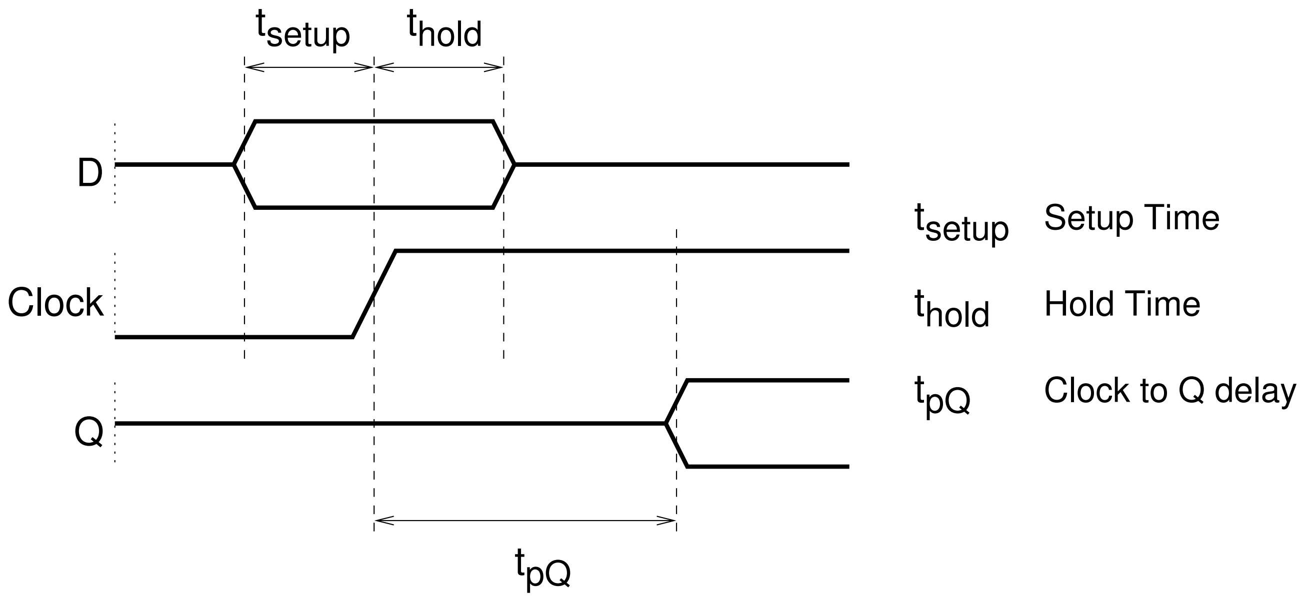




- All parts of the system share the same clock and the same clock edge sensitivity.
- The data may change between active clock transitions but must be stable by the time the next active transition occurs[1].

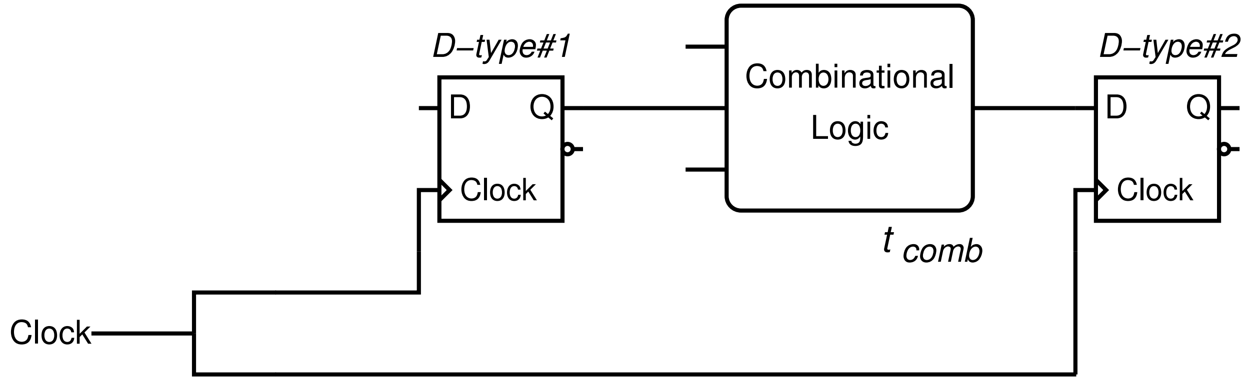
[1]for most systems the *active transition* is the rising edge of the clock

Synchronous Systems - D-type Timing



- Valid data should be present on D input for at least t_{setup} before the active clock edge and at least t_{hold} after the clock edge.
- The minimum D-type cycle time will be limited by the sum $t_{setup} + t_{pQ}$.

Synchronous Systems - Static Timing Analysis (Ideal Clock)



- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup}$$

- To avoid a hold violation:

$$t_{pQ} + t_{comb} > t_{hold}$$

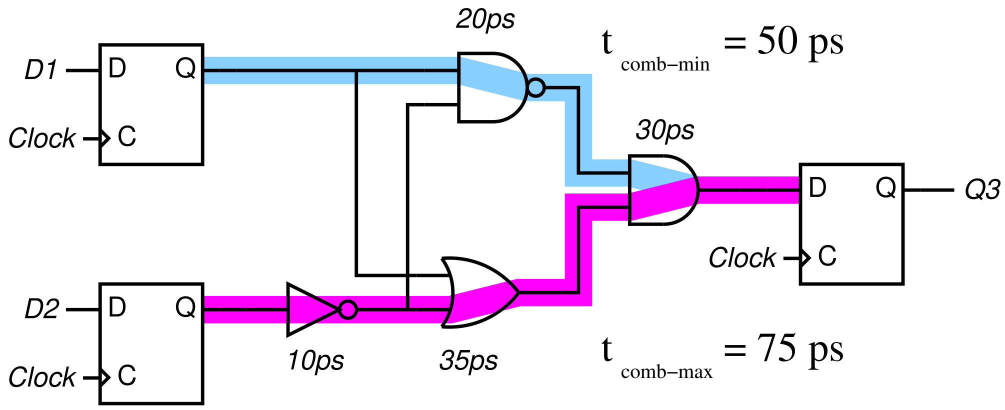
Static Timing Analysis

- Predicts the timing of a circuit without simulation[2]
- Analysis of gate network based on:
  - Propagation delays
  - Set-up and hold times for storage elements
  - Constraints such as desired operating freqency and the timing of inputs and outputs

Note that the examples given here are simplified in that they reduce the propagation delay through a gate to a single number - in reality there are predictable and unpredicatble variations in gate delays which must be accounted for by static timing analysis tools.

[2]timing simulations for large digital systems are slow and will usually not catch all edge and coner cases

Synchronous Systems - Static Timing Analysis (Ideal Clock)



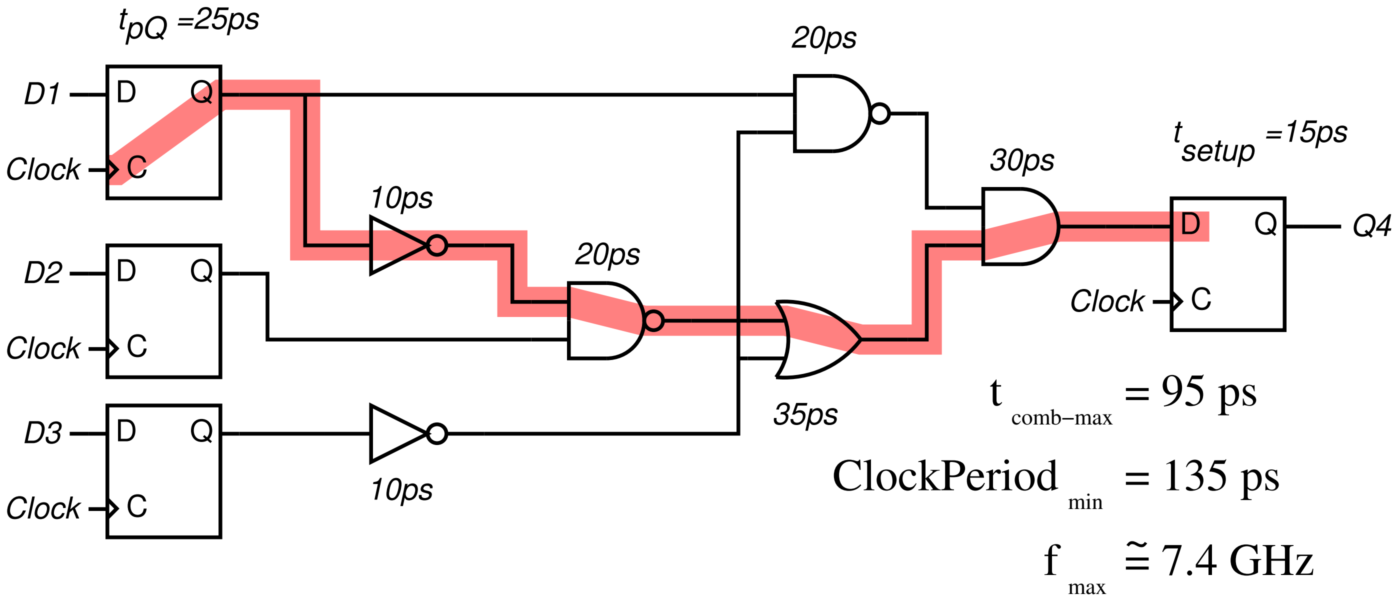
- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup}$$

- To avoid a hold violation:

$$t_{pQ} + t_{comb-min} > t_{hold}$$

Synchronous Systems - Static Timing Analysis (Ideal Clock)

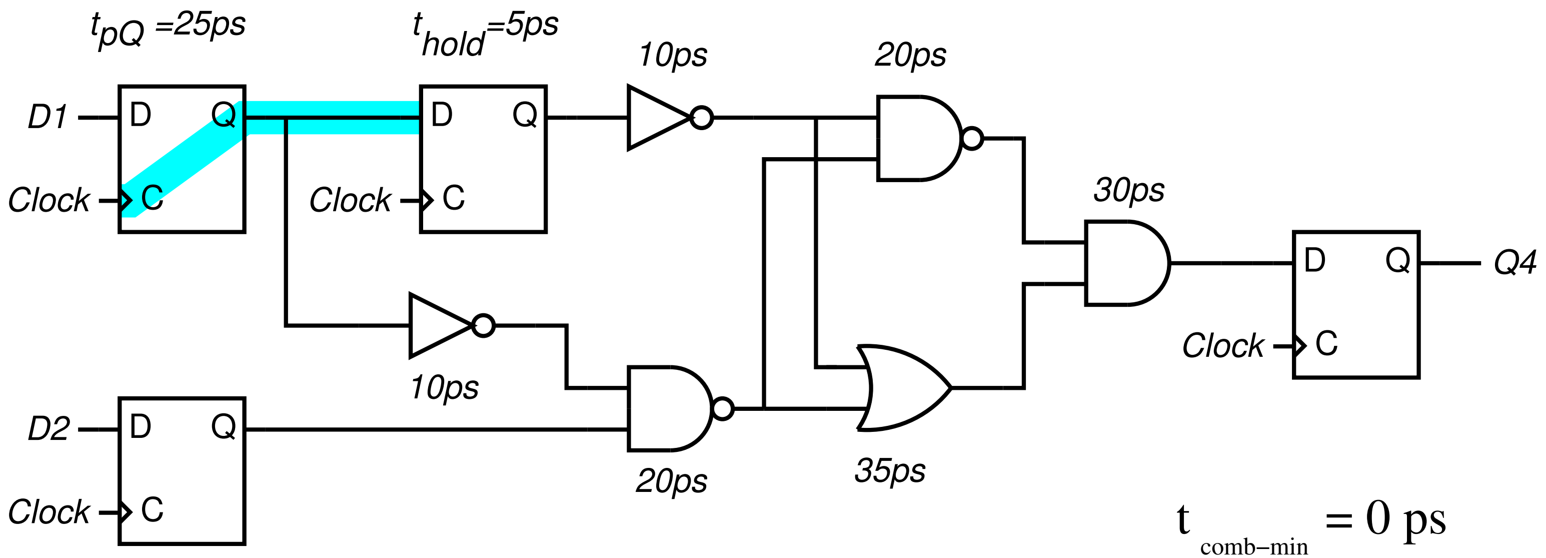


- Critcal path analysis allows us to determine the maximum feasible clock frequency:

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup}$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-max} + t_{setup}}$$

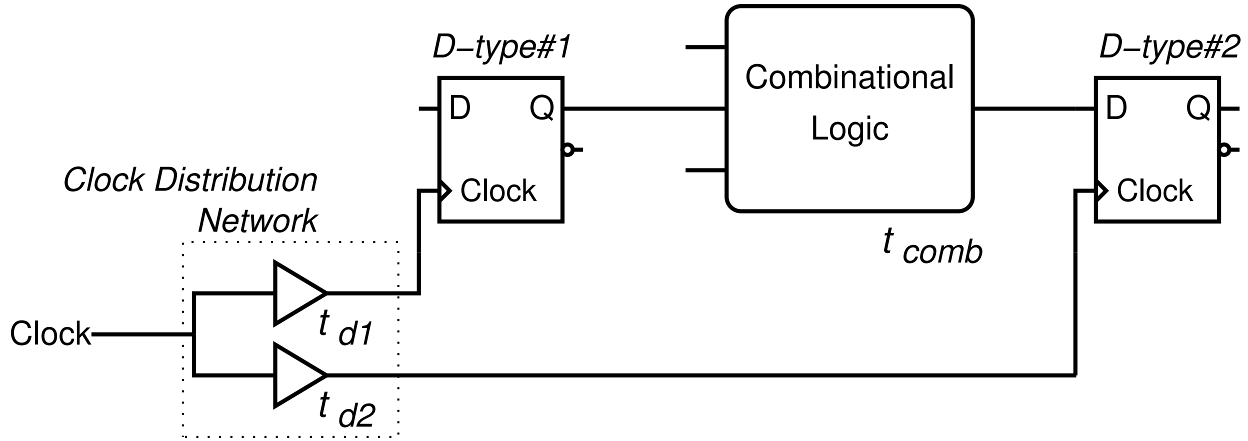
Synchronous Systems - Static Timing Analysis (Ideal Clock)



$$t_{pQ} + t_{comb-min} > t_{hold}$$

If we have an ideal clock and $t_{pQ} > t_{hold}$ we won't see hold violations even with if $t_{comb-min} = 0$.

Synchronous Systems - Clock Skew



- Clock Distribution

  The process of distributing clocks from a central source gives rise to delays.

  Clock skew is the difference between the arrival times of the clock at different points in the circuit.

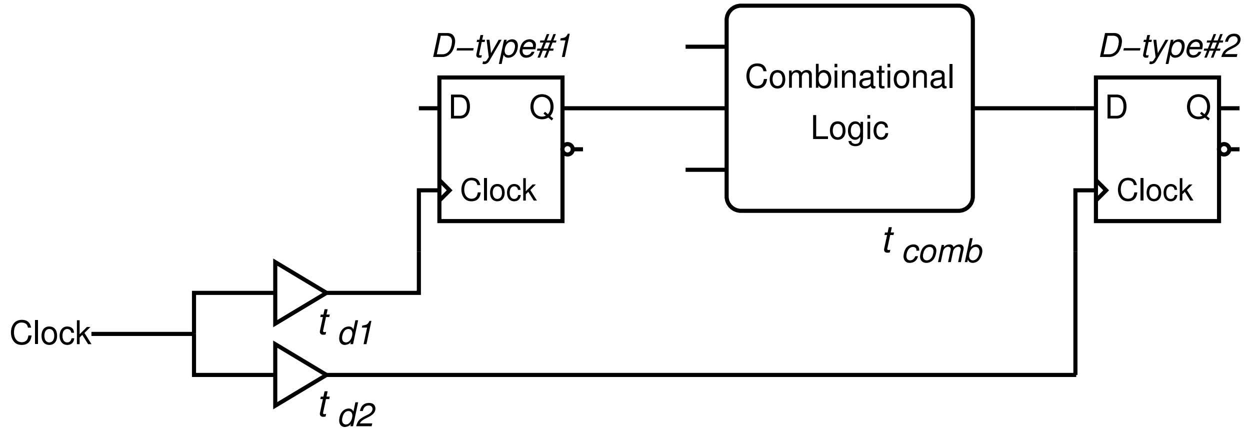
- Clock Skew may cause unexpected timing violations

  Hold: if *D-type #1* clocks first, D input of *D-type* #2 may change too early[3]

  Setup: if *D-type #1* clocks second, D input of *D-type #2* may change too late

[3] most likely where combinational logic is minimal or absent

Synchronous Systems - Static Timing Analysis (inc. clock skew)



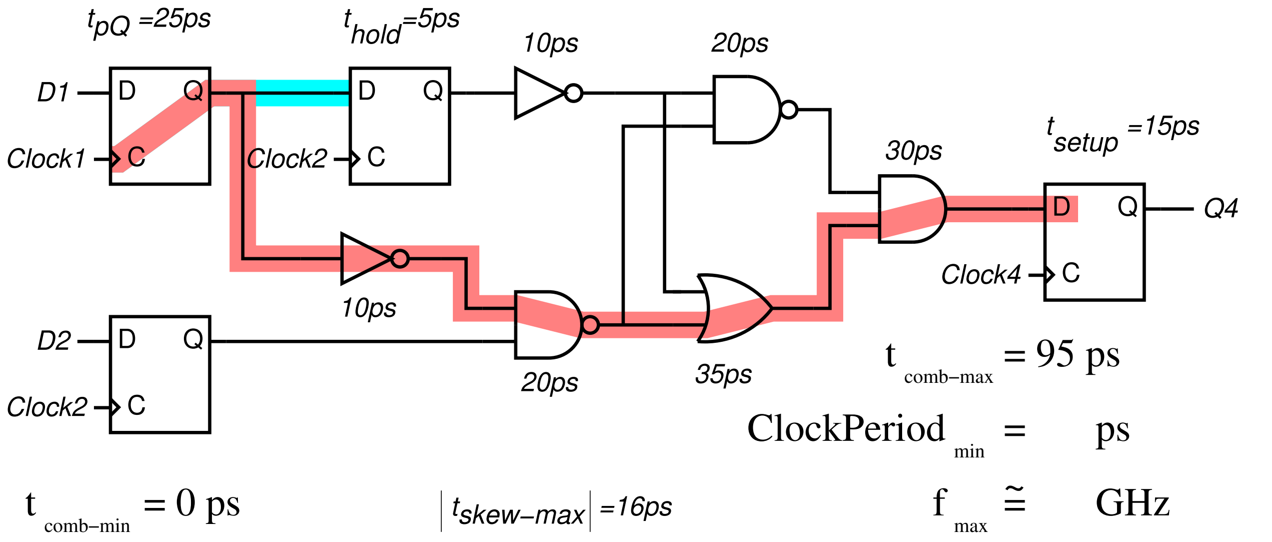
- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup} + (t_{d1} - t_{d2})$$

- To avoid a hold violation:

$$t_{pQ} + t_{comb} > t_{hold} + (t_{d2} - t_{d1})$$

Synchronous Systems - Static Timing Analysis (inc. clock skew)



- What is the maximum operating frequency of the circuit if the clock skew is no more than 16ps?

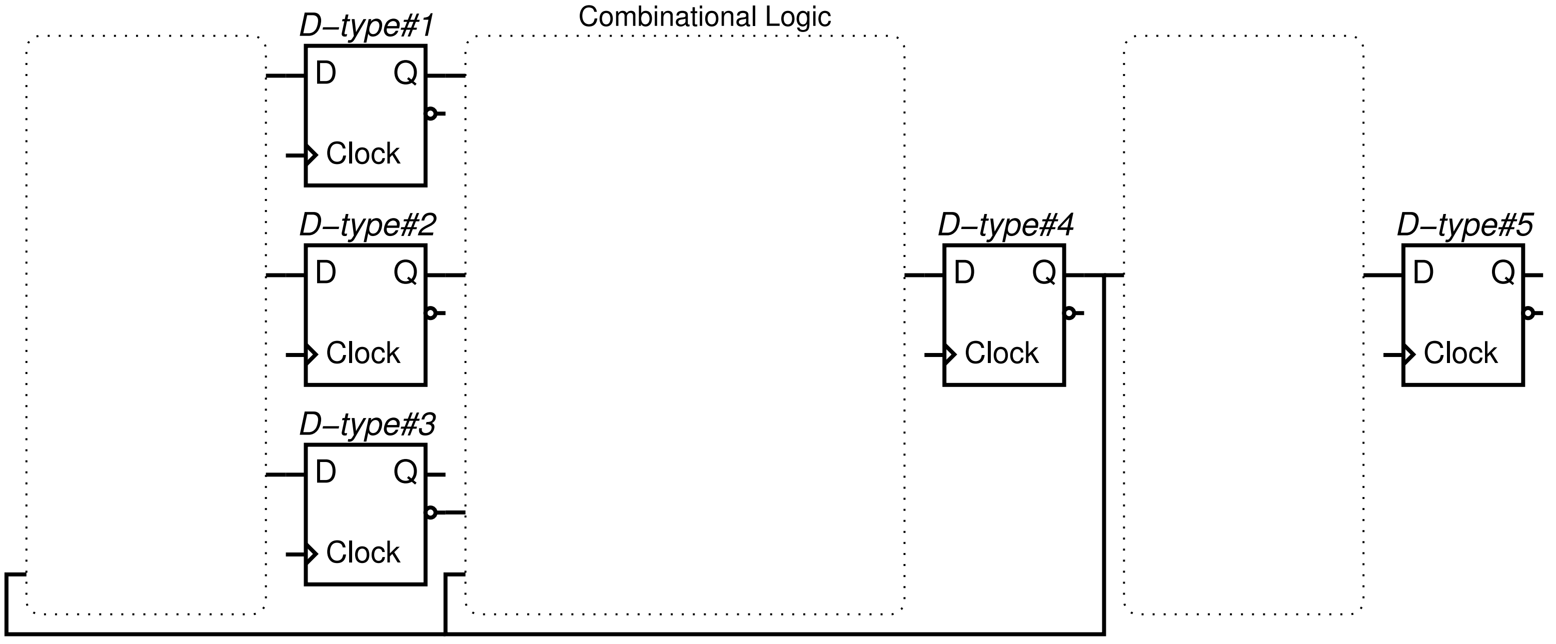
$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup} + t_{skew}$$

- What is the maximum clock skew that can be tolerated before we have a hold violation?

$$t_{pQ} + t_{comb} > t_{hold} + t_{skew}$$

Synchronous Systems - Static Timing Analysis (inc. clock skew)

Critical Path

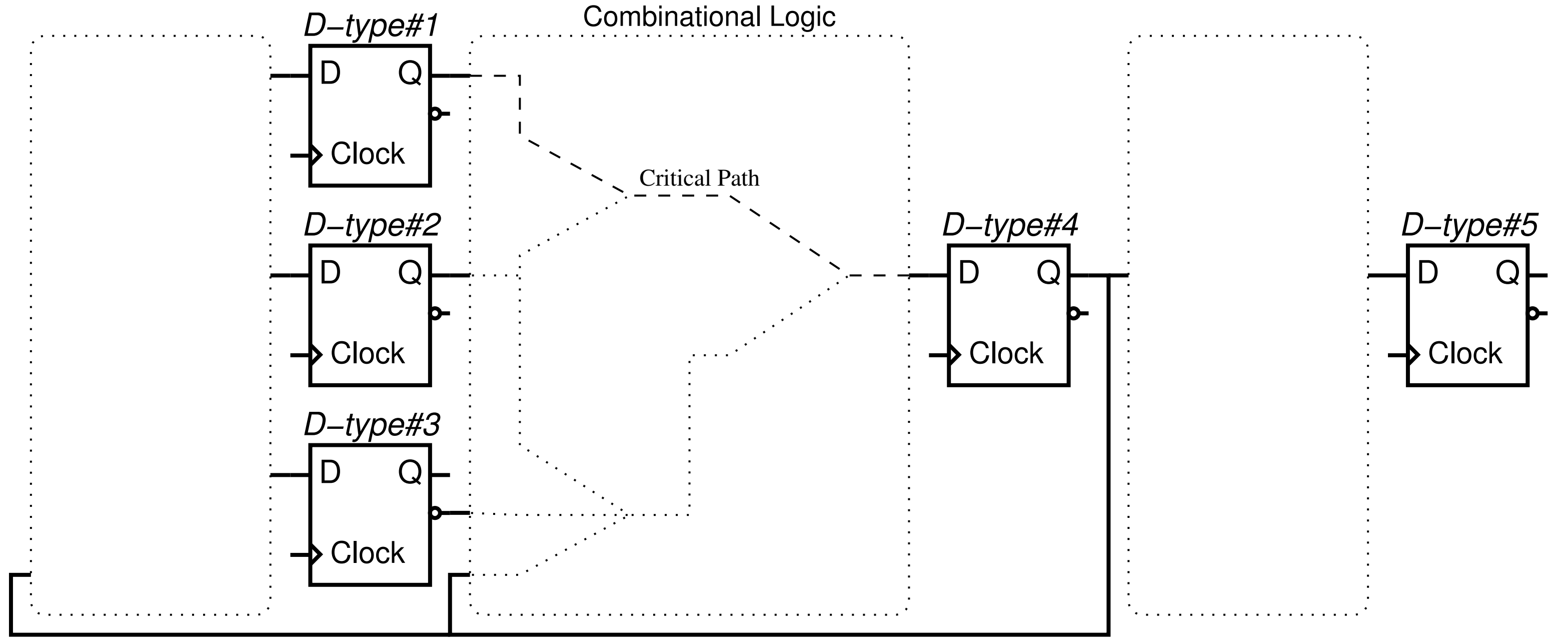


- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + t_{skew}$$

Synchronous Systems - Static Timing Analysis (inc. clock skew)

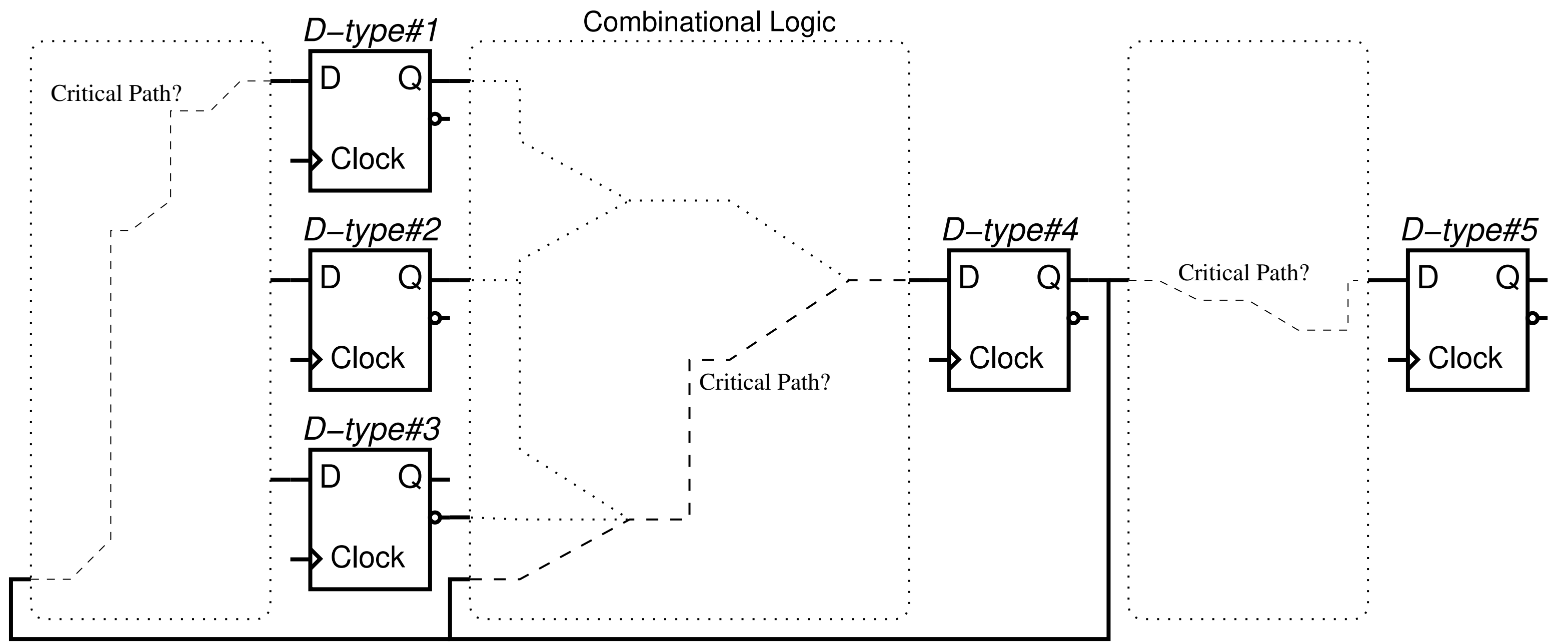
Critical Path



- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d1} - t_{d4})$$

Critical Path

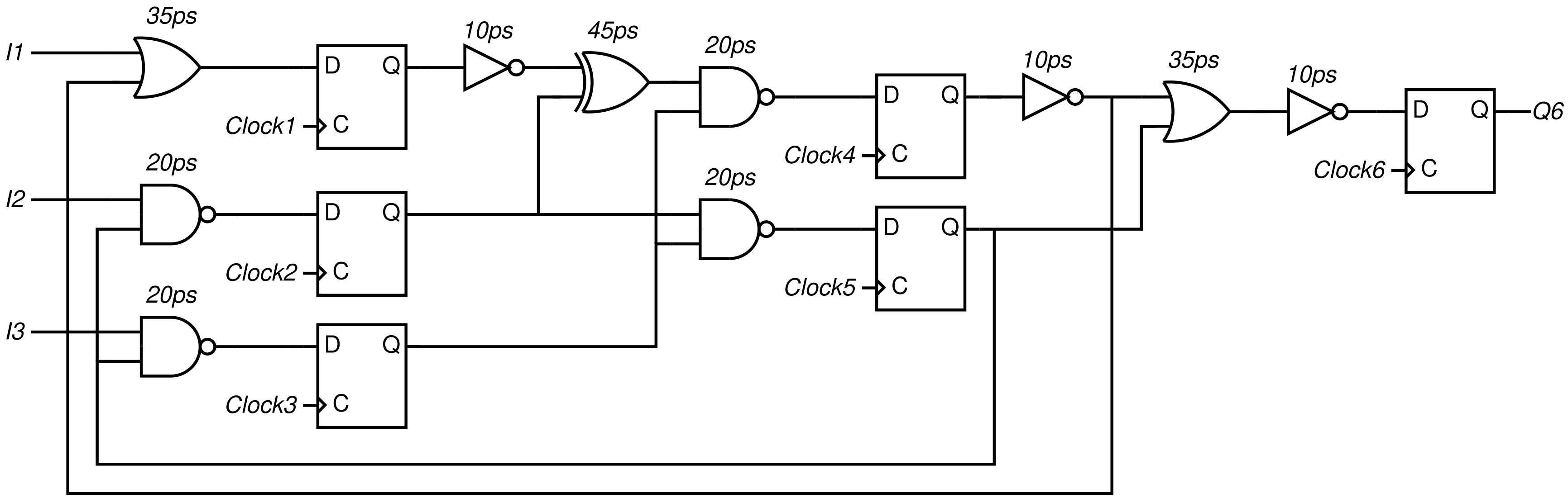


$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

- If we can control the skew (e.g. by increasing t_{d4}), we can ease the timing constraint.[4]

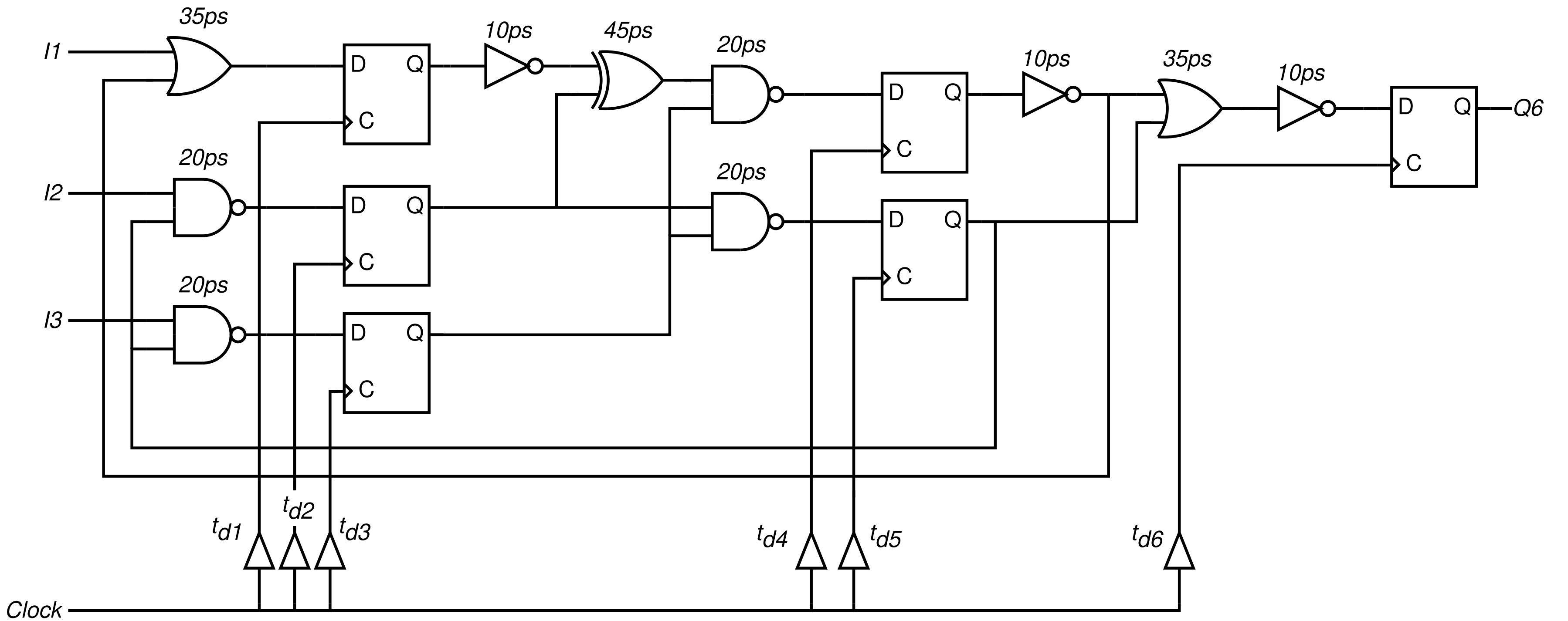
[4]this may result in the critical path moving to another part of the circuit

Synchronous Systems - Static Timing Analysis (inc. clock skew)



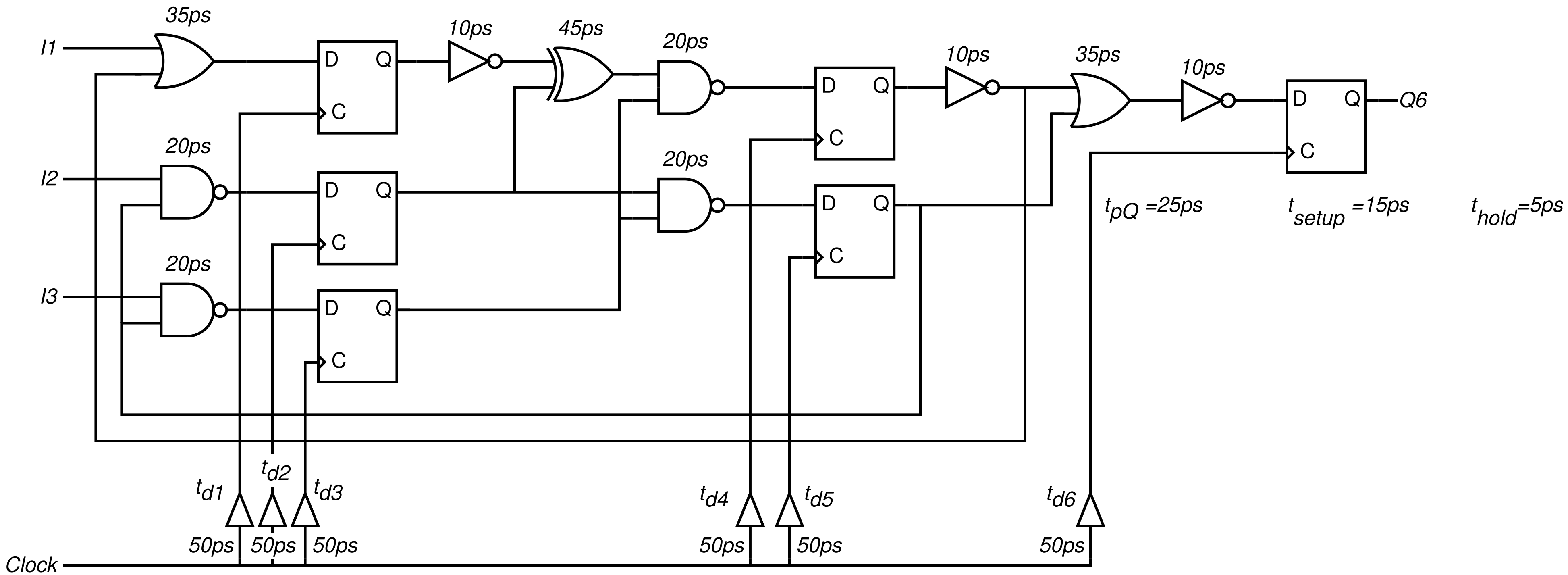
- Calculate f_{max} in the presence of intentional clock skew.

Synchronous Systems - Static Timing Analysis (inc. clock skew)



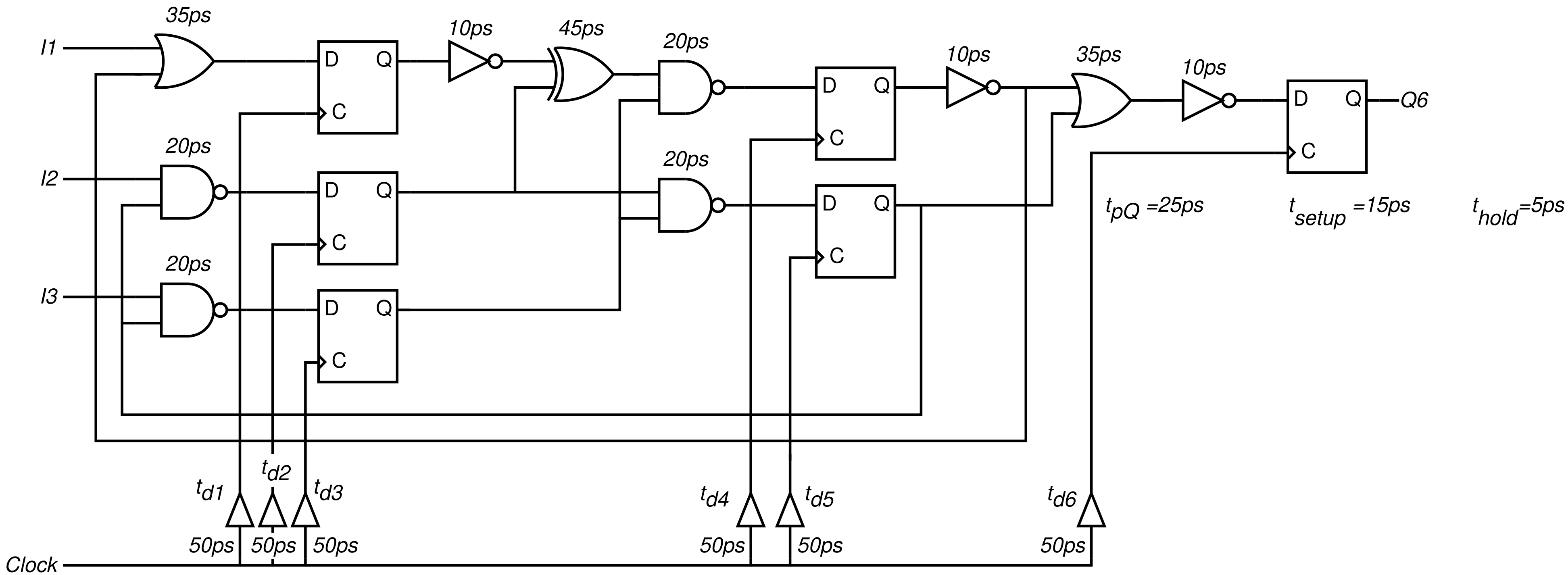
- Calculate f_{max} in the presence of intentional clock skew.
- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}, t_{d5}, t_{d6}

Synchronous Systems - Static Timing Analysis (inc. clock skew)



- Calculate f_{max} in the presence of intentional clock skew.
- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}, t_{d5}, t_{d6}
  Initially set all to a minimum value (in this case 50ps)

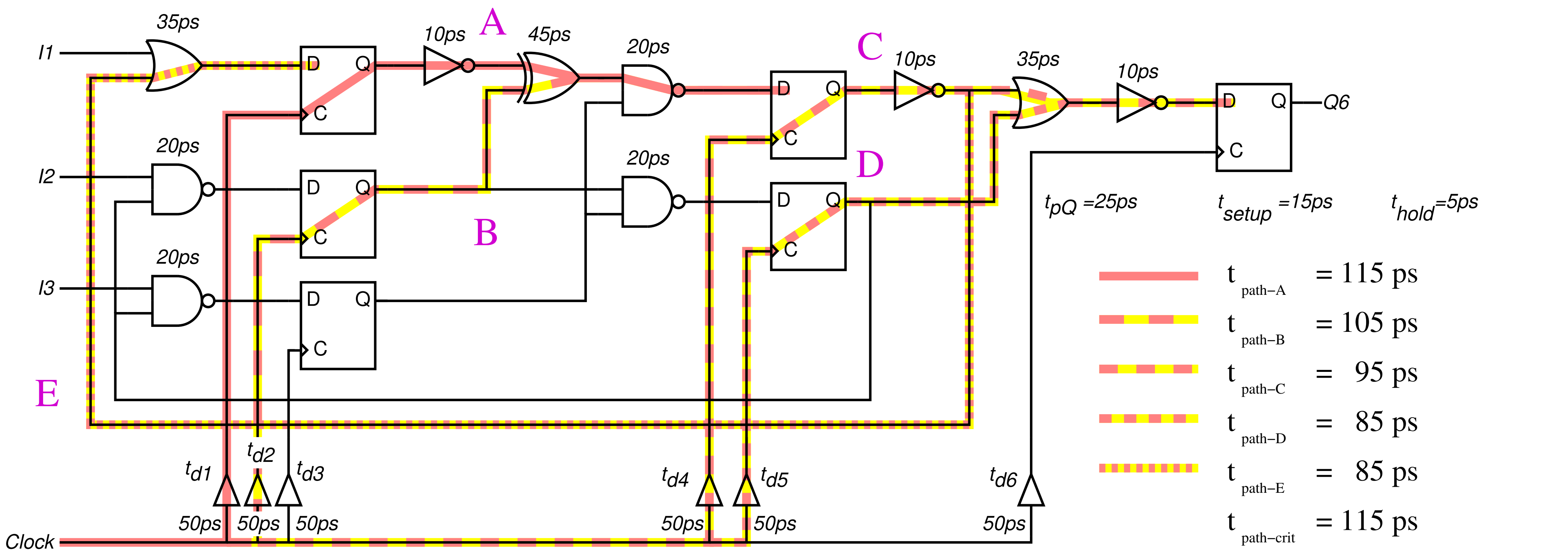
Synchronous Systems - Static Timing Analysis (inc. clock skew)



- Calculate f_{max} in the presence of intentional clock skew.
- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}, t_{d5}, t_{d6}

⇒ Identify longest timing paths

Synchronous Systems - Static Timing Analysis (inc. clock skew)

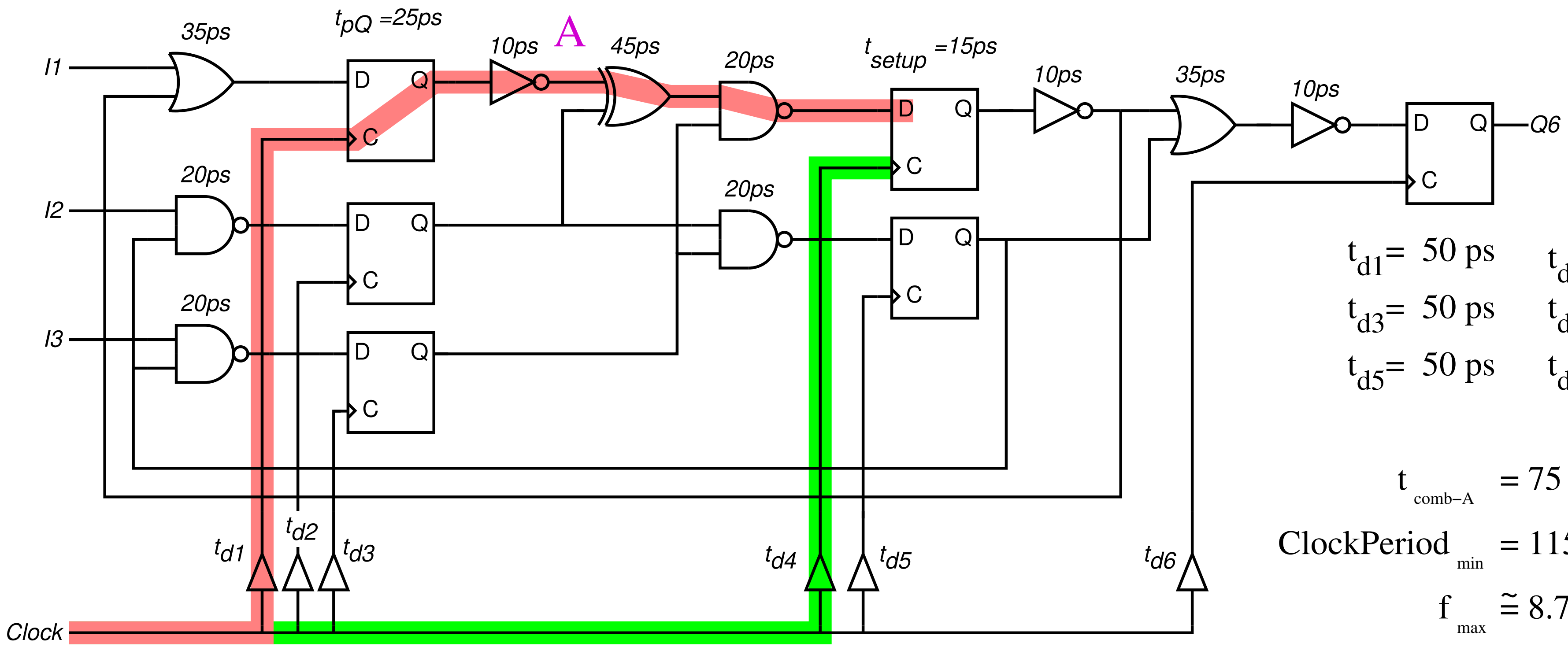


- Calculate f_{max} in the presence of intentional clock skew.
- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}, t_{d5}, t_{d6}

⇒ Identify longest timing paths

$$t_{path} = t_{pQ} + t_{comb} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

Synchronous Systems - Static Timing Analysis (inc. clock skew)



t_{d1} = 50 ps t_{d2} = 50 ps

t_{d3} = 50 ps t_{d4} = 50 ps

t_{d5} = 50 ps t_{d6} = 50 ps

t_{comb-A} = 75 ps

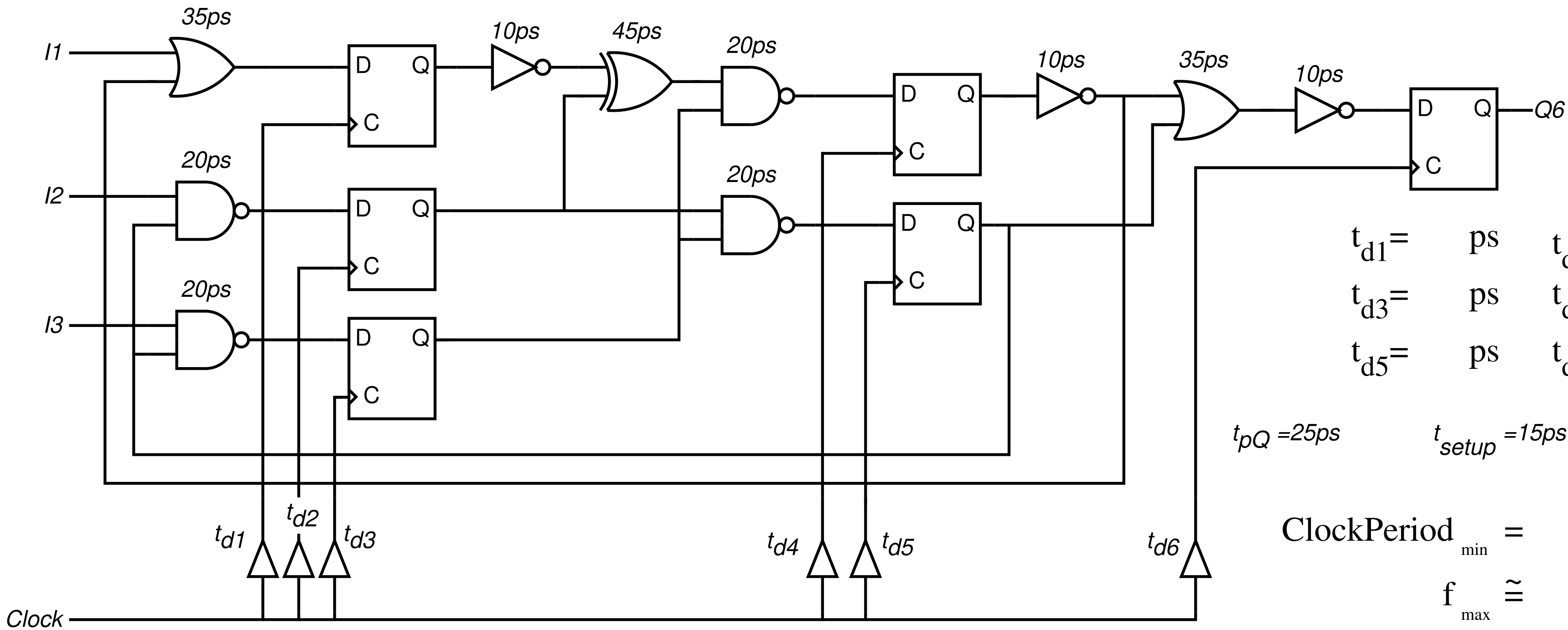
$ClockPeriod_{min}$ = 115 ps

$f_{max} \cong$ 8.7 GHz

$$ClockPeriod > t_{pQ} + t_{comb-A} + t_{setup} + (t_{d1} - t_{d4})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-A} + t_{setup} + (t_{d1} - t_{d4})}$$

Synchronous Systems - Static Timing Analysis (inc. clock skew)



t_{d1}= ps t_{d2}= ps
t_{d3}= ps t_{d4}= ps
t_{d5}= ps t_{d6}= ps

t_{pQ} =25ps t_{setup} =15ps t_{hold}=5ps

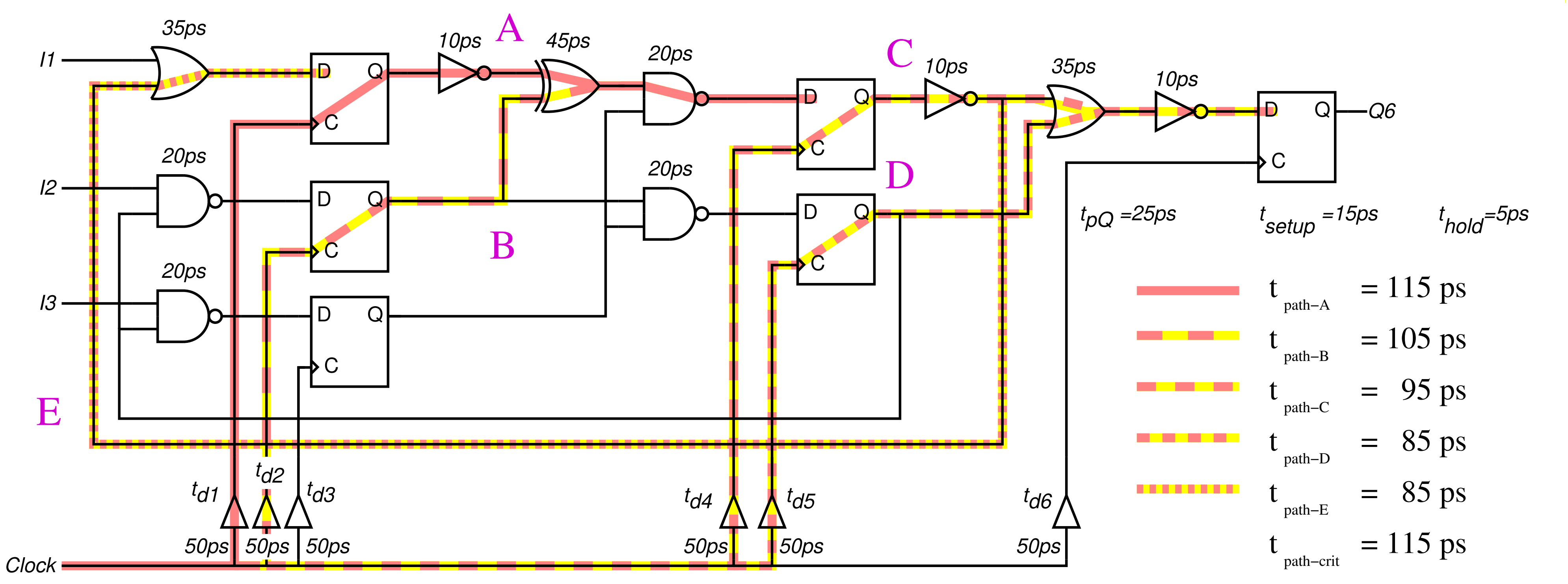
$ClockPeriod_{min}$ = ps

f_{max} ≅ GHz

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

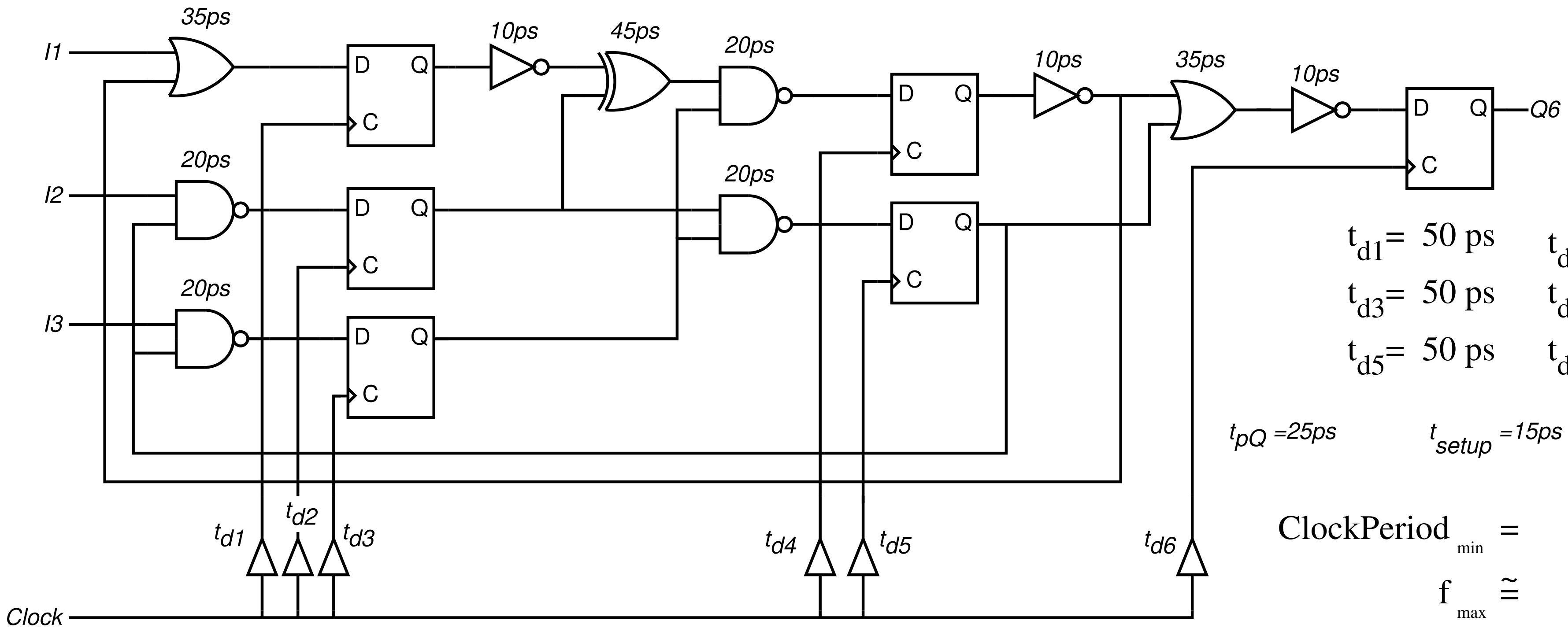
$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})}$$

Synchronous Systems - Static Timing Analysis (inc. clock skew)



⇒ Initially try increasing t_{d4} by 20ps

Synchronous Systems - Static Timing Analysis (inc. clock skew)



t_{d1}= 50 ps t_{d2}= 50 ps
t_{d3}= 50 ps t_{d4}= 70 ps
t_{d5}= 50 ps t_{d6}= 50 ps

t_{pQ} =25ps t_{setup} =15ps t_{hold}=5ps

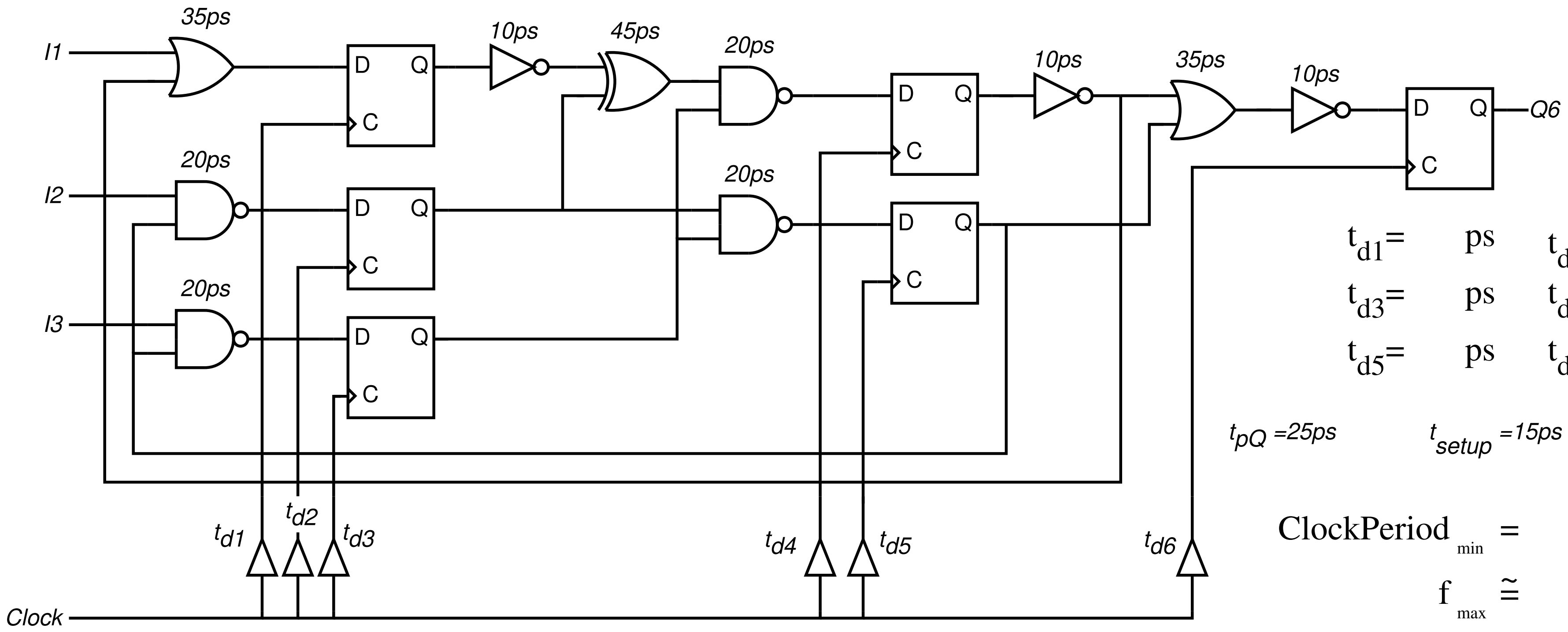
$ClockPeriod_{min}$ = ps

f_{max} ≅ GHz

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})}$$

Synchronous Systems - Static Timing Analysis (inc. clock skew)



t_{d1}= ps t_{d2}= ps

t_{d3}= ps t_{d4}= ps

t_{d5}= ps t_{d6}= ps

t_{pQ} =25ps t_{setup} =15ps t_{hold}=5ps

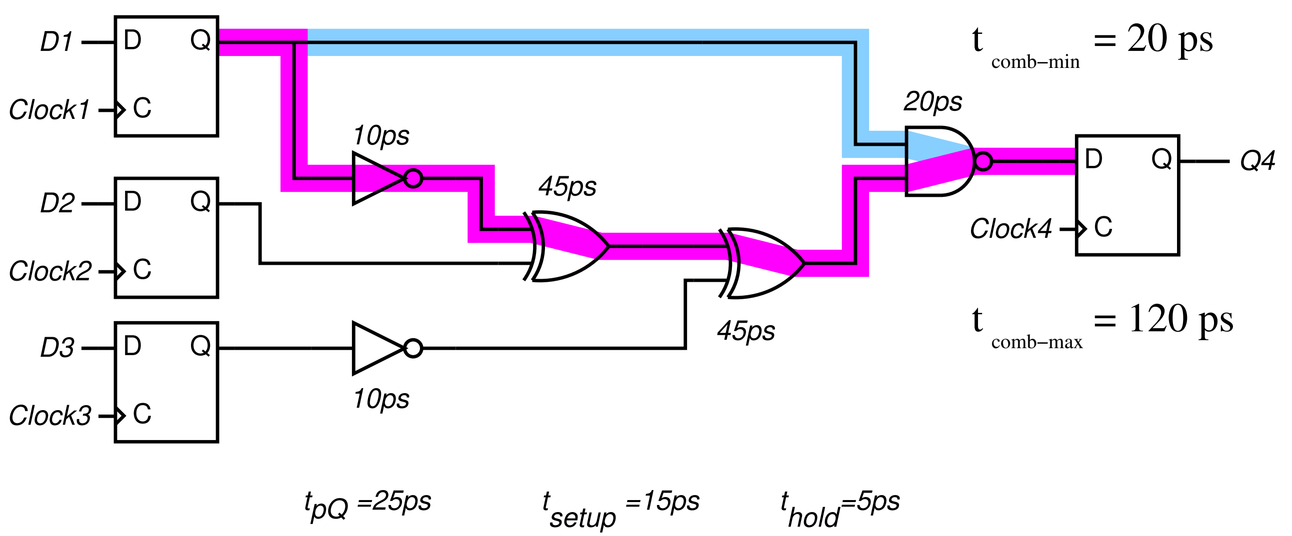
ClockPeriod $_{min}$ = ps

f $_{max}$ ≅ GHz

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})}$$

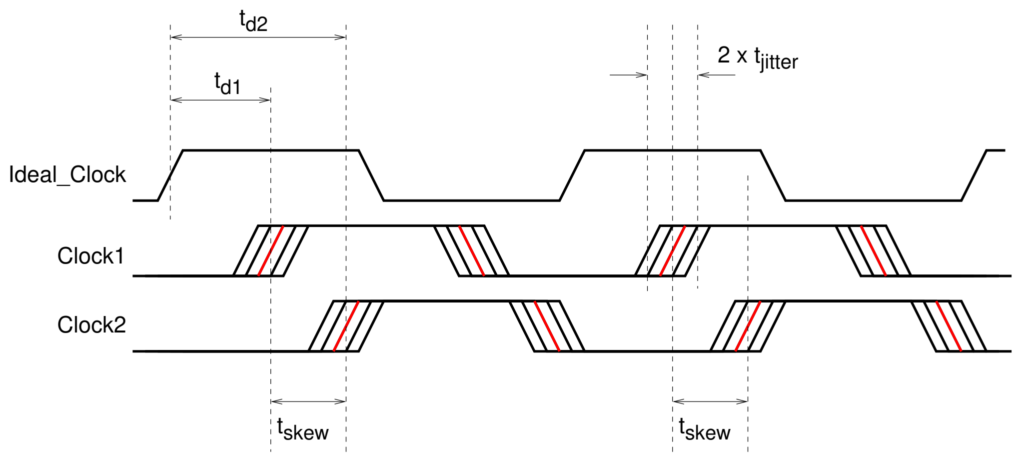
Synchronous Systems - Static Timing Analysis (inc. clock skew)



- Calculate f_{max} in the presence of intentional clock skew.
- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4} given that the minimum delay through the clock tree is 50ps

remember to check for hold violations

Synchronous Systems - Jitter



- Jitter

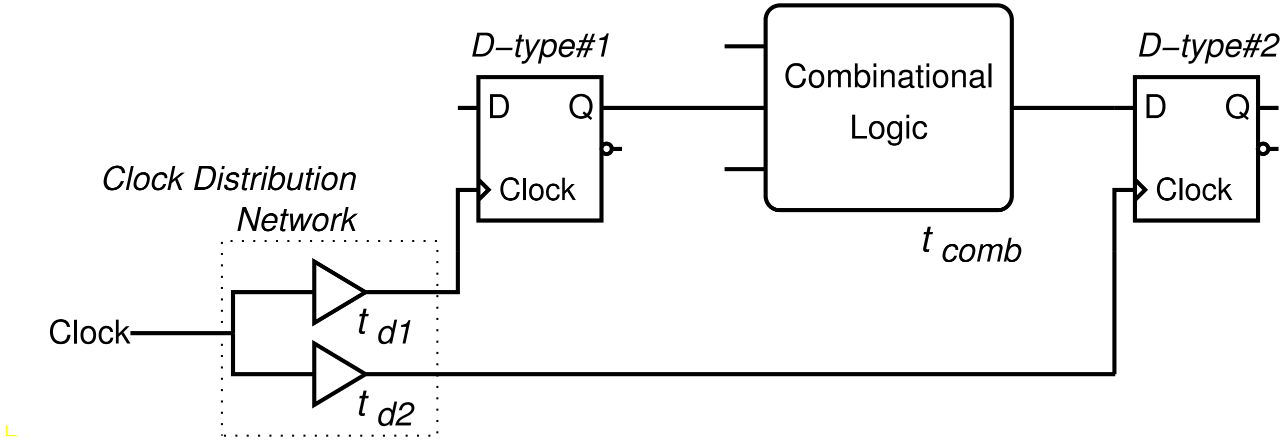
  Jitter is the cycle-by-cycle variation in the arrival time of the clock.

- Caused by
  - Variation in frequency/phase of clock source[5]
  - Power supply noise affecting clock distribution
  - Cross-talk affecting clock distribution

- Jitter may cause unexpected timing violations

[5] primary clock source or Phase-Locked Loop (PLL)

Synchronous Systems - Jitter



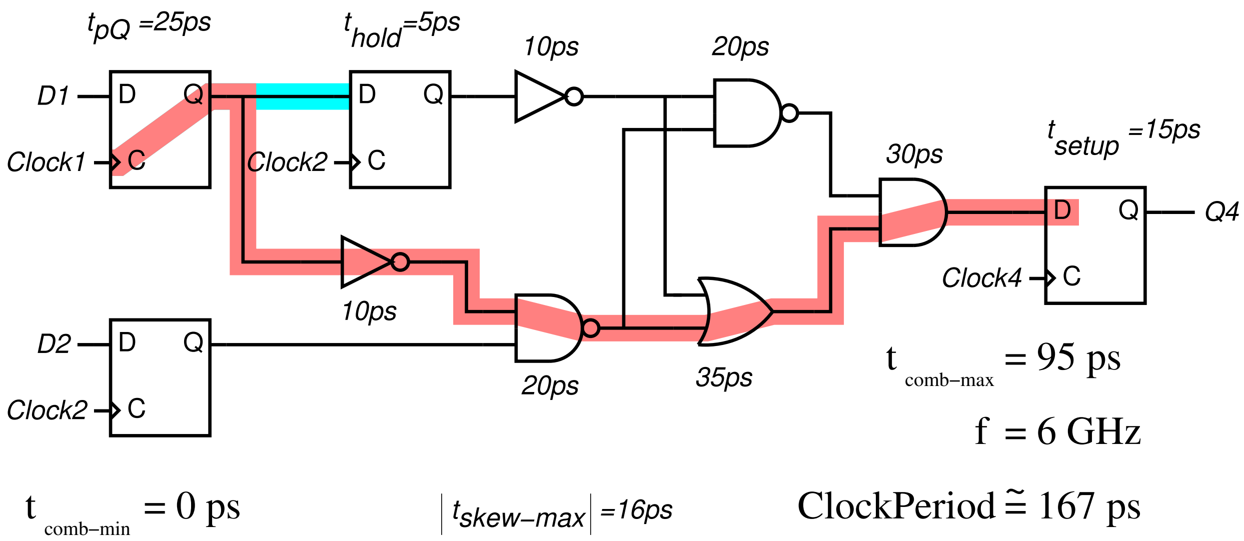
- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup} + (t_{d1} - t_{d2}) + 2 \times t_{jitter}$$

- To avoid a hold violation:

$$t_{pQ} + t_{comb} > t_{hold} + (t_{d2} - t_{d1}) + 2 \times t_{jitter}$$

Synchronous Systems - Static Timing Analysis (skew + jitter)



- What is the maximum jitter that can be tolerated given an operating frequency of 6GHz and clock skew of no more than 16ps?[6]

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup} + t_{skew} + 2 \times t_{jitter}$$

$$t_{pQ} + t_{comb-min} > t_{hold} + t_{skew} + 2 \times t_{jitter}$$

[6] remember to consider both setup and hold violations