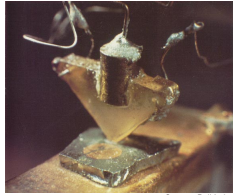


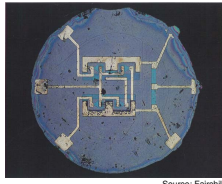
1947 Point Contact transistor



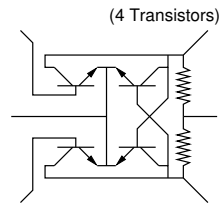
Source: Bell Labs



1961 Fairchild Bipolar RTL RS Flip-Flop



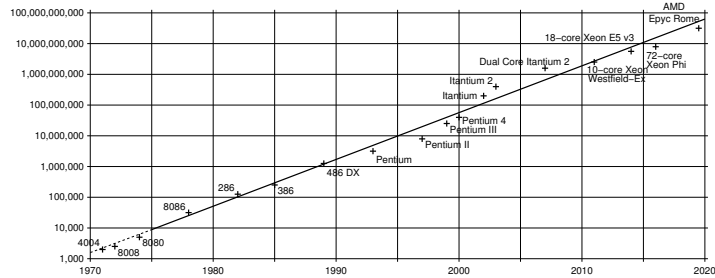
Source: Fairchild



(4 Transistors)

Moore's Law (1965) Number of components has doubled every year and will continue to do so until 1975

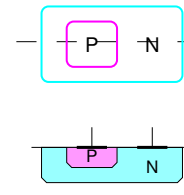
Moore's Law (1975) Number of components will double every two years



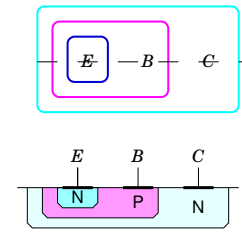
Self-fulfilling Prophecy

1000

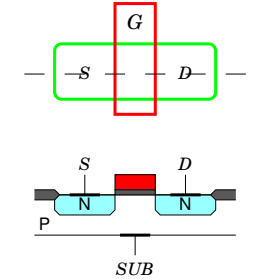
Diode



NPN Transistor



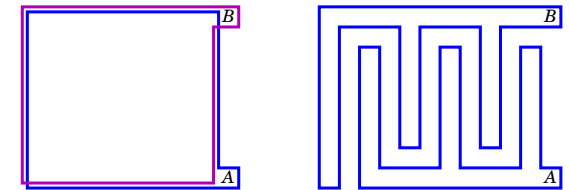
NMOS Enhancement transistor
NMOS Process



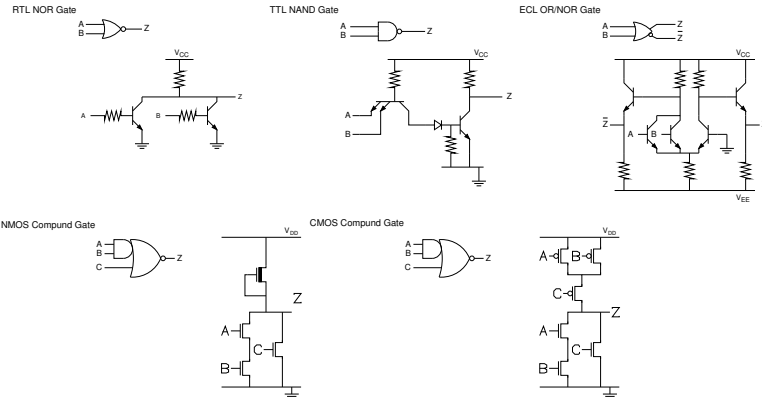
Resistor

1	2	3	4	5	6	7	8	9	10
3	18	17	16	15	14	13	12	11	2
19									
4	20	21	22	23	24	25	26	27	5
7	36	35	34	33	32	31	30	29	6
37									
8	38	39	40	41	42	43	44	45	46

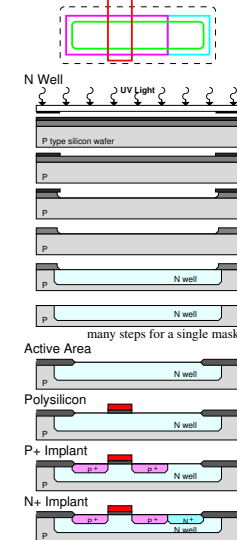
Capacitors



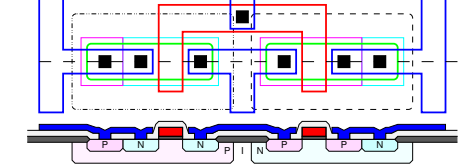
3000



PMOS Enhancement transistor
CMOS Process

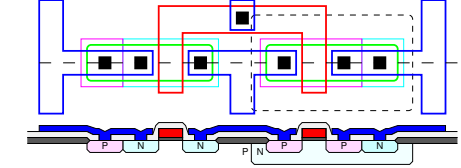


CMOS Inverter

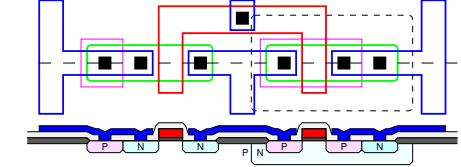


Twin Tub CMOS Process

CMOS Inverter N-Well CMOS Process (with explicit N+ implant mask)



CMOS Inverter N-Well CMOS Process (without explicit N+ implant mask)



Features may be determined by a number of masks
e.g. NMOS source drain: ActiveArea AND NOT(NWell OR Poly OR PImplant)

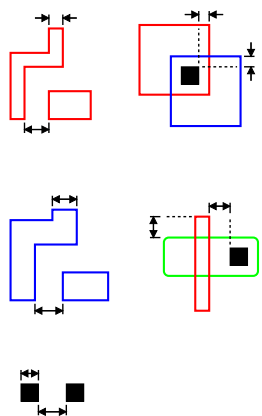
- Bipolar Transistors with Resistors - MSI/LSI
 - RTL - NOR
 - TTL - NAND
 - ECL - OR/NOR
- MOS Transistors (no resistors) - VLSI
 - NMOS
 - CMOS - No static power!

Both allow construction of NOR, NAND & Compound gate (always inverting)

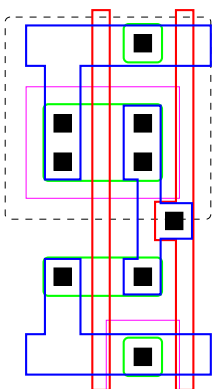
2000

4000

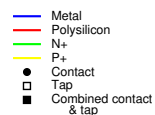
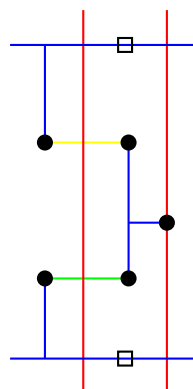
Design Rules – width, separation, overlap



Optimised Mask Layout



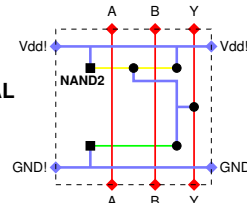
Equivalent Stick Diagram



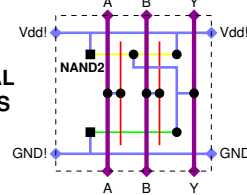
5000

LAYOUT

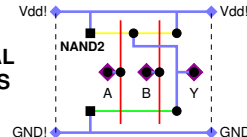
1 METAL LAYER



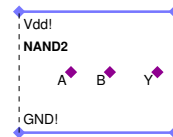
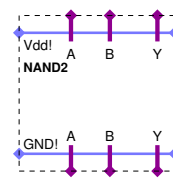
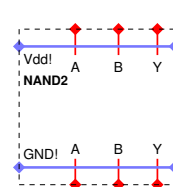
2 METAL LAYERS



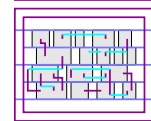
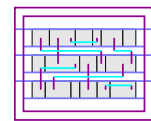
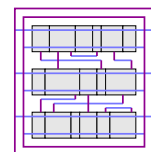
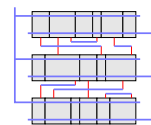
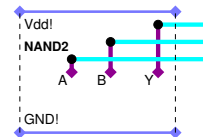
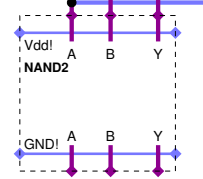
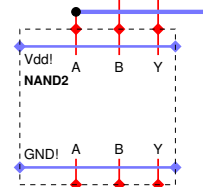
3 METAL LAYERS



ABSTRACT

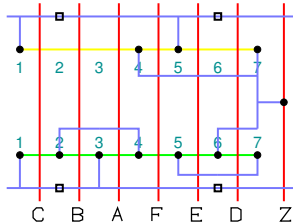
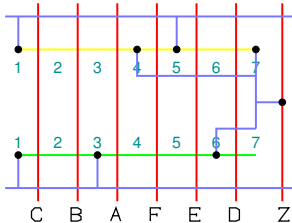
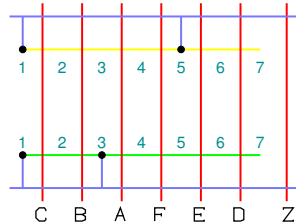
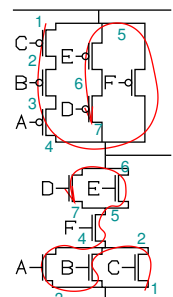
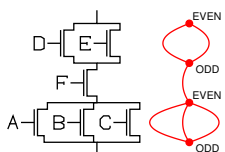
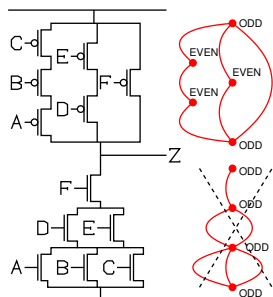


ROUTING



7000

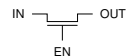
Investigation of Euler paths leads to more efficient layout*



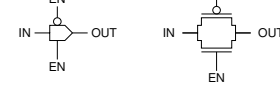
*not all gates will support a common Euler path for both PMOS and NMOS

6000

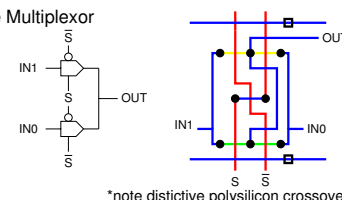
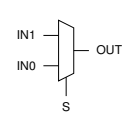
Pass Transistor



CMOS Transmission Gate

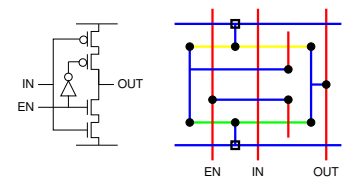
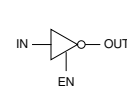


Transmission Gate Multiplexor

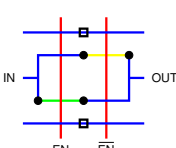
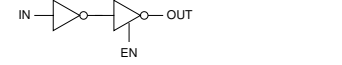
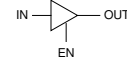


*note distinctive polysilicon crossover

Tri-state Inverter



Tri-state Buffer



Tri-state gates are used for Multiplexing

Distributed Multiplexing

using transmission gates



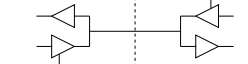
using tri-state inverters



using tri-state buffers

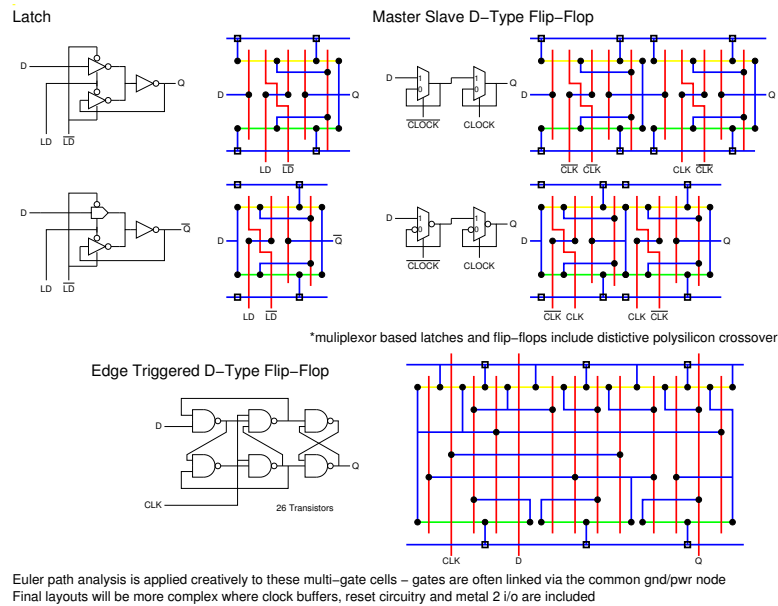


Bi-directional I/O



*this is another form of multiplexing

8000



9000

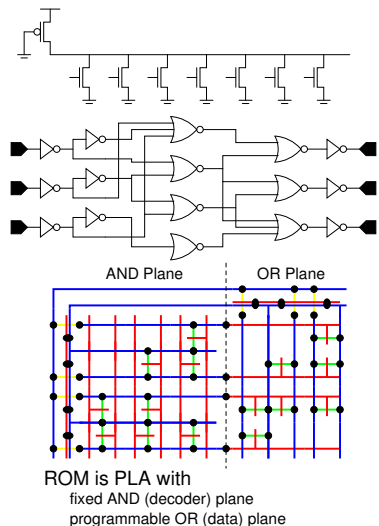
	Programmable Logic	Semi-Custom	Full Custom
Skill Required	Little		
Time to Market	Quick		
One-off Manufacturing Cost	Cheap		
Unit Cost In Production	Cheap		
Speed	Fast		
Area	Small		
Power	Low		

All design styles need full custom designers

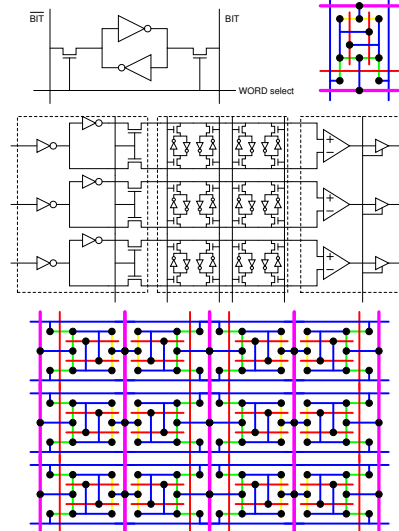
A large ASIC (especially SoC) may mix Semi-Custom and Full Custom

11000

PLA and ROM



SRAM



Cells are designed to butt together in two dimensions leading to efficient layout

PLA layout efficiency will depend on the actual function implemented (e.g. number of common product terms)

10000