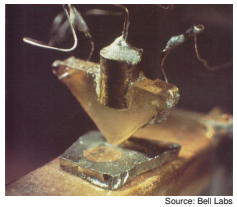
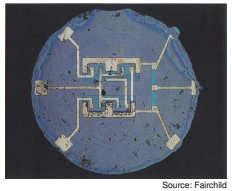
1947 Point Contact transistor



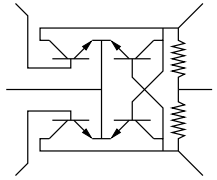
Source: Bell Labs

1961 Fairchild Bipolar RTL RS Flip–Flop

(4 Transistors)

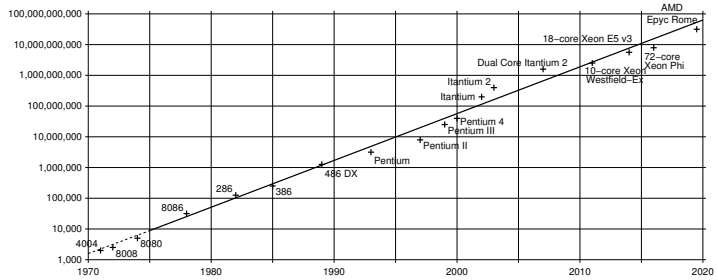


Source: Fairchild



Moore's Law (1965) Number of components has doubled every year and will continue to do so until 1975

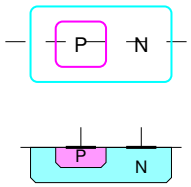
Moore's Law (1975) Number of components will double every two years



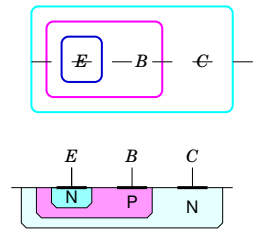
Self–fulfilling Prophecy

1000

Diode

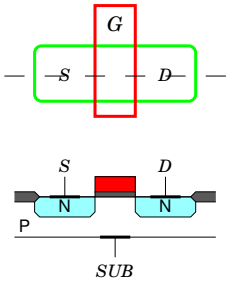


NPN Transistor

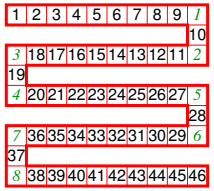


NMOS Enhancement transistor

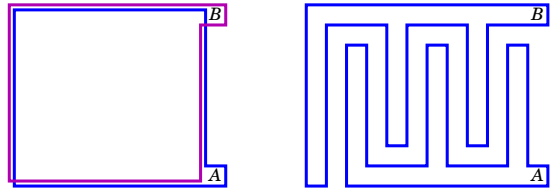
NMOS Process



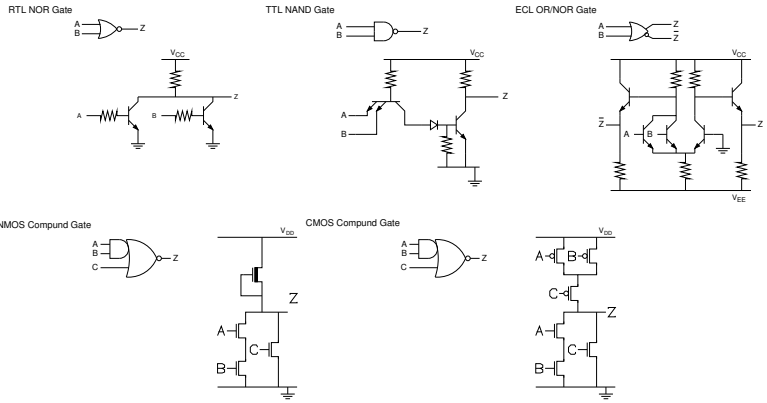
Resistor



Capacitors



3000



- Bipolar Transitors with Resistors - MSI/LSI

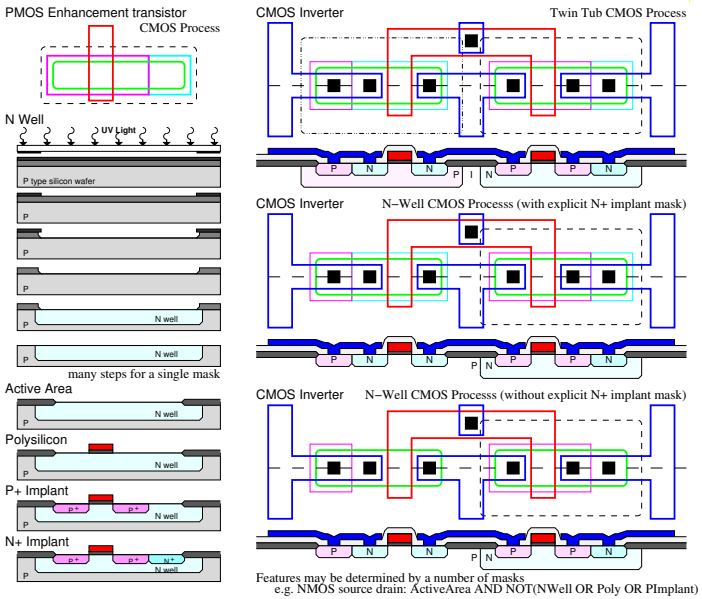
  RTL - NOR TTL - NAND ECL - OR/NOR

- MOS Transistors (no resistors) - VLSI

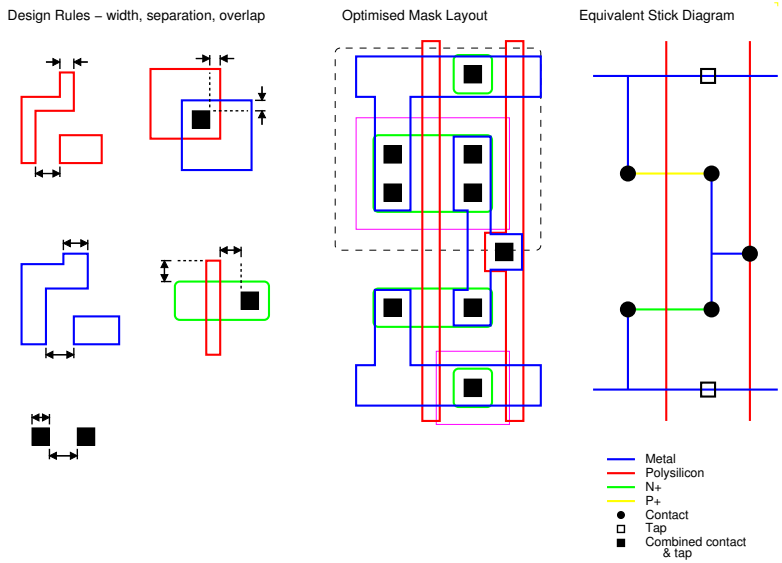
  NMOS CMOS - No static power!

Both allow construction of NOR, NAND & Compound gate (always inverting)

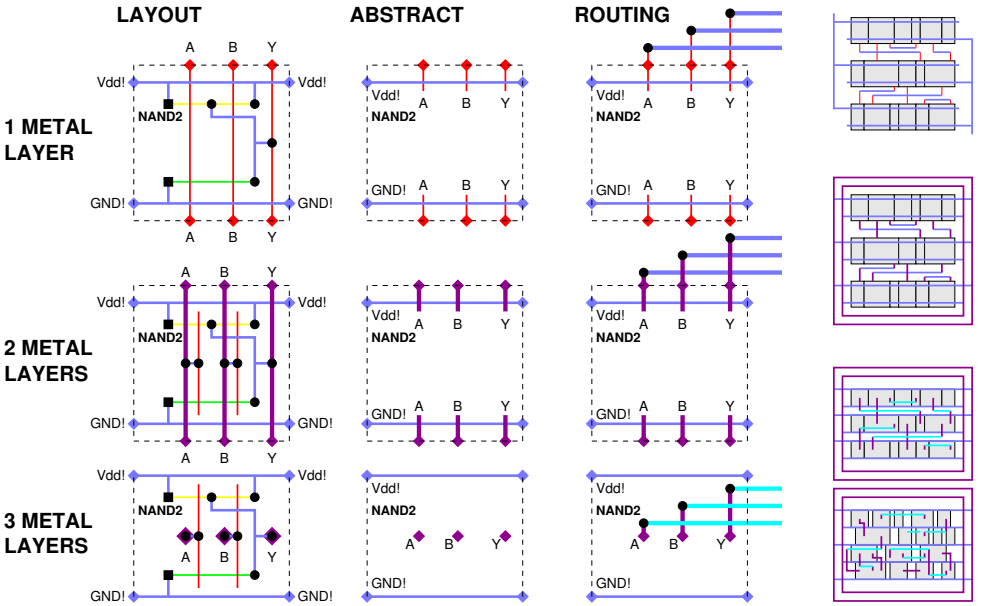
2000



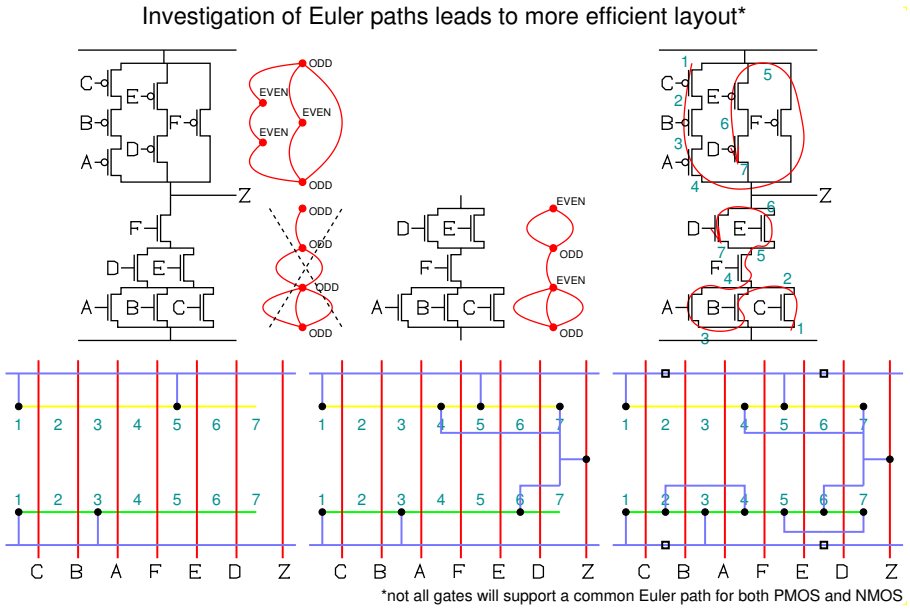
4000



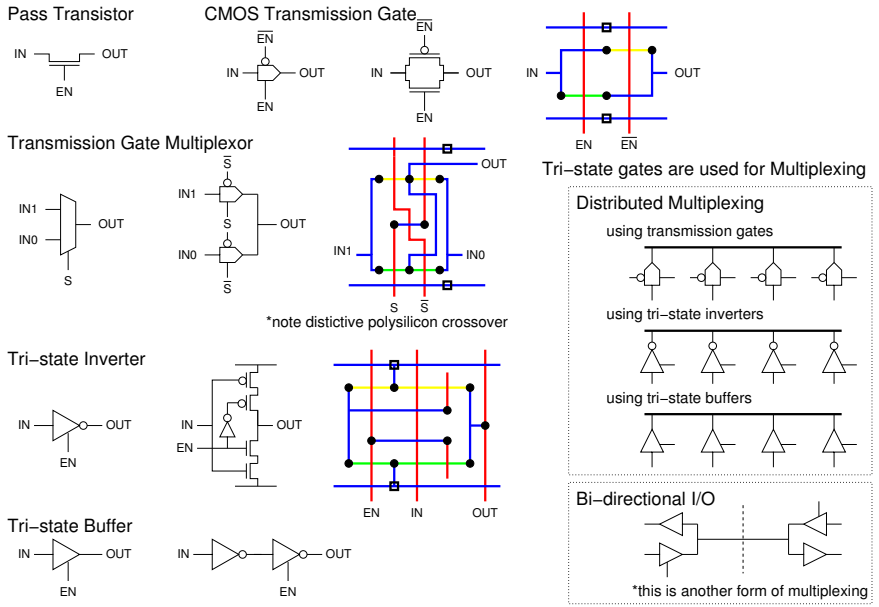
5000



7000

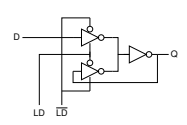


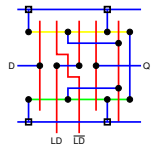
6000

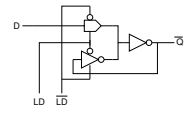


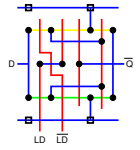
8000

Latch

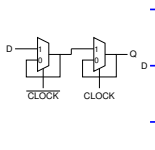


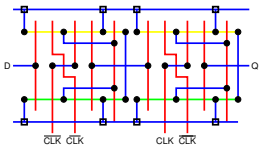


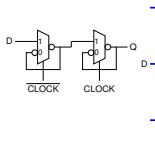


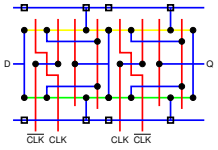


Master Slave D–Type Flip–Flop



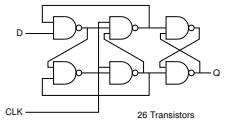


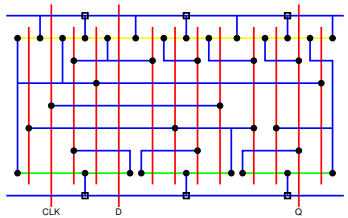




*muliplexor based latches and flip–flops include distictive polysilicon crossover

Edge Triggered D–Type Flip–Flop

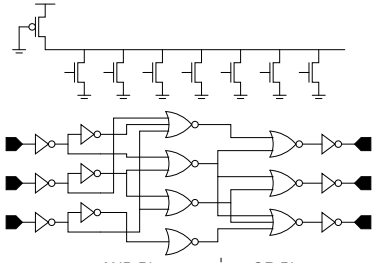




Euler path analysis is applied creatively to these multi–gate cells – gates are often linked via the common gnd/pwr node
Final layouts will be more complex where clock buffers, reset circuitry and metal 2 i/o are included

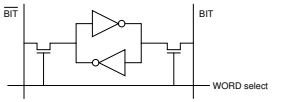
9000

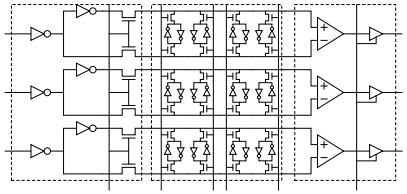
PLA and ROM

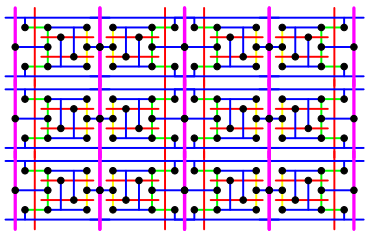


ROM is PLA with
fixed AND (decoder) plane
programmable OR (data) plane

SRAM

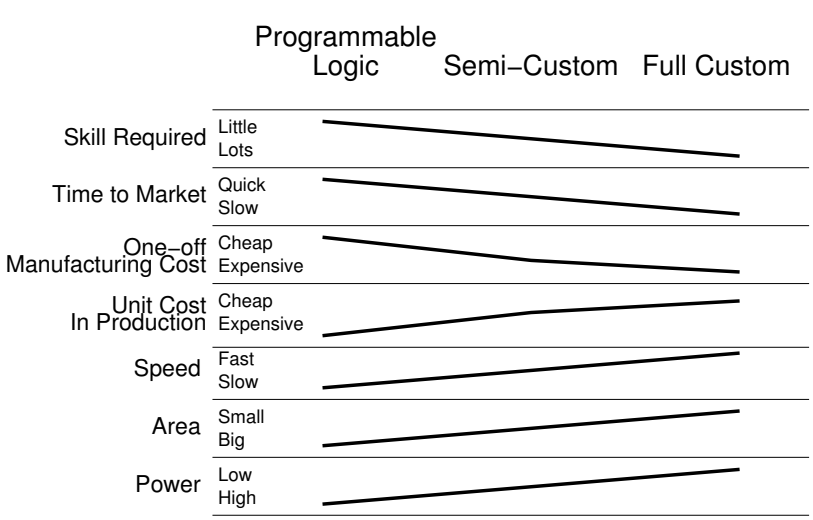






Cells are designed to butt together in two dimensions leading to efficient layout
PLA layout efficiency will depend on the actual function implemented (e.g. number of common product terms)

10000



All design styles need full custom designers
A large ASIC (especially SoC) may mix Semi–Custom and Full Custom

11000