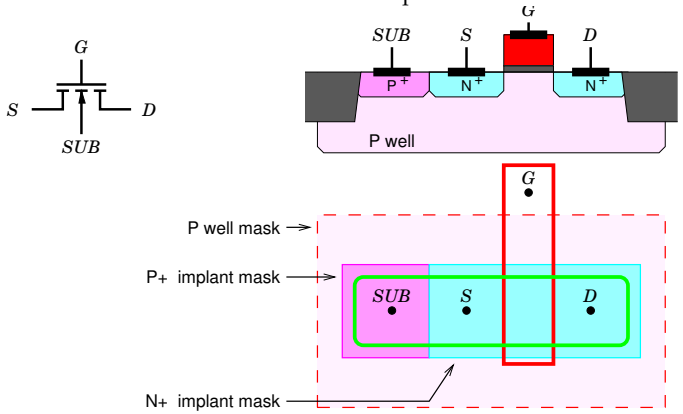
NMOS Transistor – with top substrate connection

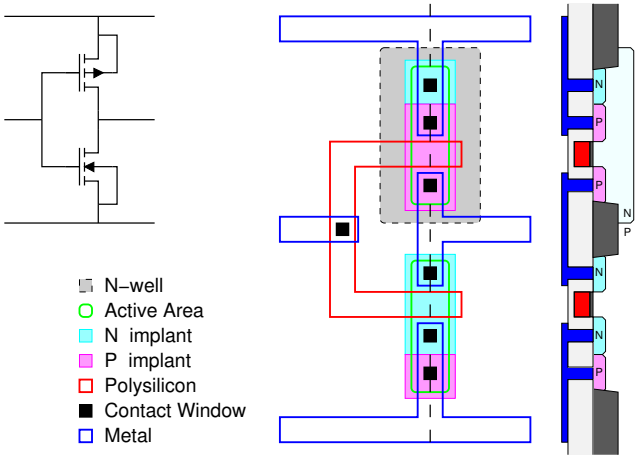


NMOS Transistor – with top substrate connection

Where it is not suitable for substrate connections to be shared, a more complex process is used.

- Five masks must be used to define the transistor:
  - P Well
  - Active Area
  - Polysilicon
  - N+ implant
  - P+ implant
- P Well, for isolation.
- Top *substrate* connection.
- P+/N+ implants produce good *ohmic* contacts.

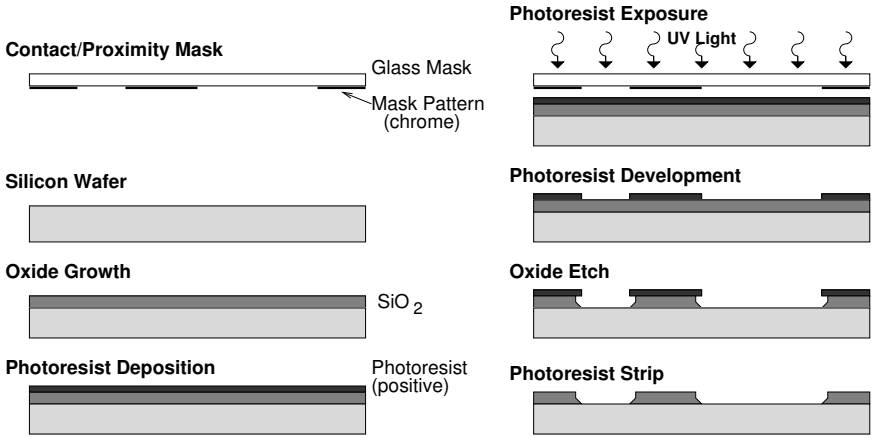
CMOS Inverter



CMOS Inverter

- The process described here is an *N Well process* since it has only an N Well.
  P Well and Twin Tub processes also exist.
- Note that the P-N junction between chip substrate and N Well will remain reverse biased.
  Thus the transistors remain isolated.
- N implant defines NMOS source/drain and PMOS substrate contact.
- P implant defines PMOS source/drain and NMOS substrate contact.

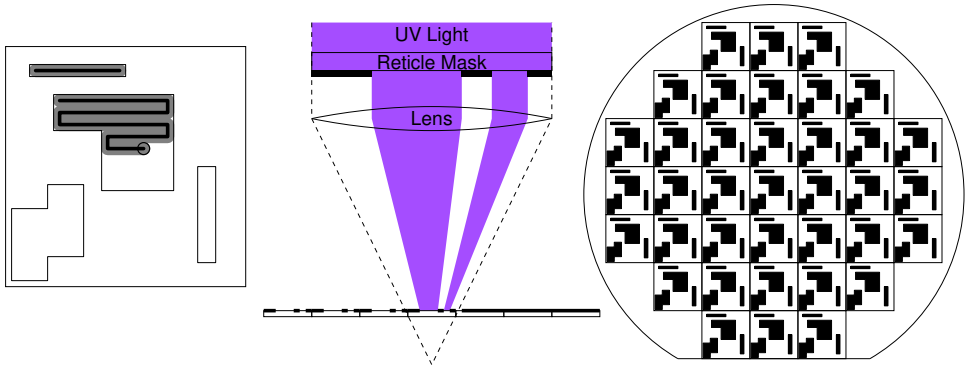
Processing – Photolithography



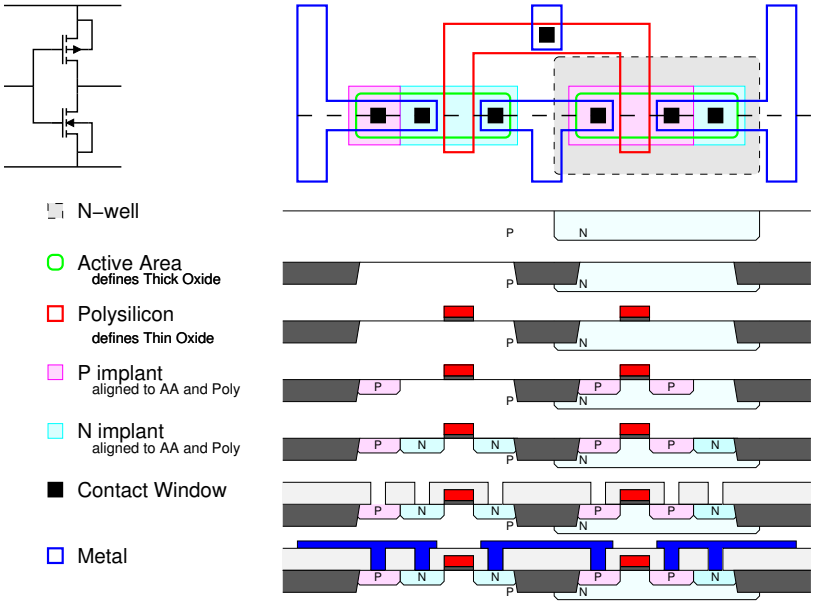
Processing – Mask Making

Reticle written by scanning electron beam

Pattern reproduced on wafer (or contact/proximity mask) by step and repeat with optical reduction

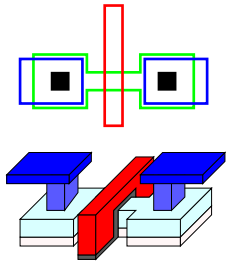


- Optical reduction allows narrower line widths.



CMOS - Short Gate Techiques

Fin FET



- With the aid of trenches we raise the active area above the bulk silicon.
- We can then wrap the gate around the channel.
- Avoids an effect where a channel is created in a region which is closer to the drain than the gate.