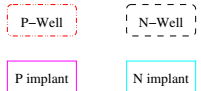
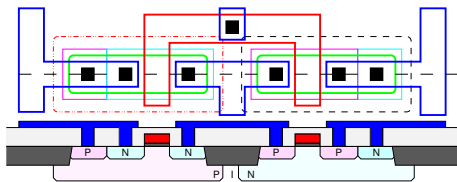


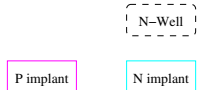
Twin Tub CMOS Process  
with explicit N+ implant mask



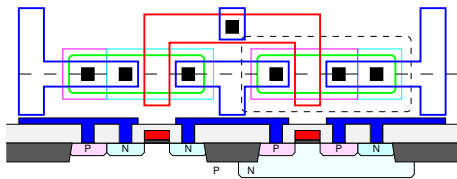
includes combined contact and tap



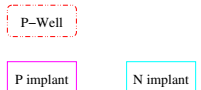
N-Well CMOS Process  
with explicit N+ implant mask



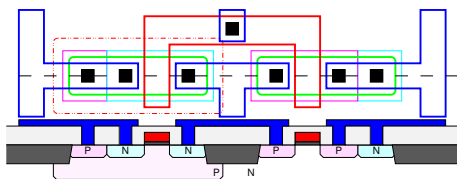
includes combined contact and tap



P-Well CMOS Process  
with explicit N+ implant mask

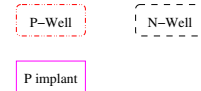


includes combined contact and tap

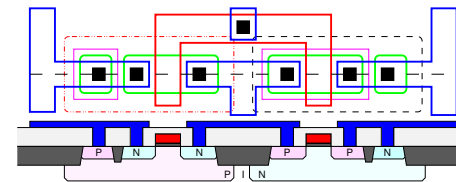


4101

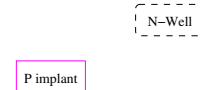
Twin Tub CMOS Process  
without explicit N+ implant mask



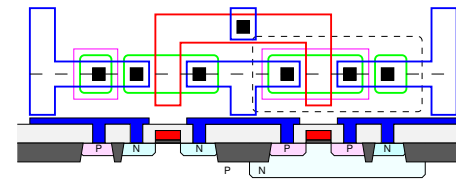
includes separate contact and tap



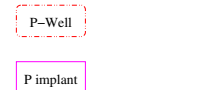
N-Well CMOS Process  
without explicit N+ implant mask



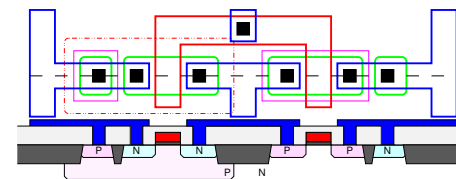
includes separate contact and tap



P-Well CMOS Process  
without explicit N+ implant mask

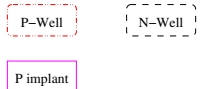


includes separate contact and tap

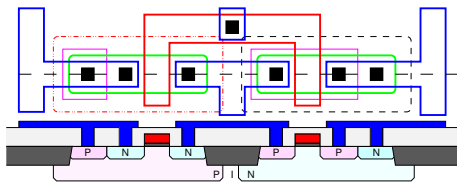


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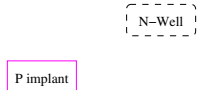
Twin Tub CMOS Process  
without explicit N+ implant mask



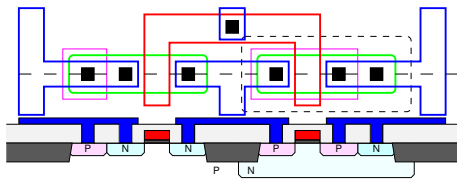
includes combined contact and tap



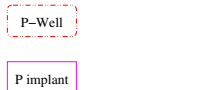
N-Well CMOS Process  
without explicit N+ implant mask



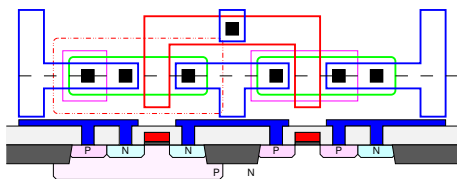
includes combined contact and tap



P-Well CMOS Process  
without explicit N+ implant mask



includes combined contact and tap



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