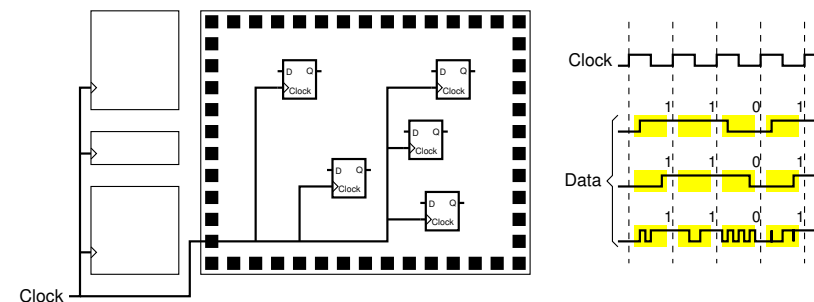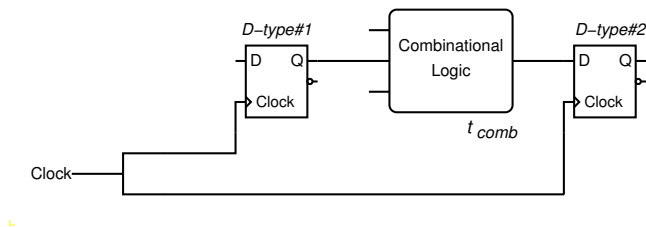## Synchronous Systems

- All parts of the system share the same clock and the same clock edge sensitivity.
- The data may change between active clock transitions but must be stable by the time the next active transition occurs[1].

---

[1]for most systems the *active transition* is the rising edge of the clock

Synchronous Systems - D-type Timing

- Valid data should be present on D input for at least t_{setup} before the active clock edge and at least t_{hold} after the clock edge.
- The minimum D-type cycle time will be limited by the sum $t_{setup} + t_{pQ}$.

Synchronous Systems - Static Timing Analysis (Ideal Clock)
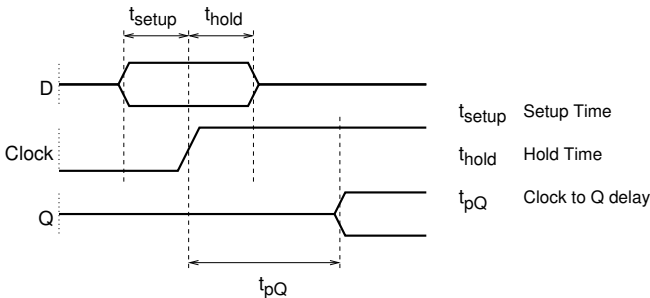

- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup}$$

- To avoid a hold violation:

$$t_{pQ} + t_{comb} > t_{hold}$$

Synchronous Systems
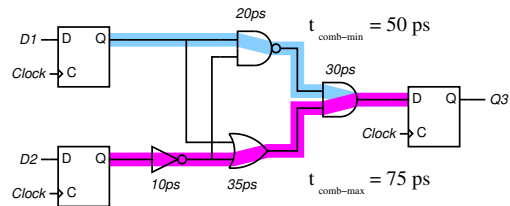
Static Timing Analysis

- Predicts the timing of a circuit without simulation[2]

- Analysis of gate network based on:
  - Propagation delays
  - Set-up and hold times for storage elements
  - Constraints such as desired operating freqency and the timing of inputs and outputs

Note that the examples given here are simplified in that they reduce the propagation delay through a gate to a single number - in reality there are predictable and unpredicatble variations in gate delays which must be accounted for by static timing analysis tools.

---

[2]timing simulations for large digital systems are slow and will usually not catch all edge and coner cases

t$_{comb-min}$ = 50 ps

t$_{comb-max}$ = 75 ps

- To avoid a setup violation:
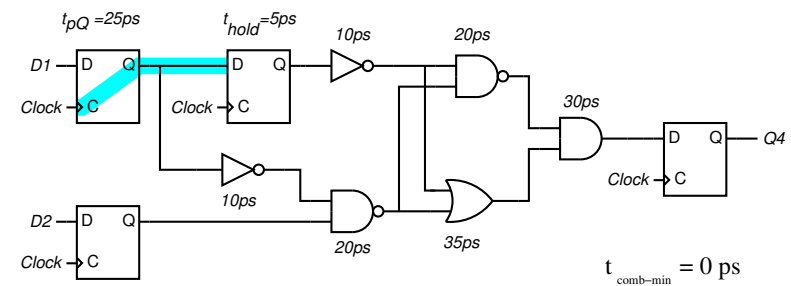
$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup}$$

- To avoid a hold violation:

$$t_{pQ} + t_{comb-min} > t_{hold}$$

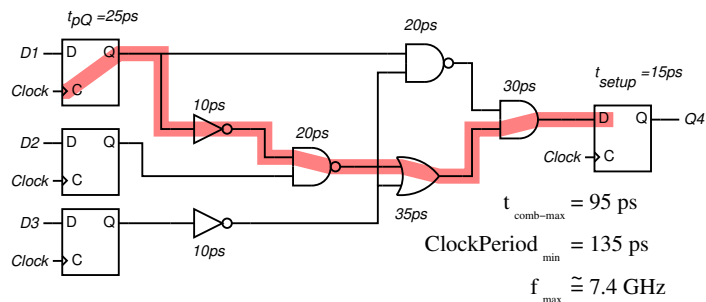20005

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t$_{comb-min}$ = 0 ps

$$t_{pQ} + t_{comb-min} > t_{hold}$$

If we have an ideal clock and $t_{pQ} > t_{hold}$ we won't see hold violations even with if $t_{comb-min} = 0$.

20007

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t$_{comb-max}$ = 95 ps

ClockPeriod$_{min}$ = 135 ps

f$_{max}$ ≅ 7.4 GHz
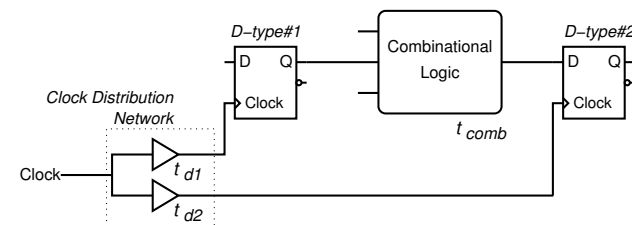
- Critcal path analysis allows us to determine the maximum feasible clock frequency:

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup}$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-max} + t_{setup}}$$

20006

- Clock Distribution

  The process of distributing clocks from a central source gives rise to delays.

  Clock skew is the difference between the arrival times of the clock at different points in the circuit.

- Clock Skew may cause unexpected timing violations
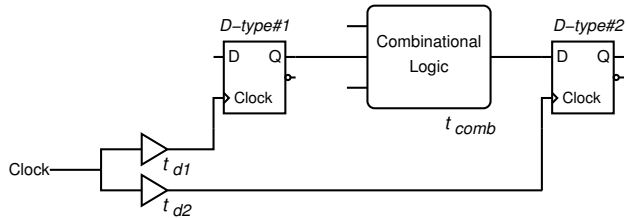
  Hold: if *D-type #1* clocks first, D input of *D-type #2* may change too early[3]

  Setup: if *D-type #1* clocks second, D input of *D-type #2* may change too late

[3]most likely where combinational logic is minimal or absent

20008

- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup} + (t_{d1} - t_{d2})$$

- To avoid a hold violation:

$$t_{pQ} + t_{comb} > t_{hold} + (t_{d2} - t_{d1})$$

20009

$t_{comb-max} = 95$ ps

ClockPeriod$_{min}$ = ps

$f_{max} \cong$ GHz

$t_{comb-min} = 0$ ps $\quad |t_{skew-max}| = 16ps$

- What is the maximum operating frequency of the circuit if the clock skew is no more than 16ps?

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup} + t_{skew}$$

- What is the maximum clock skew that can be tolerated before we have a hold violation?

$$t_{pQ} + t_{comb} > t_{hold} + t_{skew}$$

20010

Critical Path

- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + t_{skew}$$

20011
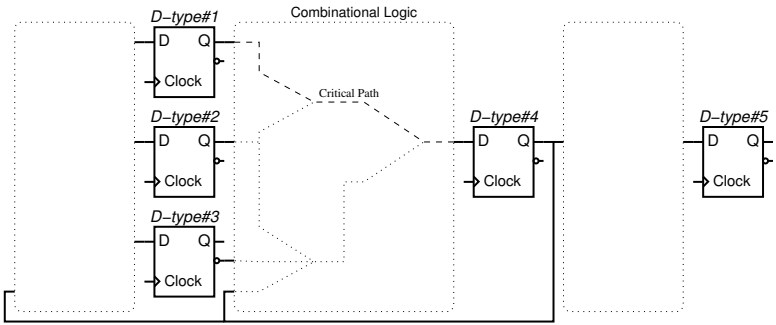
Critical Path

- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d1} - t_{d4})$$

20012

Critical Path
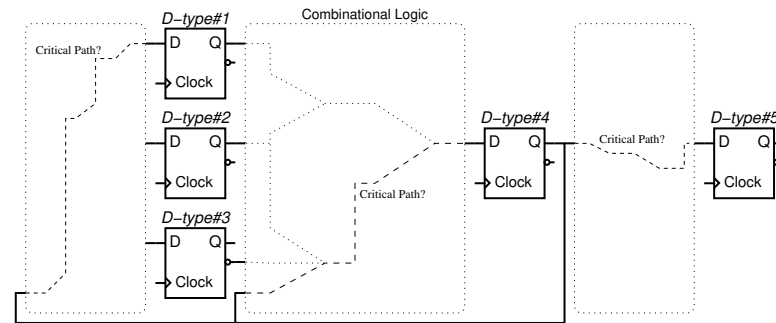
$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

- If we can control the skew (e.g. by increasing t_{d4}), we can ease the timing constraint.[4]

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[4]this may result in the critical path moving to another part of the circuit
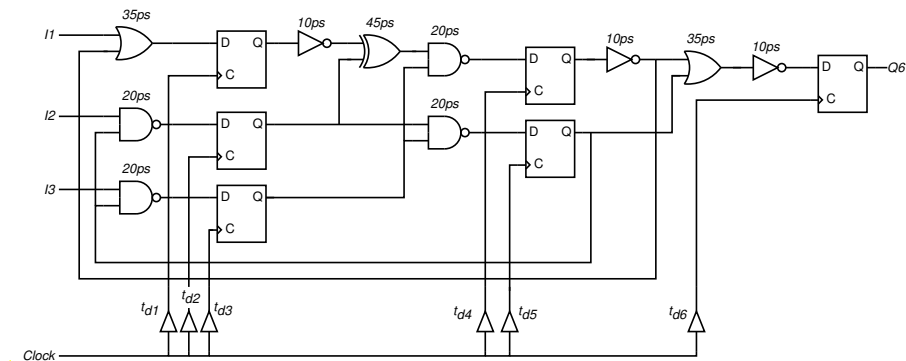
- Calculate f_{max} in the presence of intentional clock skew.
- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}, t_{d5}, t_{d6}
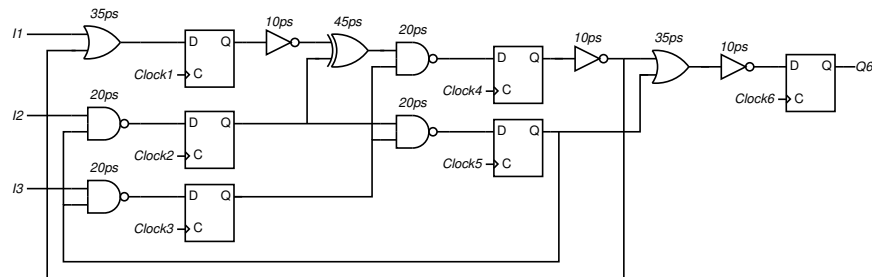
- Calculate f_{max} in the presence of intentional clock skew.
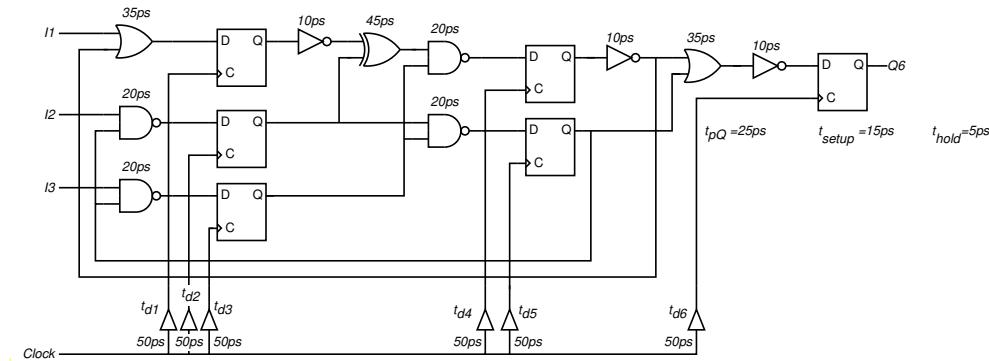
- Calculate f_{max} in the presence of intentional clock skew.
- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}, t_{d5}, t_{d6}
  Initially set all to a minimum value (in this case 50ps)

Slide 20017

35ps, 10ps, 45ps, 20ps, 10ps, 35ps, 10ps

I1, I2, I3

20ps, 20ps

$t_{pQ} = 25ps$ $t_{setup} = 15ps$ $t_{hold} = 5ps$

Q6

t_{d1} t_{d2} t_{d3} t_{d4} t_{d5} t_{d6}

50ps 50ps 50ps 50ps 50ps 50ps

Clock

- Calculate f_{max} in the presence of intentional clock skew.
- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}, t_{d5}, t_{d6}

$\Rightarrow$ Identify longest timing paths

20017

Slide 20019

35ps, $t_{pQ} = 25ps$, 10ps A 45ps, 20ps, $t_{setup} = 15ps$, 10ps, 35ps, 10ps

I1, I2, I3

20ps, 20ps, 20ps

Q6

t_{d1} t_{d2} t_{d3} t_{d4} t_{d5} t_{d6}

Clock

$t_{d1} = 50$ ps $t_{d2} = 50$ ps
$t_{d3} = 50$ ps $t_{d4} = 50$ ps
$t_{d5} = 50$ ps $t_{d6} = 50$ ps

$t_{comb-A} = 75$ ps

$ClockPeriod_{min} = 115$ ps

$f_{max} \cong 8.7$ GHz

$$ClockPeriod > t_{pQ} + t_{comb-A} + t_{setup} + (t_{d1} - t_{d4})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-A} + t_{setup} + (t_{d1} - t_{d4})}$$

20019

Slide 20018

35ps, 10ps A 45ps, 20ps, C 10ps, 35ps, 10ps

I1, I2, I3

20ps, 20ps, 20ps

B, D, E

$t_{pQ} = 25ps$ $t_{setup} = 15ps$ $t_{hold} = 5ps$

Q6

t_{d1} t_{d2} t_{d3} t_{d4} t_{d5} t_{d6}

50ps 50ps 50ps 50ps 50ps 50ps

Clock

$t_{path-A} = 115$ ps
$t_{path-B} = 105$ ps
$t_{path-C} = 95$ ps
$t_{path-D} = 85$ ps
$t_{path-E} = 85$ ps
$t_{path-crit} = 115$ ps

- Calculate f_{max} in the presence of intentional clock skew.
- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}, t_{d5}, t_{d6}

$\Rightarrow$ Identify longest timing paths

$$t_{path} = t_{pQ} + t_{comb} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

20018

Slide 20020

35ps, 10ps, 45ps, 20ps, 10ps, 35ps, 10ps

I1, I2, I3

20ps, 20ps, 20ps

Q6

$t_{pQ} = 25ps$ $t_{setup} = 15ps$ $t_{hold} = 5ps$

t_{d1} t_{d2} t_{d3} t_{d4} t_{d5} t_{d6}

Clock

$t_{d1} =$ ps $t_{d2} =$ ps
$t_{d3} =$ ps $t_{d4} =$ ps
$t_{d5} =$ ps $t_{d6} =$ ps

$ClockPeriod_{min} =$ ps

$f_{max} \cong$ GHz

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})}$$

20020

Synchronous Systems - Static Timing Analysis (inc. clock skew)

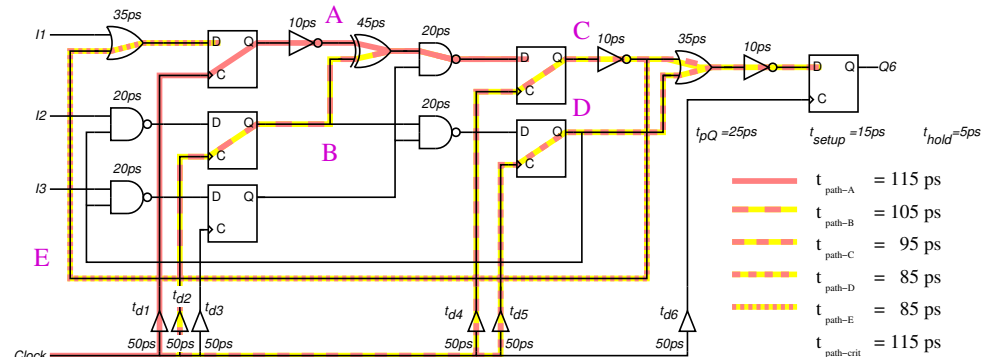$t_{pQ} = 25ps$ $t_{setup} = 15ps$ $t_{hold} = 5ps$

t_{path-A}	= 115 ps
t_{path-B}	= 105 ps
t_{path-C}	= 95 ps
t_{path-D}	= 85 ps
t_{path-E}	= 85 ps
$t_{path-crit}$	= 115 ps

$\Rightarrow$ Initially try increasing t_{d4} by 20ps

20021

Synchronous Systems - Static Timing Analysis (inc. clock skew)

$t_{d1}=$	ps	$t_{d2}=$	ps
$t_{d3}=$	ps	$t_{d4}=$	ps
$t_{d5}=$	ps	$t_{d6}=$	ps

$t_{pQ} = 25ps$ $t_{setup} = 15ps$ $t_{hold} = 5ps$

ClockPeriod$_{min}$ =   ps

$f_{max} \cong$ GHz

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

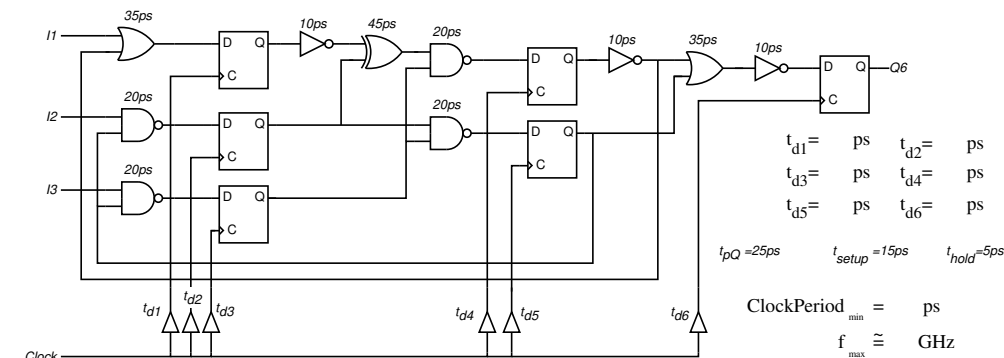$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})}$$

20023

Synchronous Systems - Static Timing Analysis (inc. clock skew)
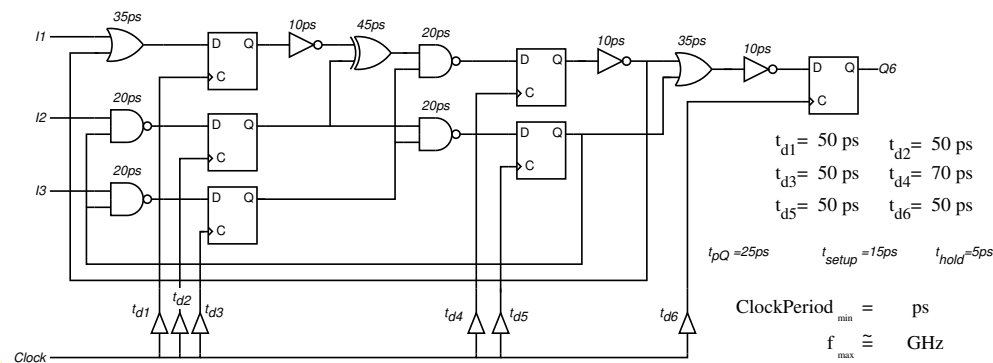
$t_{d1}=$ 50 ps		$t_{d2}=$ 50 ps	
$t_{d3}=$ 50 ps		$t_{d4}=$ 70 ps	
$t_{d5}=$ 50 ps		$t_{d6}=$ 50 ps	

$t_{pQ} = 25ps$ $t_{setup} = 15ps$ $t_{hold} = 5ps$

ClockPeriod$_{min}$ =   ps

$f_{max} \cong$ GHz

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})}$$

20022

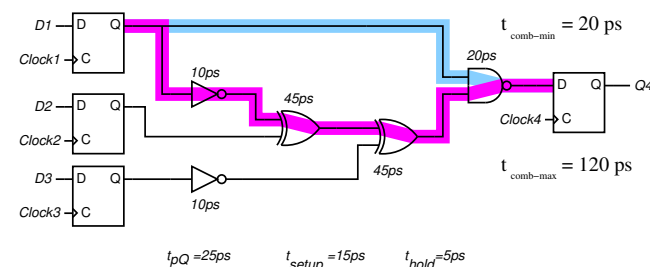## Synchronous Systems - Static Timing Analysis (inc. clock skew)

$t_{comb-min}$ = 20 ps

$t_{comb-max}$ = 120 ps

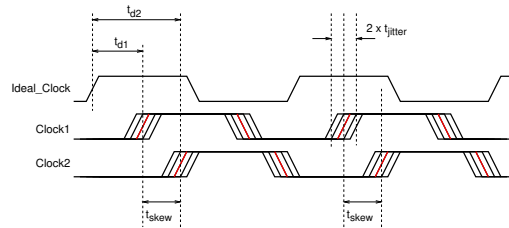$t_{pQ} = 25ps$ $t_{setup} = 15ps$ $t_{hold} = 5ps$

- Calculate f_{max} in the presence of intentional clock skew.

- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4} given that the minimum delay through the clock tree is 50ps

remember to check for hold violations

20024

## Synchronous Systems - Jitter

- Jitter

  Jitter is the cycle-by-cycle variation in the arrival time of the clock.

- Caused by

  - Variation in frequency/phase of clock source[5]
  - Power supply noise affecting clock distribution
  - Cross-talk affecting clock distribution

- Jitter may cause unexpected timing violations

---

[5]primary clock source or Phase-Locked Loop (PLL)

Synchronous Systems - Static Timing Analysis (skew + jitter)

$$t_{comb-min} = 0 \text{ ps} \qquad |t_{skew-max}| = 16ps \qquad \text{ClockPeriod} \cong 167 \text{ ps}$$
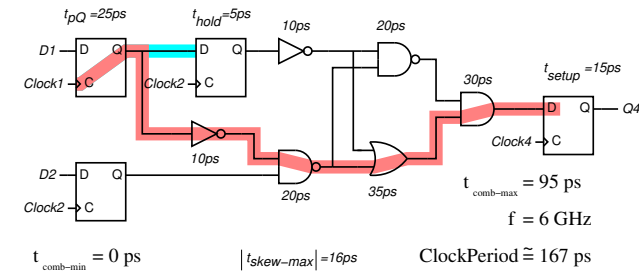
- What is the maximum jitter that can be tolerated given an operating frequency of 6GHz and clock skew of no more than 16ps?[6]
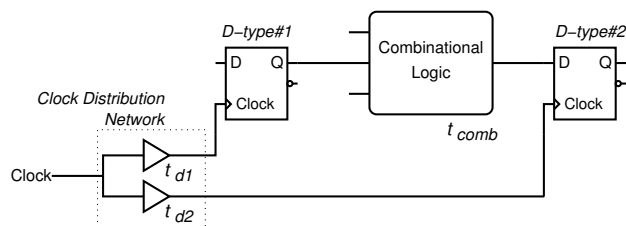
$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup} + t_{skew} + 2 \times t_{jitter}$$

$$t_{pQ} + t_{comb-min} > t_{hold} + t_{skew} + 2 \times t_{jitter}$$

---

[6]remember to consider both setup and hold violations

Synchronous Systems - Jitter

- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup} + (t_{d1} - t_{d2}) + 2 \times t_{jitter}$$

- To avoid a hold violation:

$$t_{pQ} + t_{comb} > t_{hold} + (t_{d2} - t_{d1}) + 2 \times t_{jitter}$$