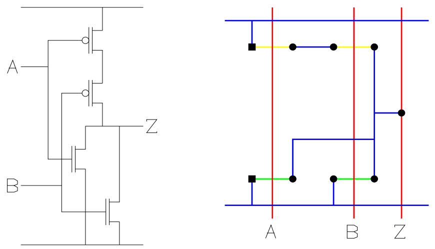
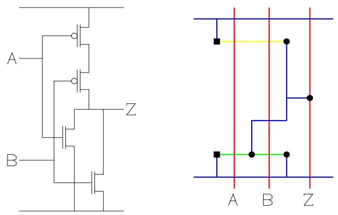
A logical approach to gate layout.

- *All complementary gates may be designed using a single row of n-transistors above or below a single row of p-transistors, aligned at common gate connections.*



Euler Path

- For the majority of these gates we can find an arrangement of transistors such that we can butt adjoining transistors.
  - Careful selection of transistor ordering.
  - Careful orientation of transistor source and drain.
- Referred to as *line of diffusion*.



Finding an Euler Path

Computer Algorithms

- It is relatively easy for a computer to consider all possible arrangements of transistors in search of a suitable Euler path.

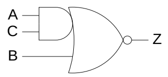
  This is not so easy for the human designer.

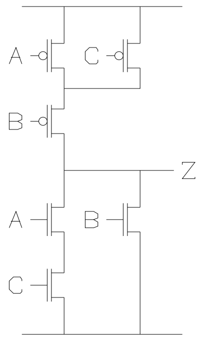
One Human Algorithm

- Find a path which passes through all n-transistors exactly once.
- Express the path in terms of the gate connections.
- Is it possible to follow a similarly labelled path through the p-transistors?
  - Yes – you've succeeded.
  - No – try again (you may like to try a p path first this time).

Finding an Euler Path

$Z = \overline{(A \bullet C) + B}$



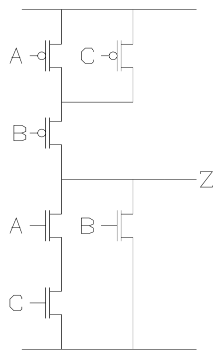


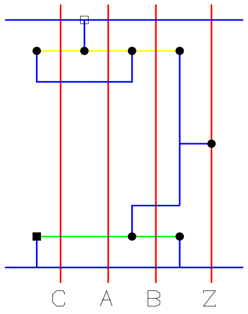
A–C–B
B–A–C
B–C–A
C–A–B ⇐

A–B–C
A–C–B
B–A–C
B–C–A
C–A–B ⇐
C–B–A

Here there are four possible Euler paths.

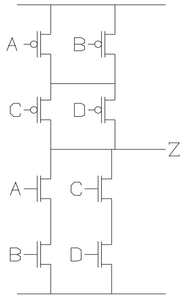
Finding an Euler Path

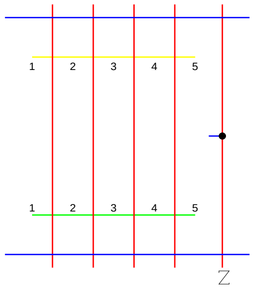




Euler Path Example

$Z = \overline{(A \bullet B) + (C \bullet D)}$





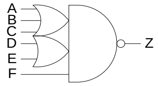
1. Find Euler path
2. Label poly columns
3. Route power nodes
4. Route output node
5. Route remaining nodes
6. Add taps[1] for PMOS and NMOS

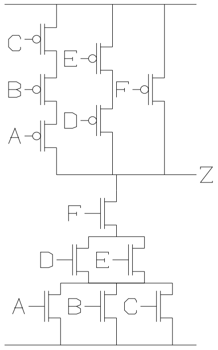
A combined contact and tap, ■, may be used only where a power contact exists at the end of a line of diffusion. Where this is not the case a simple tap, ⊟, should be used.

[1] 1 tap is good for about 6 transistors – insufficient taps may leave a chip vulnerable to latch-up

Finding an Euler Path

$Z = \overline{(A+B+C) \bullet (D+E) \bullet F}$

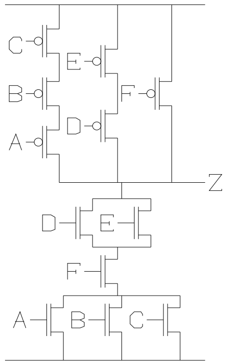


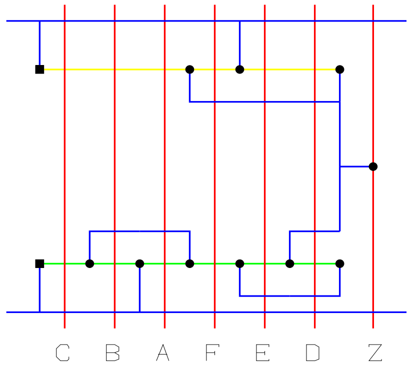


No possible path through n-transistors!

Finding an Euler Path

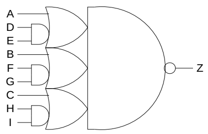
$Z = \overline{(A+B+C) \bullet (D+E) \bullet F}$

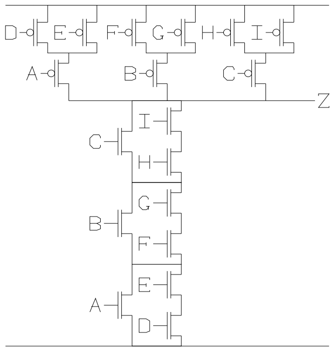




Finding an Euler Path

$$Z = \overline{(A+(D \bullet E)) \bullet (B+(F \bullet G)) \bullet (C+(H \bullet I))}$$





No possible path through p-transistors.
No re-arrangement will create a solution!