ELEC3221

Digital IC & Sytems Design

Iain McNally

≈ 15 lectures

Koushik Maharatna

≈ 15 lectures

1001

Digital IC & Sytems Design

- Assessment

  10% Coursework L-Edit Gate Design (BIM)

  90% Examination

- Books

  Integrated Circuit Design

  a.k.a. Principles of CMOS VLSI Design - A Circuits and Systems Perspective

  Neil Weste & David Harris

  Pearson, 2011

  Digital System Design with SystemVerilog

  Mark Zwolinski

  Pearson Prentice-Hall, 2010

Iain McNally

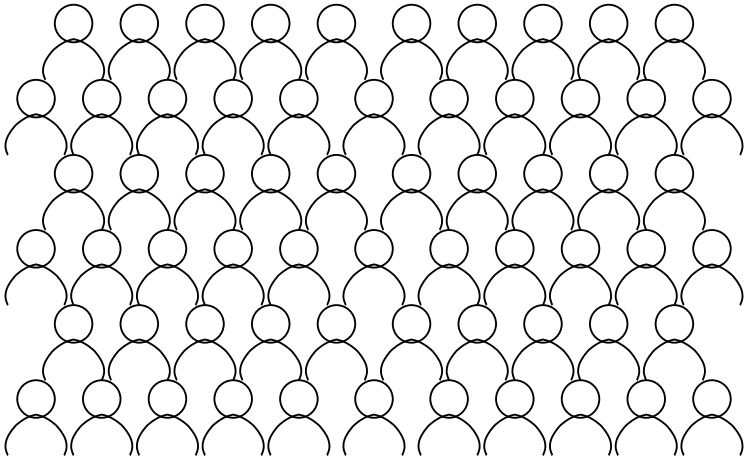
Integrated Circuit Design

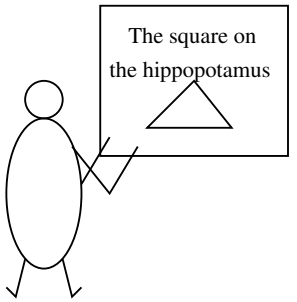
- Content
  - Introduction
  - Overview of Technologies
  - Layout
  - CMOS Processing
  - Design Rules and Abstraction
  - Cell Design and Euler Paths
  - System Design using Standard Cells
  - Pass Transistor Circuits
  - Latches and Flip-Flops
  - PLAs, ROMs, RAMs
  - Wider View
- Notes & Resources

  `https://secure.ecs.soton.ac.uk/notes/bim/notes/icd/`

Lecture Style

Lecture **(1)** A method for the transfer of information from the notes of the lecturer to the notes of the student without passing through the brains of either.





Lecture Style

Lecture (2) A method for the transfer of information from the notes of the lecturer to the brain of the student.

- Pre-written lecture notes:
  - Beautiful pictures
  - Economy of words
- Lecturer Input:
  - Attend
  - Explain
  - Answer questions
- Student Input:
  - Attend
  - Ask Questions
  - Understand

Lecture Style

Lecture (2) A method for the transfer of information from the notes of the lecturer to the brain of the student.

- Pre-written lecture notes:

  Beautiful pictures

  Economy of words

- Lecturer Input:

  Attend

  Explain

  Answer questions

- Student Input:

  Attend

  Ask Questions

  Understand

  Make some notes

Note Taking

It's a long time between now and an exam worth 90% of the module.

- Annotate Printed Copies
  suggest 4-UP versions to save paper
- Annotate PDF Copies
  this works well on a tablet
- Another carefully chosen strategy[1]

[1] some students will always make time to review the material and make notes soon after lecture with the aid of text book and other sources

History

1947 First Transistor

John Bardeen, Walter Brattain, and William Shockley (Bell Labs)

1952 Integrated Circuits Proposed

Geoffrey Dummer (Royal Radar Establishment) - *prototype failed...*

1958 First Integrated Circuit

Jack Kilby (Texas Instruments) - *Co-inventor*

1959 First Planar Integrated Circuit

Robert Noyce (Fairchild) - *Co-inventor*

1961 First Commercial ICs

Simple logic functions from TI and Fairchild

1965 Moore's Law

Gordon Moore (Fairchild) observes the trends in integration.

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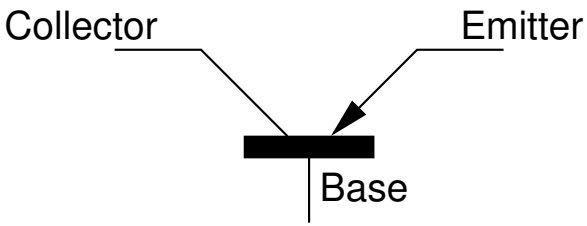
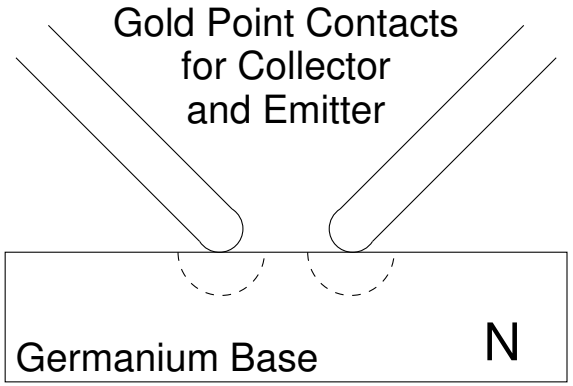
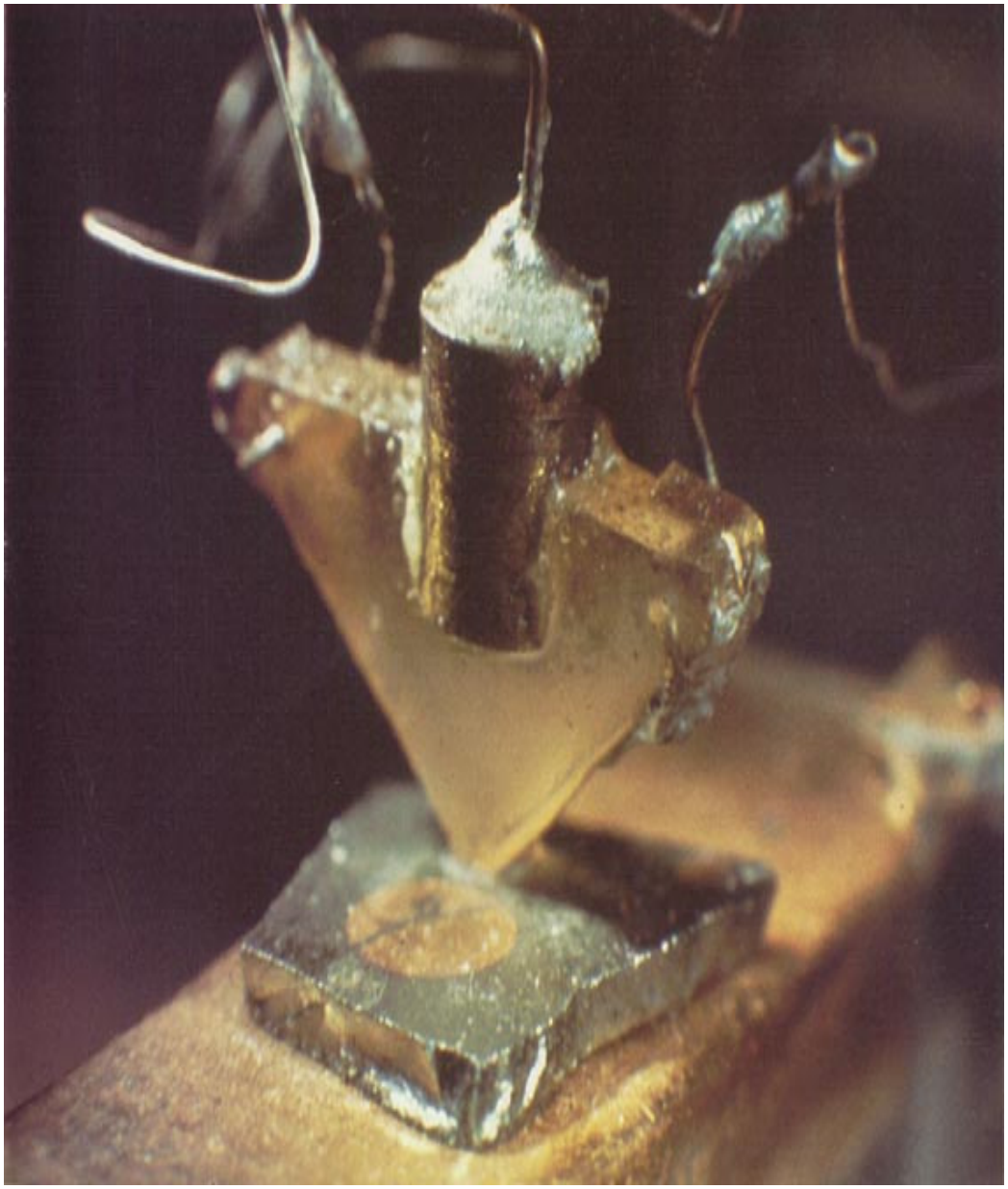
1947 Point Contact Transistor





Each contact creates a metal/semiconductor (Schottky) diode

Depletion regions are shown for zero bias voltage.



Source: Bell Labs

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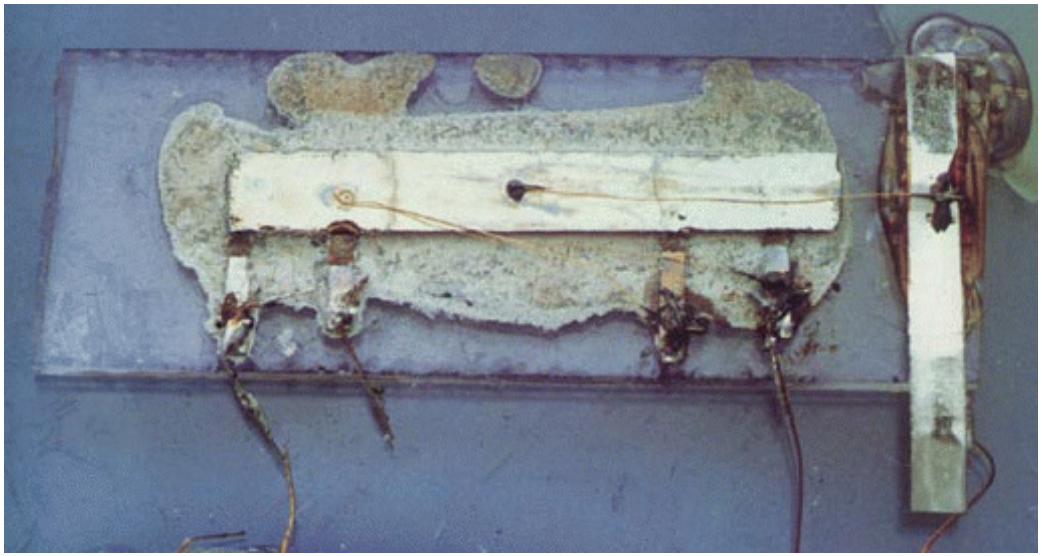
1958 First Integrated Circuit

1 Transistor

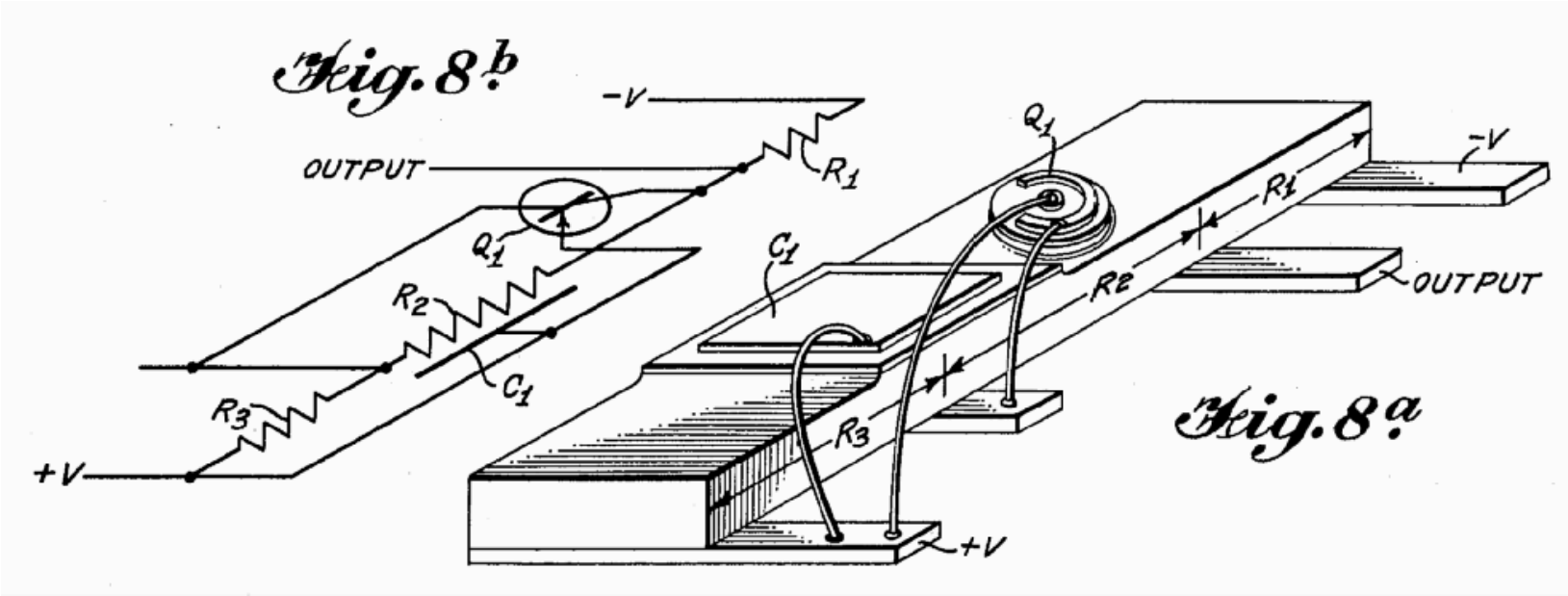
1 Capacitor

3 Resistors

Hand soldered interconnect



Source: Texas Instruments



Source: Jack Kilby (Patent Application)

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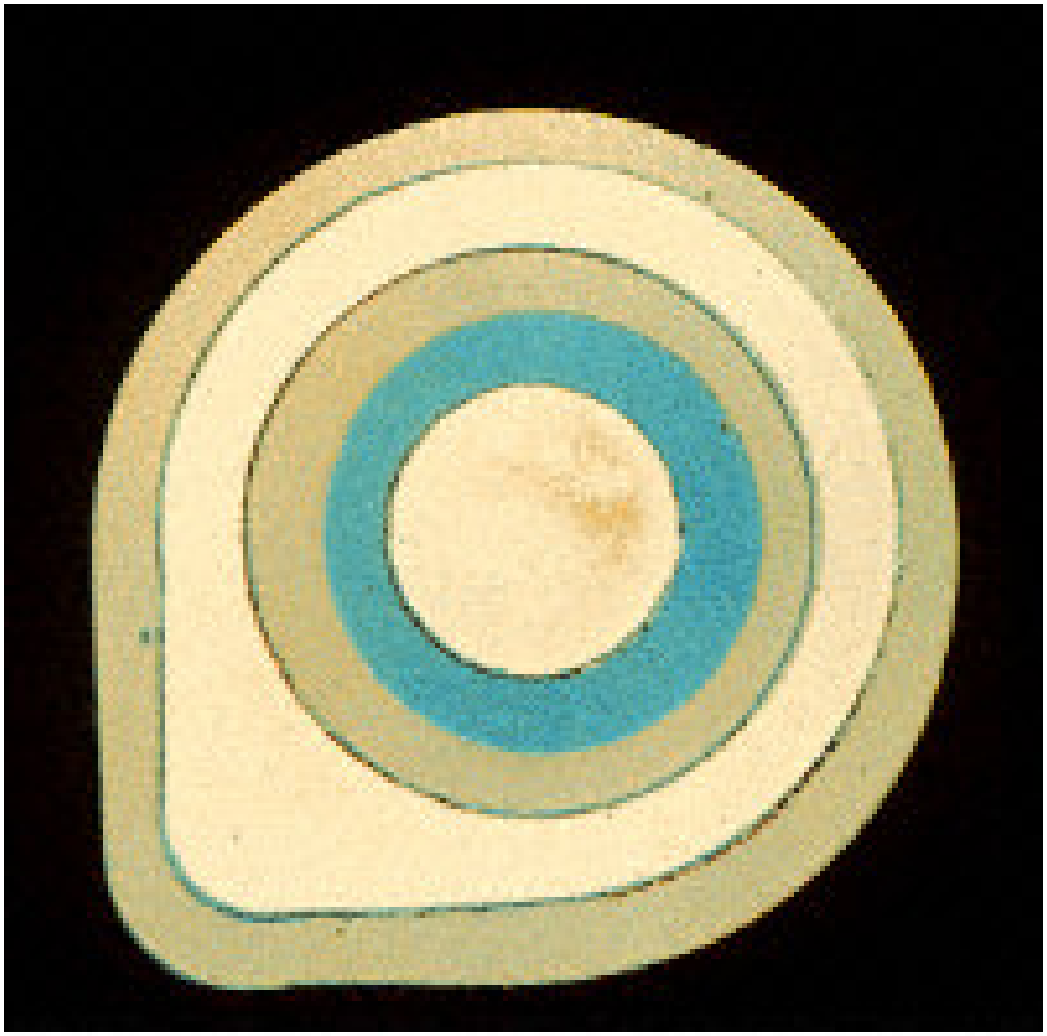

Source: Fairchild

April 25, 1961 R. N. NOYCE 2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959 3 Sheets-Sheet 2

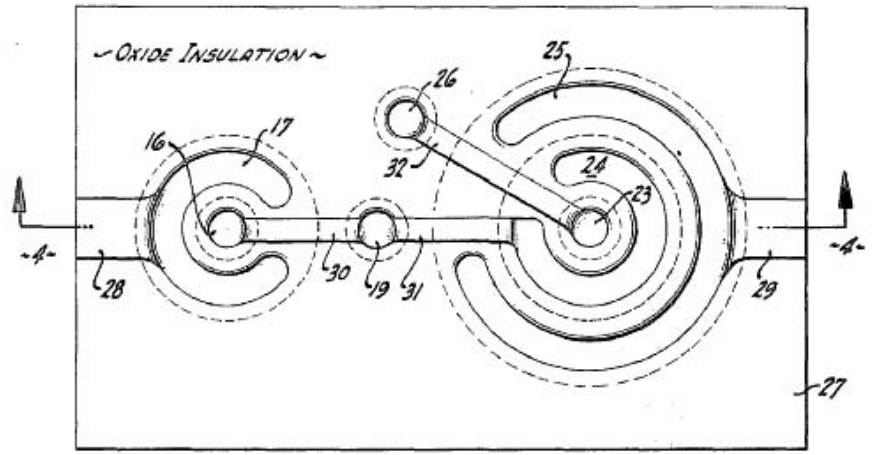

FIG. 3

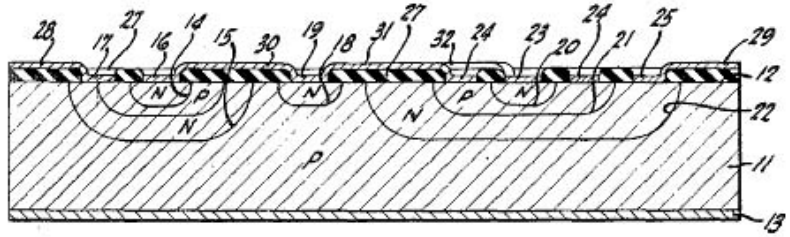

FIG. 4

Source: Robert Noyce (Patent Application)

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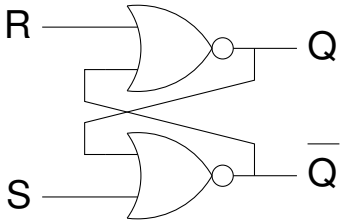
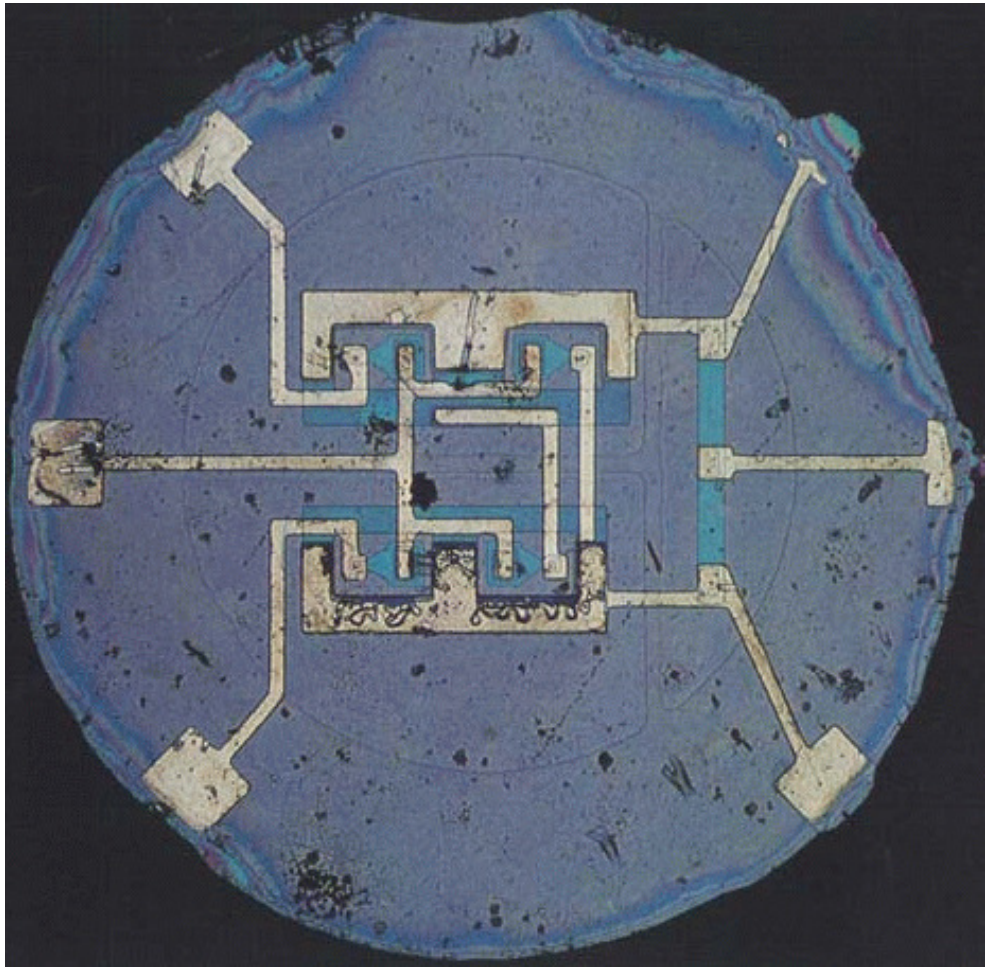
Fairchild Bipolar RTL RS Flip−Flop

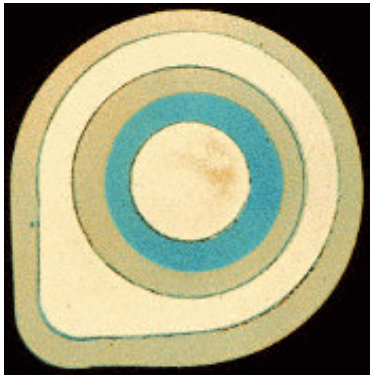




Source: Fairchild

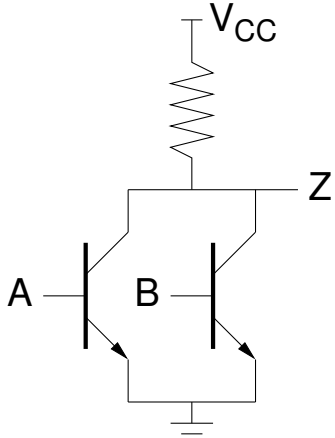
Using

- Planar Bipolar Transistors



Source: Fairchild

- Back to back PN junctions to provide isolation
- Integrated interconnect
- Resistor Transistor Logic



RTL NOR gate

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Moore's Law

Predicts exponential growth in the number of components per chip.

1965 - 1975 Doubling Every Year

In 1965 Gordon Moore observed that the number of components per chip had doubled every year since 1959 and predicted that the trend would continue through to 1975.

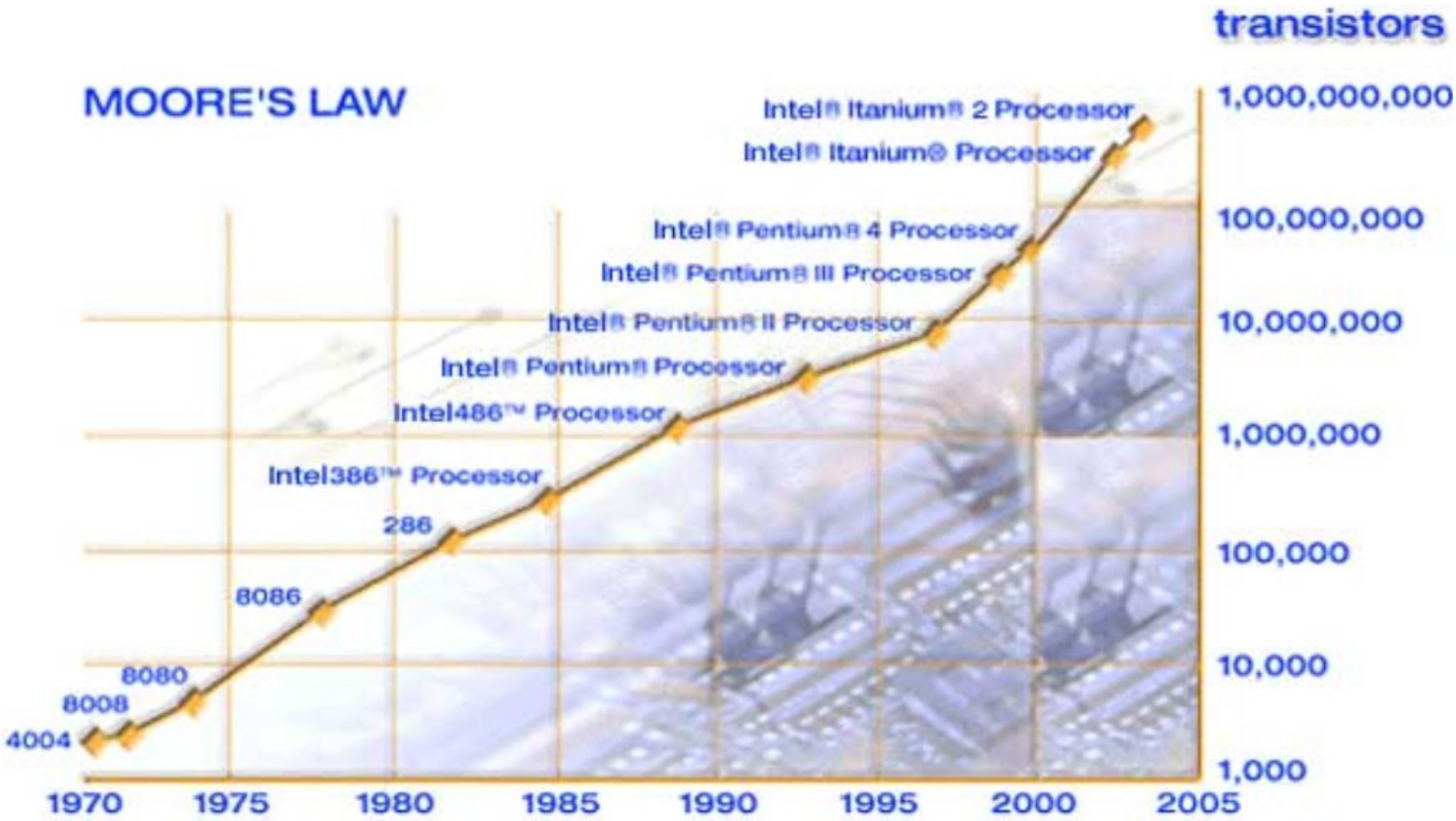
Moore describes his initial growth predictions as ”ridiculously precise”.

1975 - 20?? Doubling Every Two Years

In 1975 Moore revised growth predictions to doubling every two years.

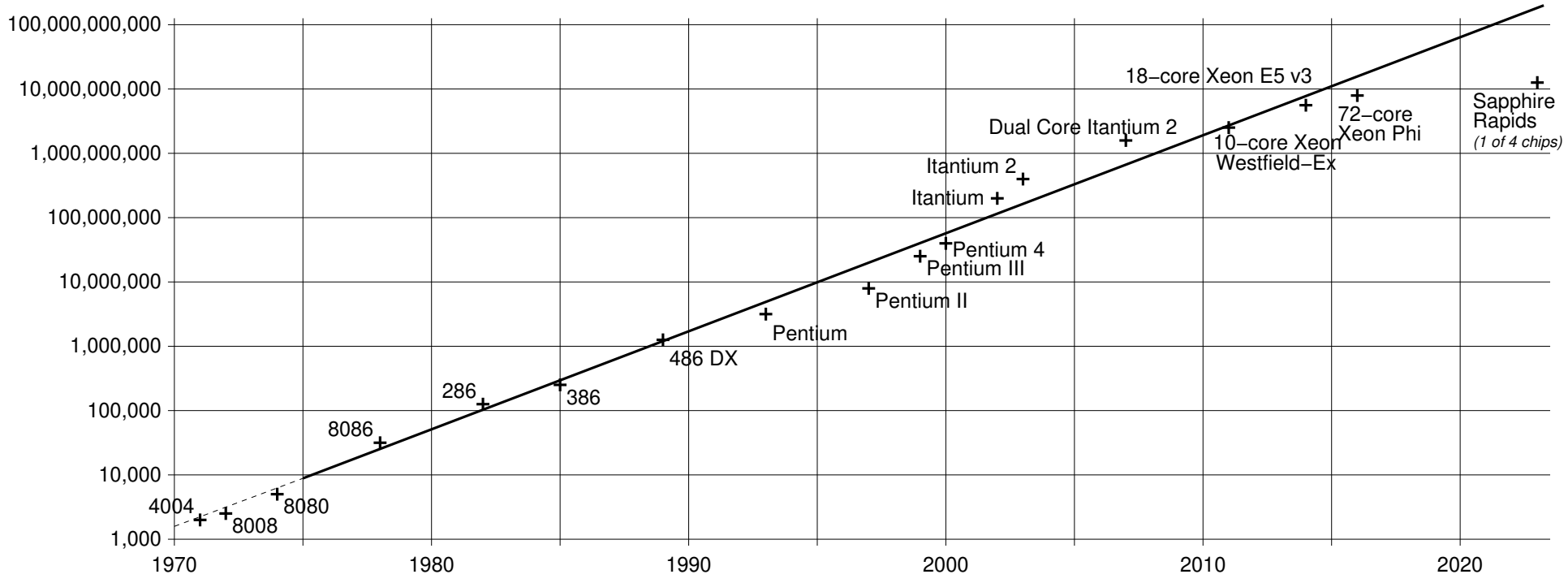
Growth would now depend only on process improvements rather than on more efficient packing of components.

In 2000 he predicted that the growth would continue at the same rate for another 10-15 years before slowing due to physical limits.



Source: Intel

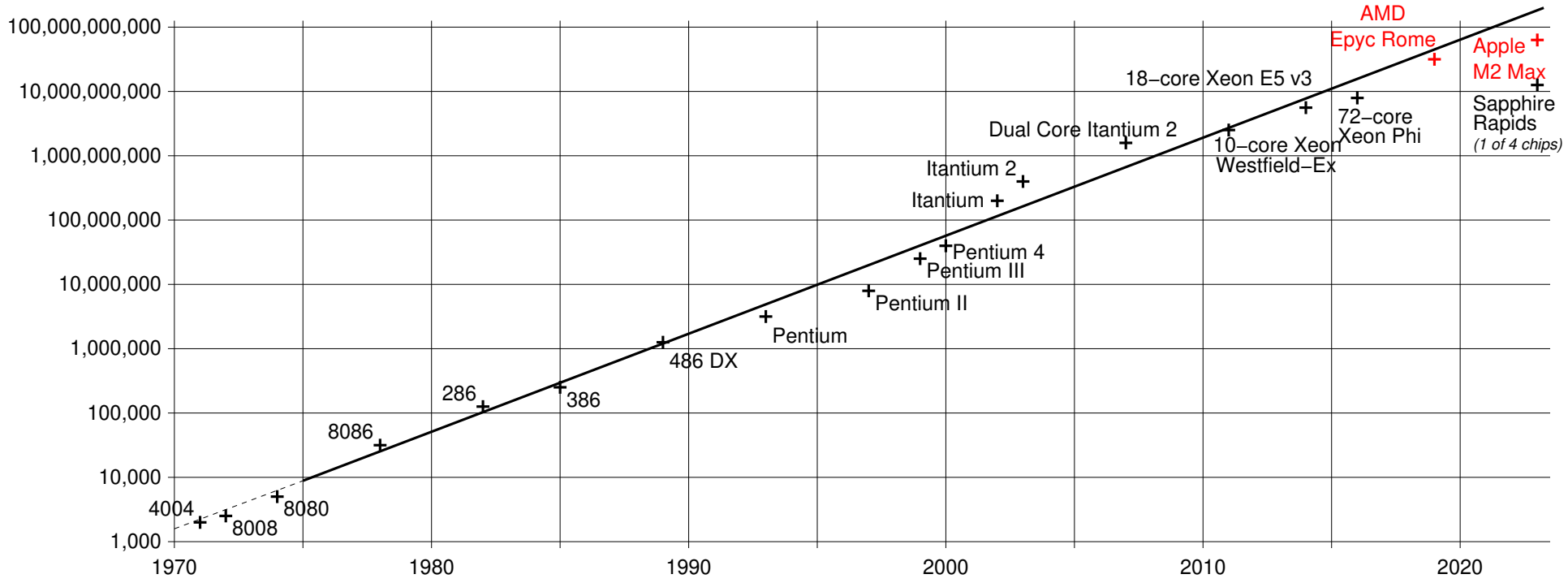
Moore's Law at Intel[2]



[2]Intel was founded by Gordon Moore and Robert Noyce from Fairchild

History

Moore's Law at Intel[3] + Apple/TSMC, AMD/TSMC



[3]Intel has had some hiccups recently - Apple/TSMC and AMD/TSMC appear to be in front

Moore's Law; a Self-fulfilling Prophesy

The whole industry has used the Moore's Law curve to plan new fabrication facilities.

Slower - wasted investment

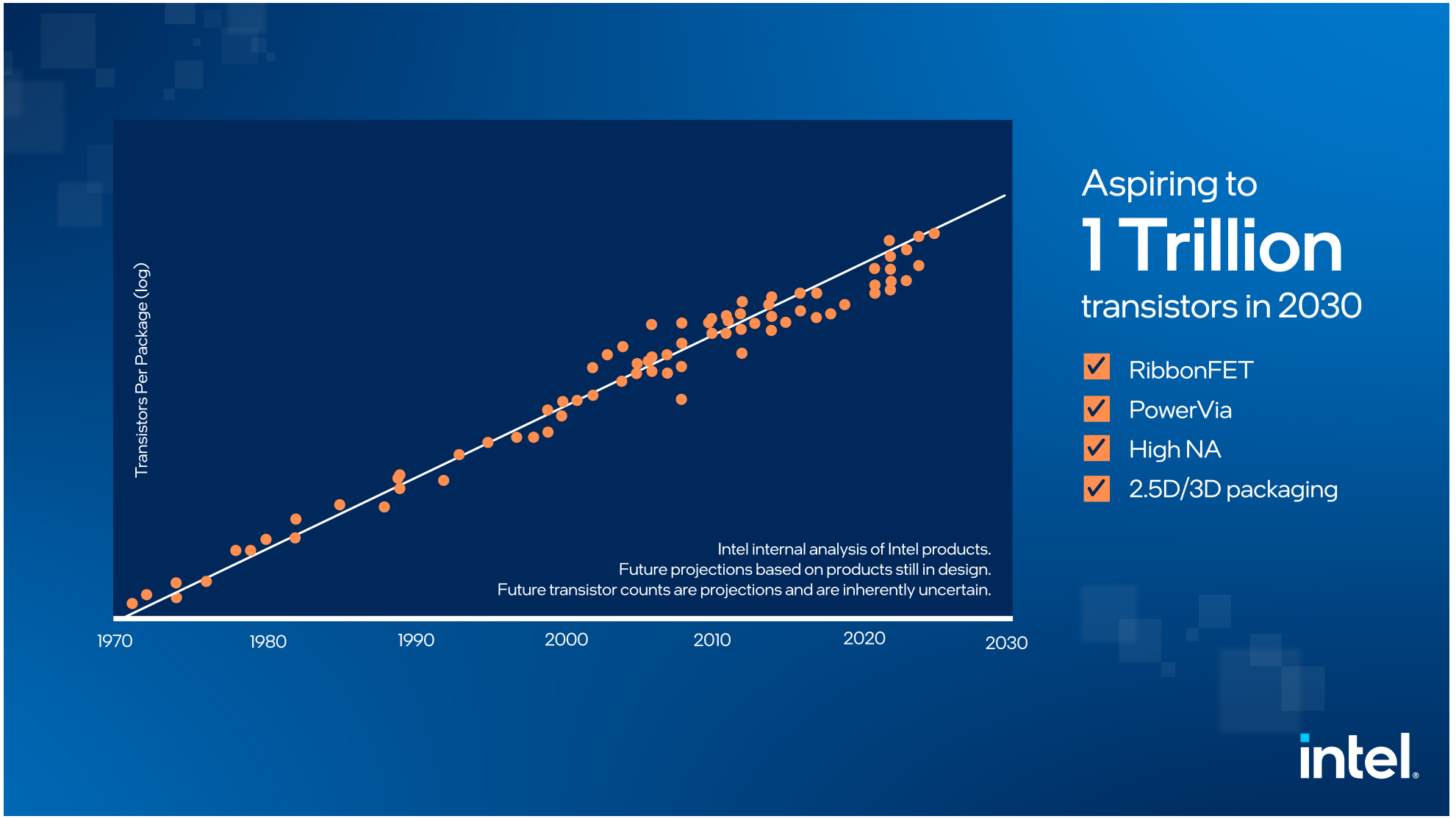
Must keep up with the Joneses[4].

Faster - too costly

Cost of capital equipment to build ICs doubles approximately every 4 years.

Moore's law is not dead (at least not quite). As transistor dimensions approach the size of a few tens of molecules, new techniques are needed. Recent developments include the stacking of transistors in V-NAND Flash memory to achieve higher densities.

[4] or the Intels



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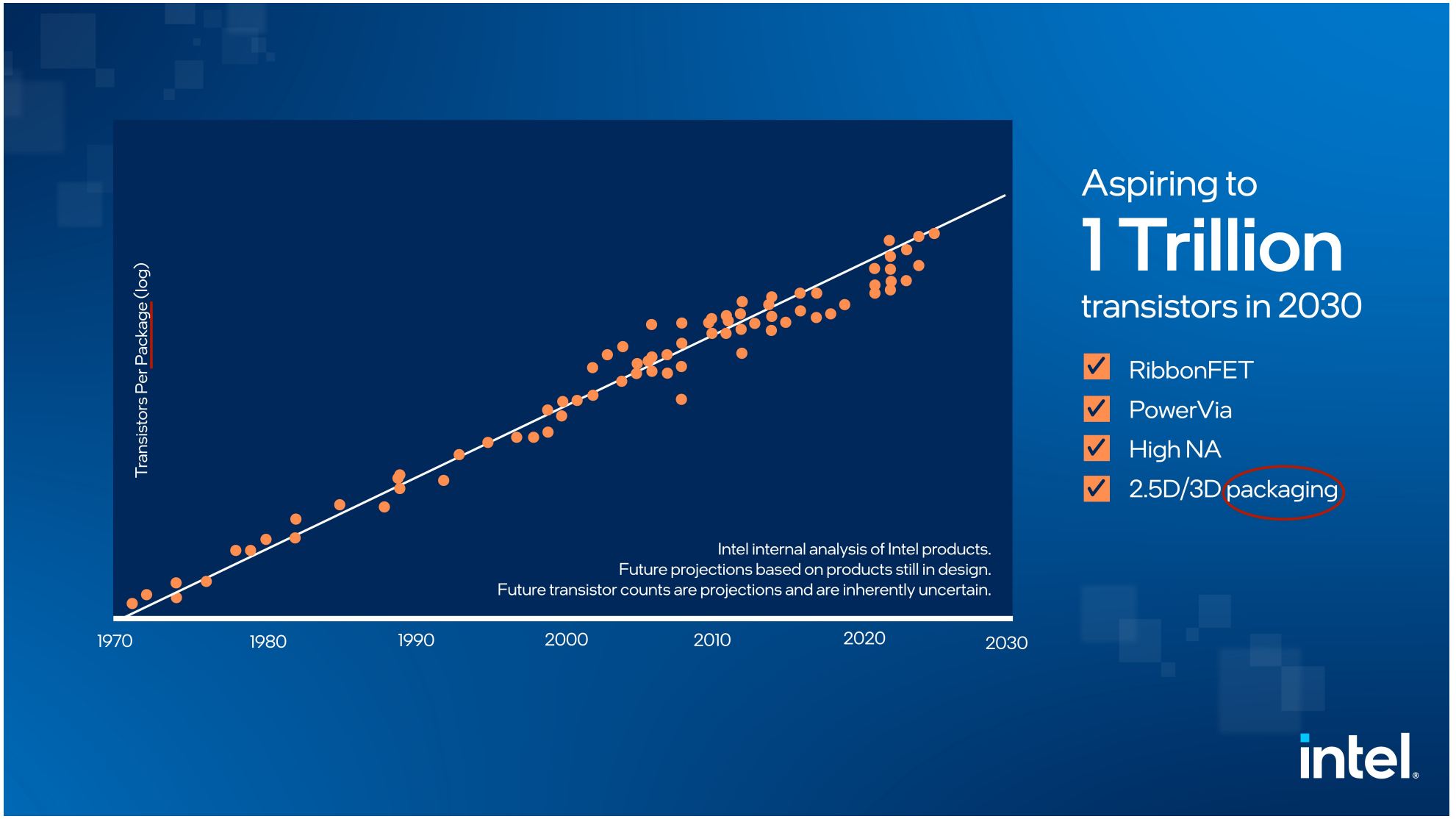
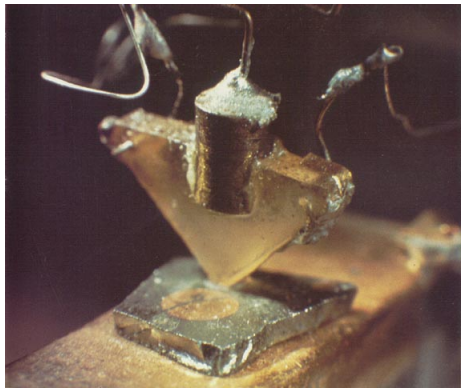
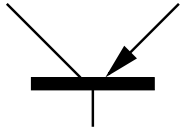


Source: Intel

1947 Point Contact transistor

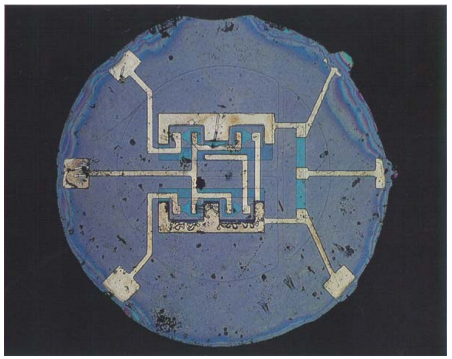


Source: Bell Labs

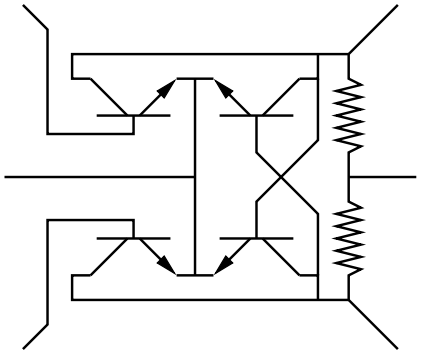


1961 Fairchild Bipolar RTL RS Flip–Flop

(4 Transistors)

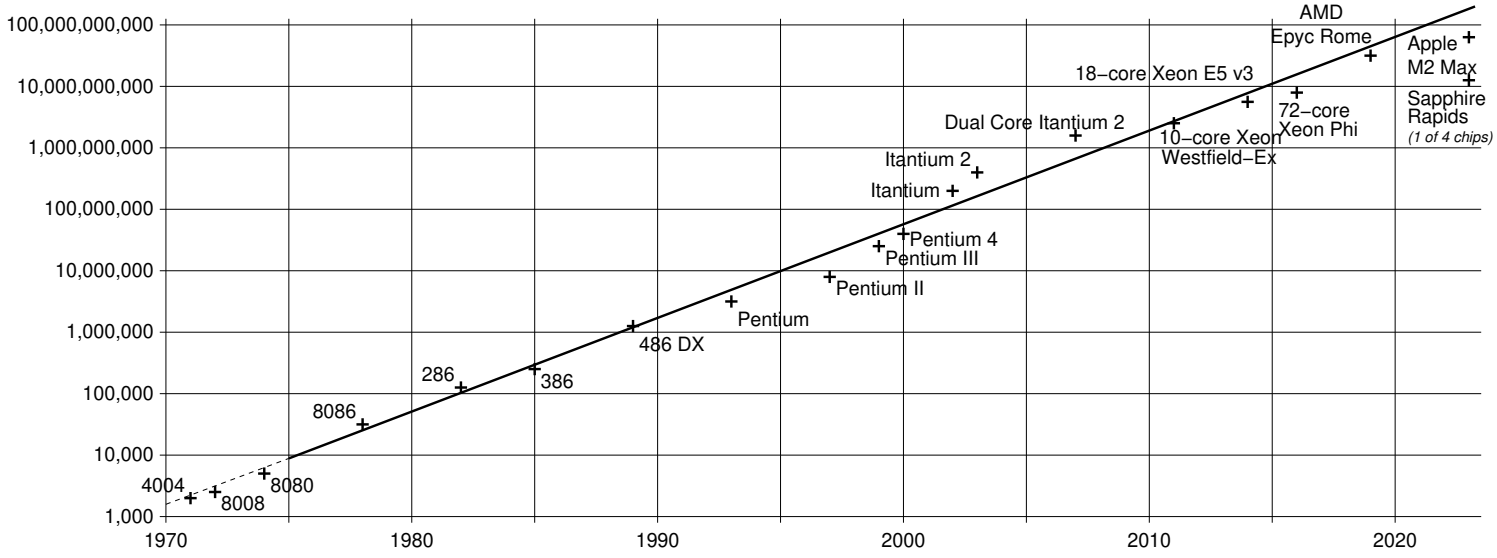


Source: Fairchild



Moore's Law (1965) Number of components has doubled every year and will continue to do so until 1975

Moore's Law (1975) Number of components will double every two years



Self–fulfilling Prophecy