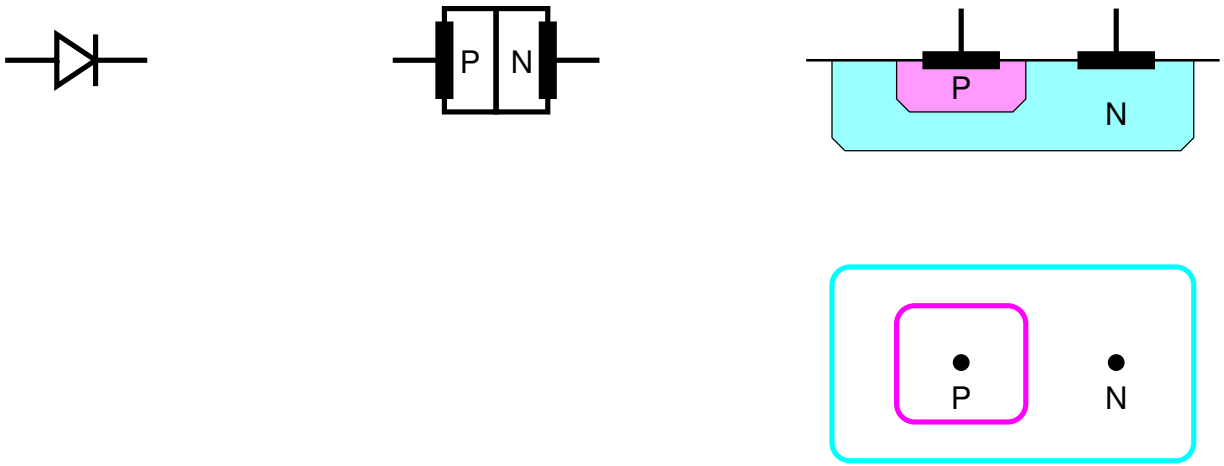
Components for IC Design

Diodes and Bipolar Transistors

Diode



- Ideal structure - 1D
- Real structure - 3D
- Depth controlled implants.

Diodes and Bipolar Transistors

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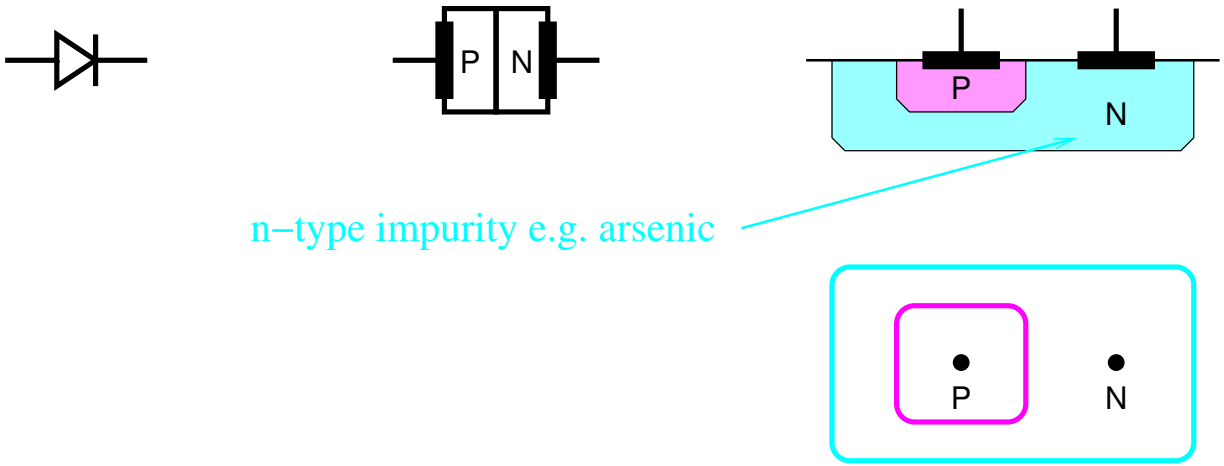

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Diodes and Bipolar Transistors

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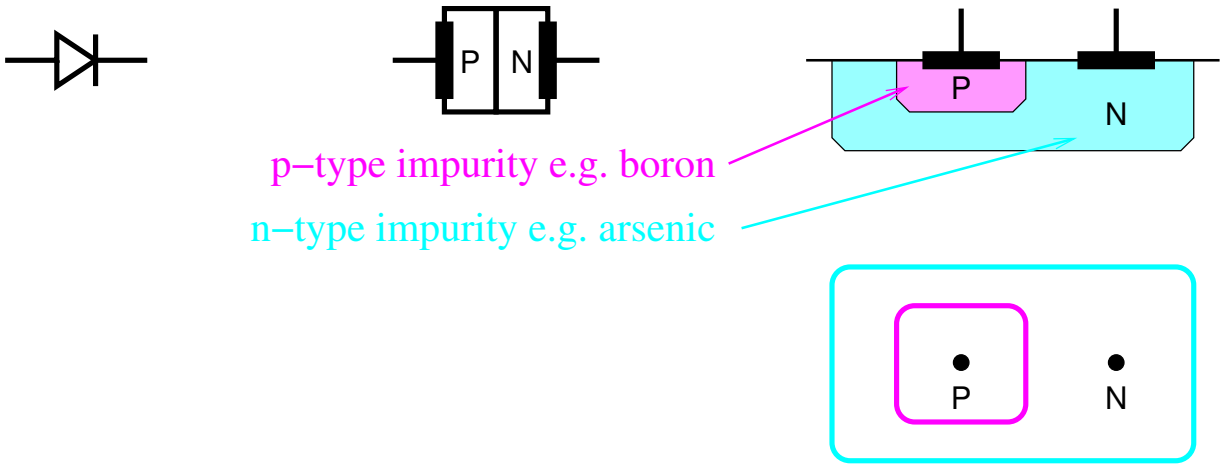

- Ideal structure - 1D
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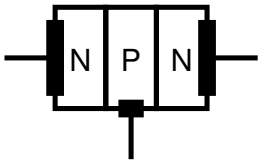
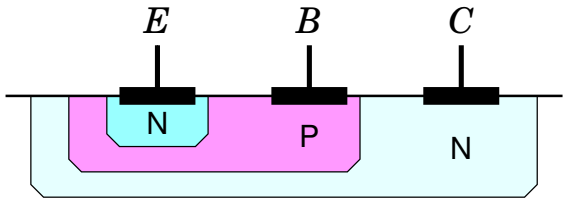
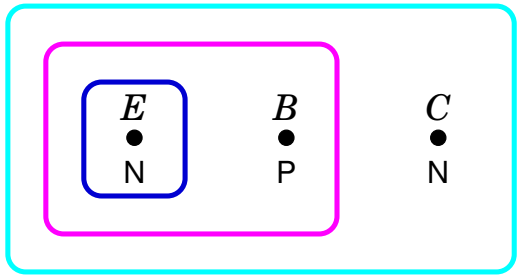
Diodes and Bipolar Transistors

NPN Transistor



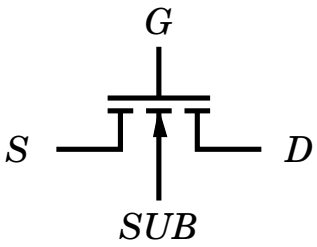


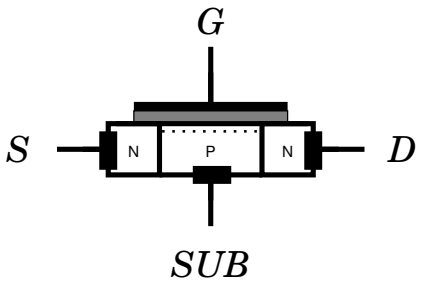


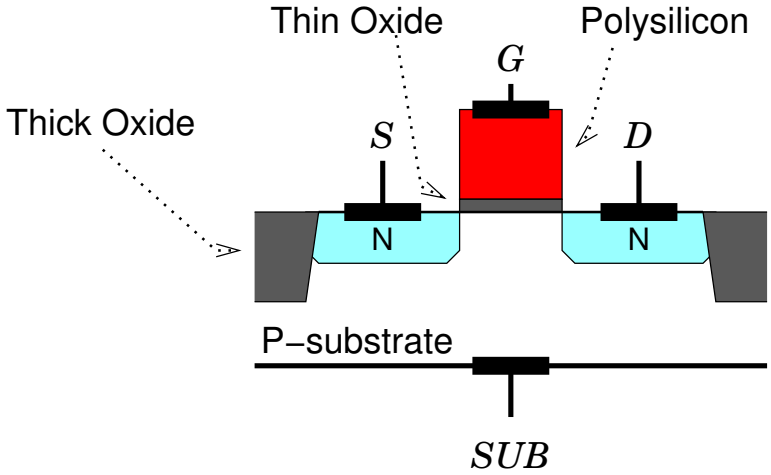
- Two n-type implants.

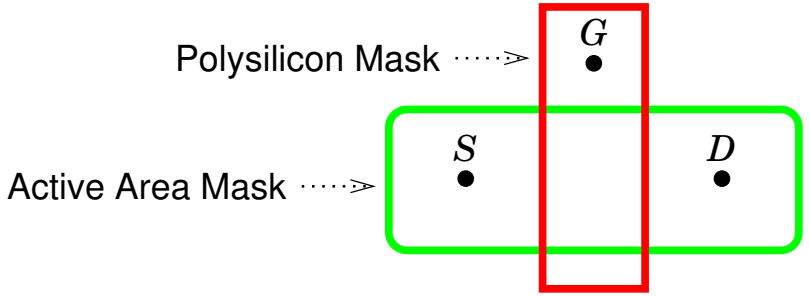
MOS Transistors

Simple NMOS Transistor









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- Active Area mask defines extent of *Thick Oxide*.
- Polysilicon mask also controls extent of *Thin Oxide* (alias *Gate Oxide*).
- N-type implant has no extra mask.
  – It is blocked by thick oxide and by polysilicon.
  – The implant is *Self Aligned*.
- Substrate connection is to bottom of wafer.
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- Gate connection not above transistor area.
  – Design Rule.

MOS Transistors

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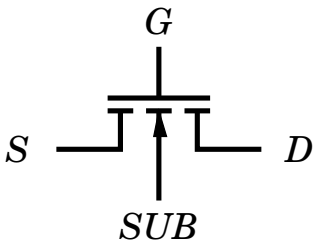

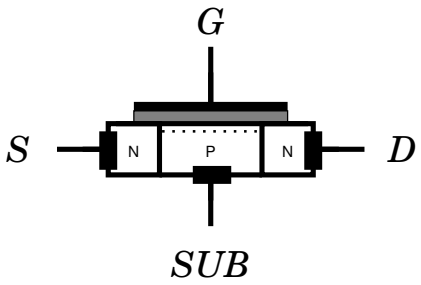

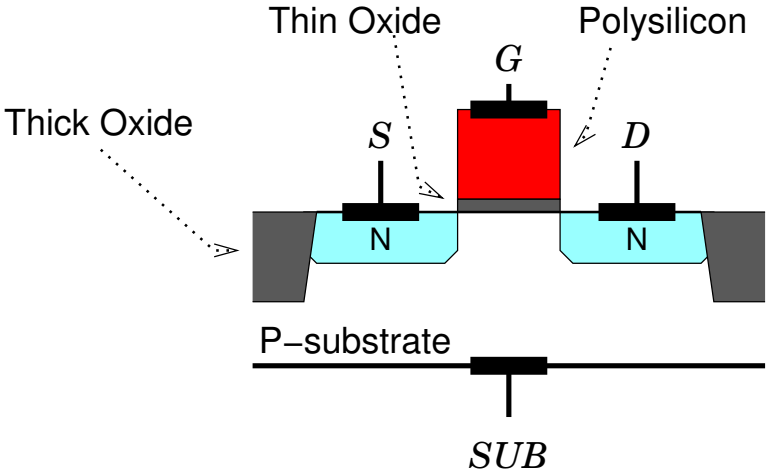

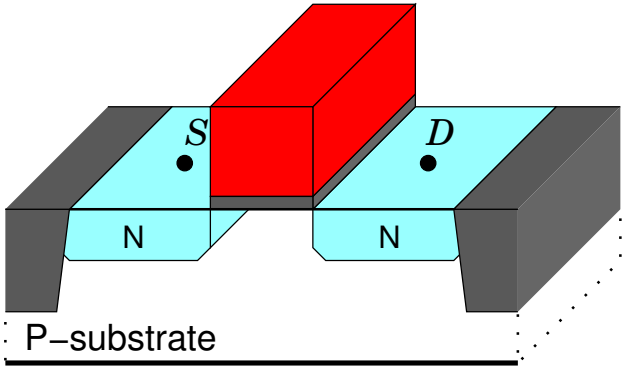

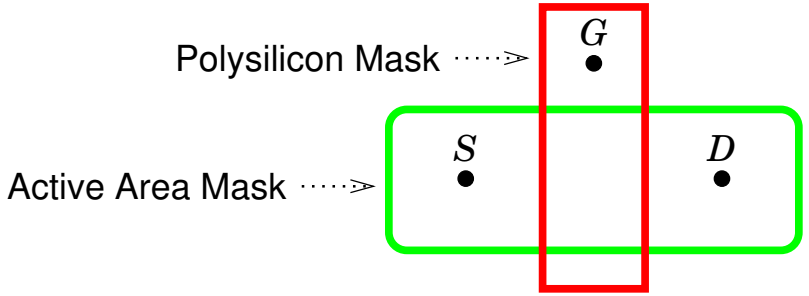

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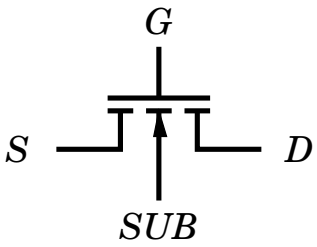

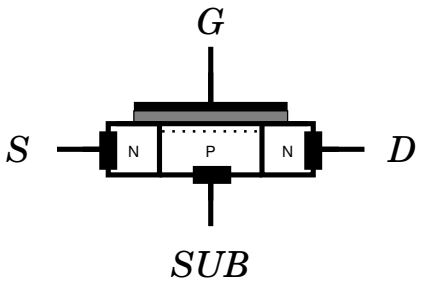

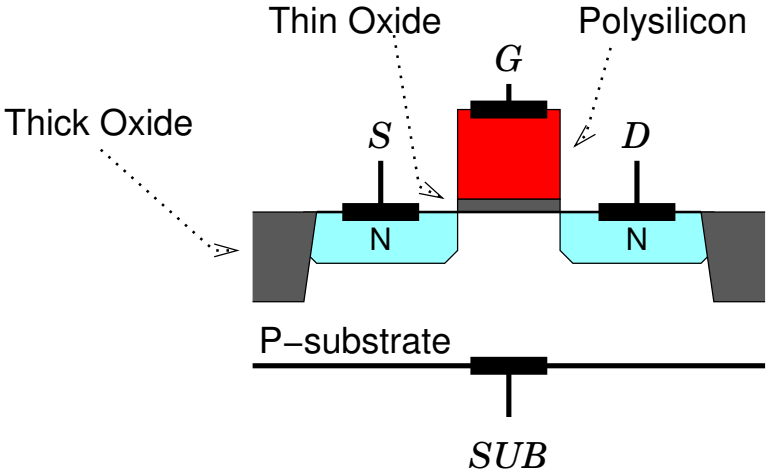

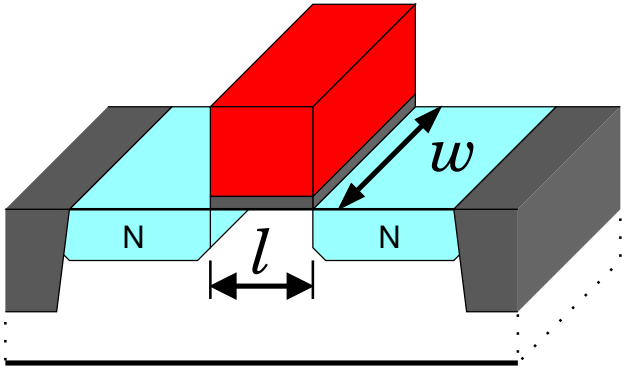

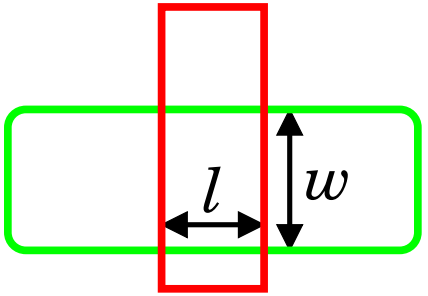

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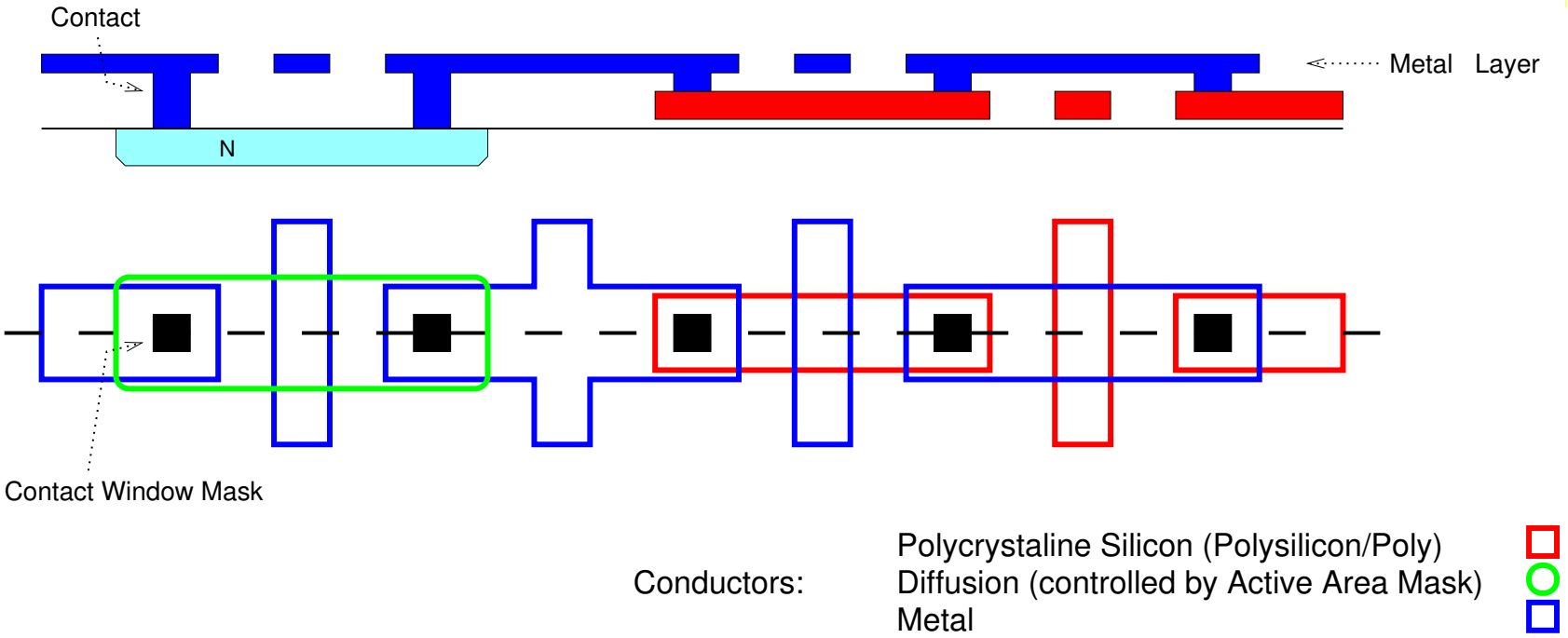
Interconnect



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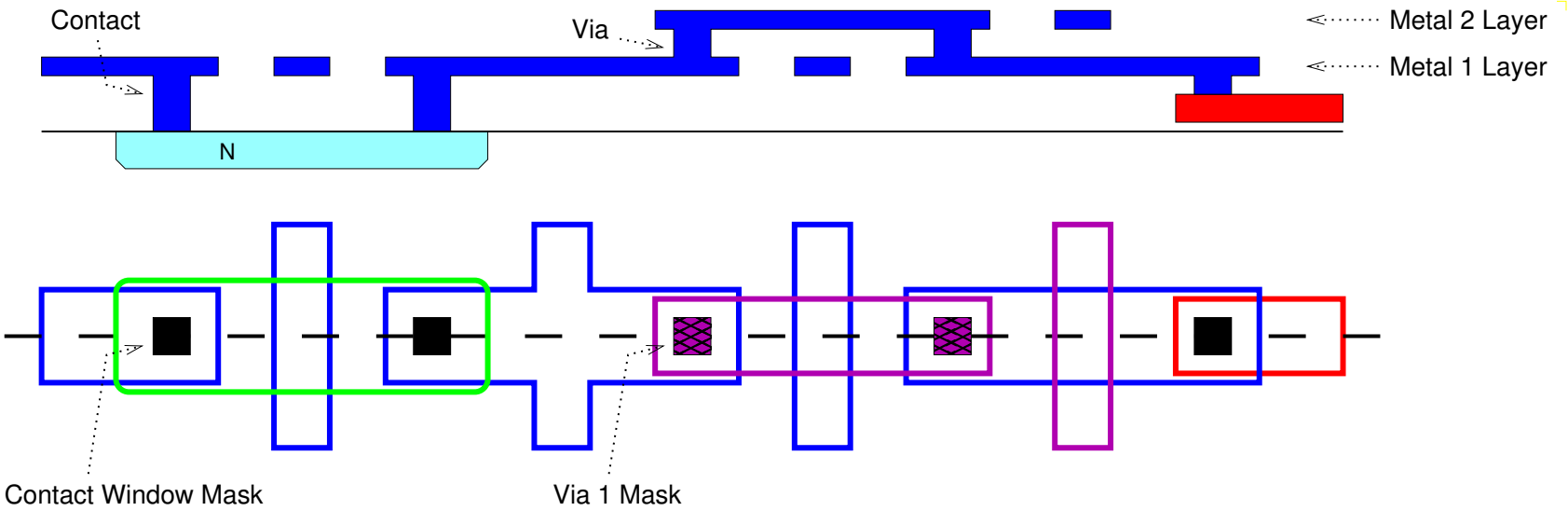

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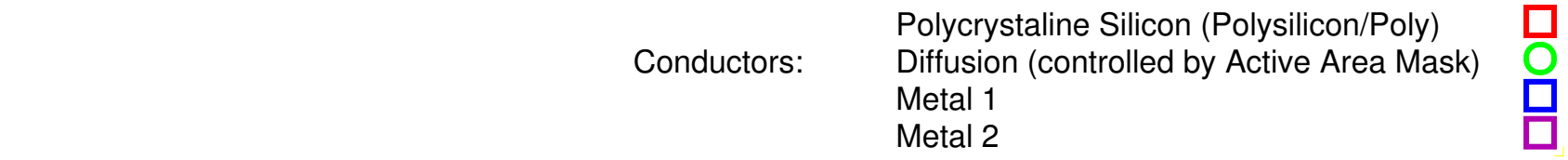

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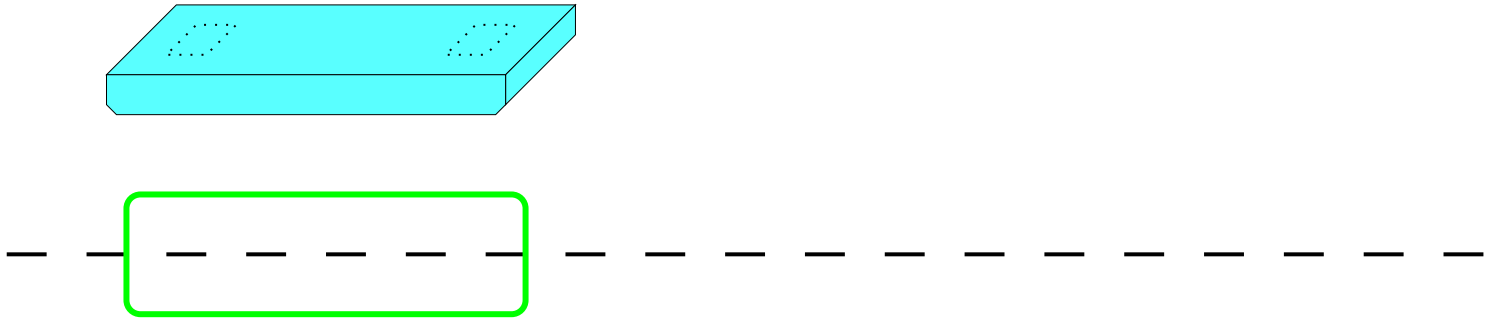

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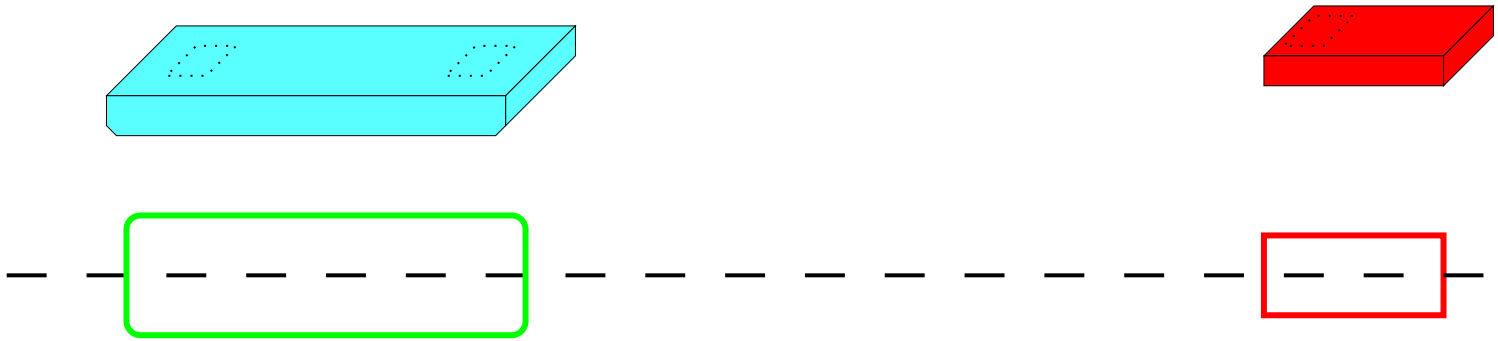

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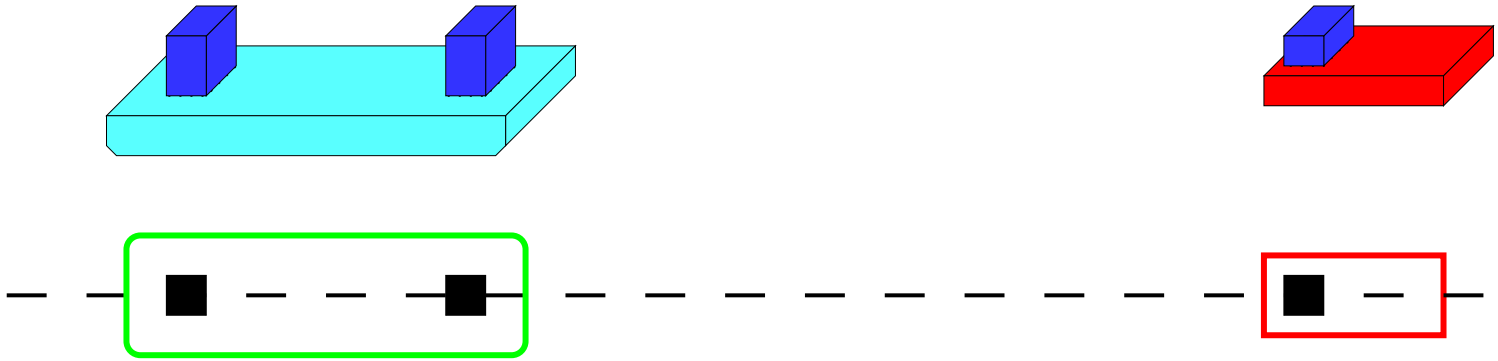

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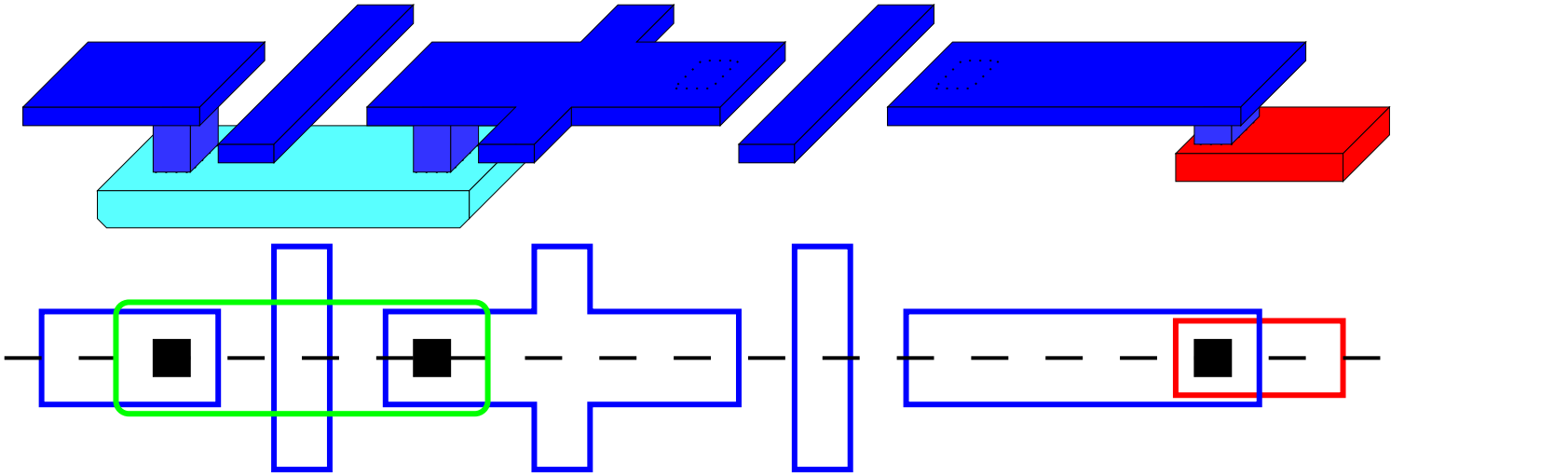

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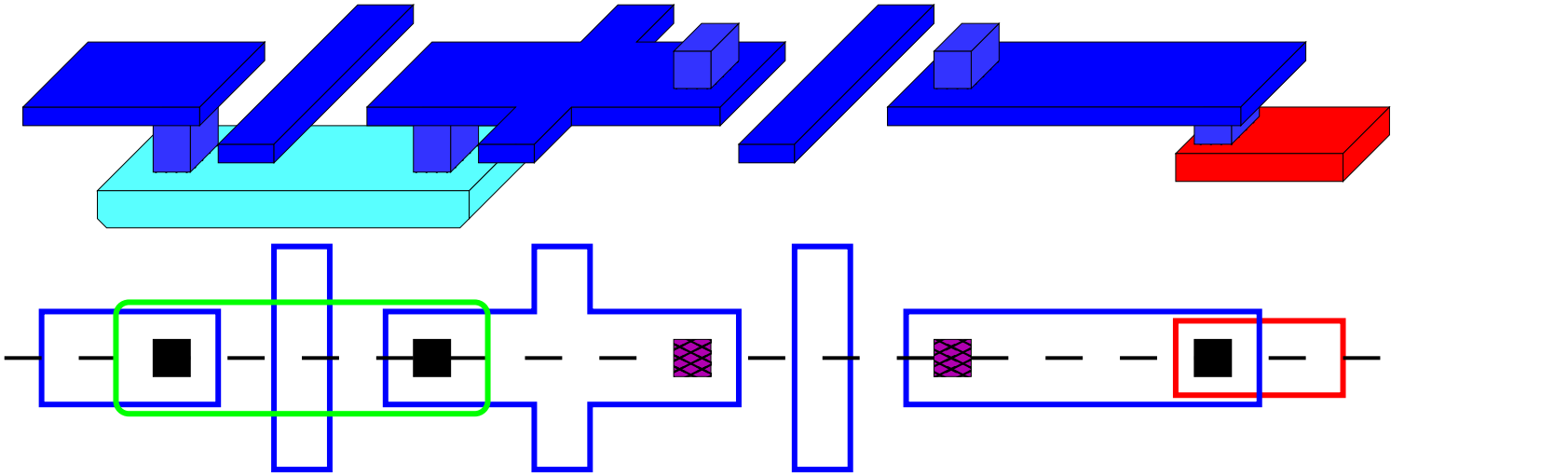

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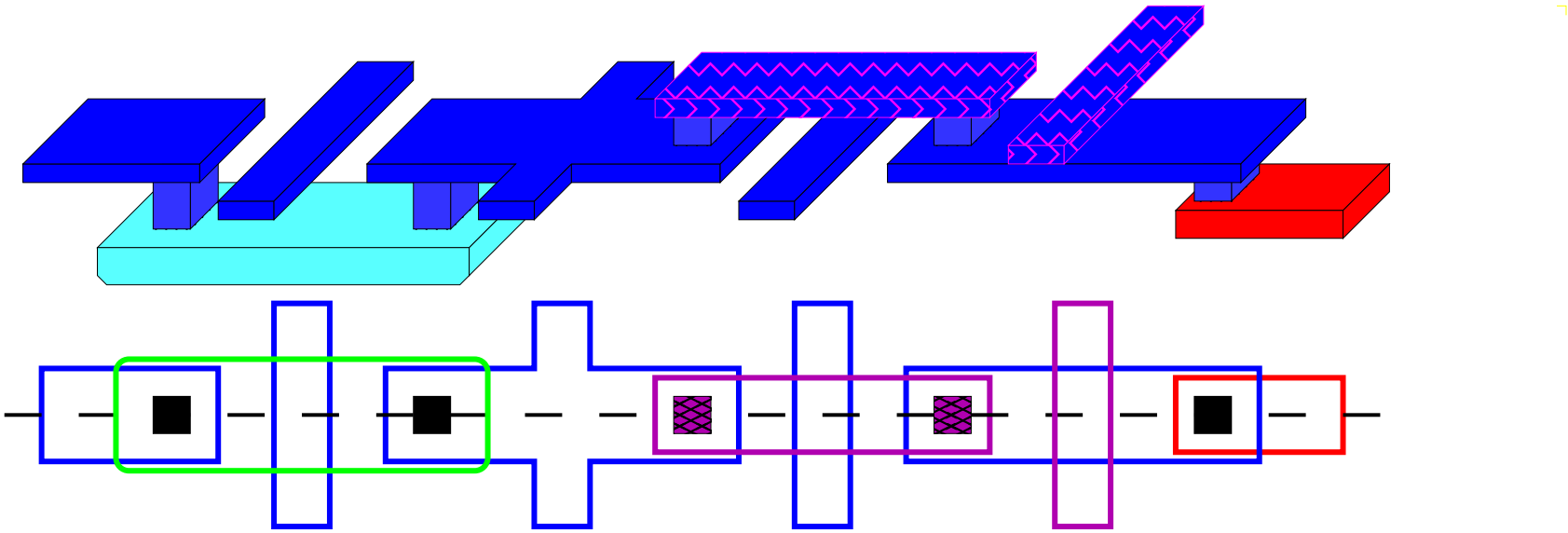

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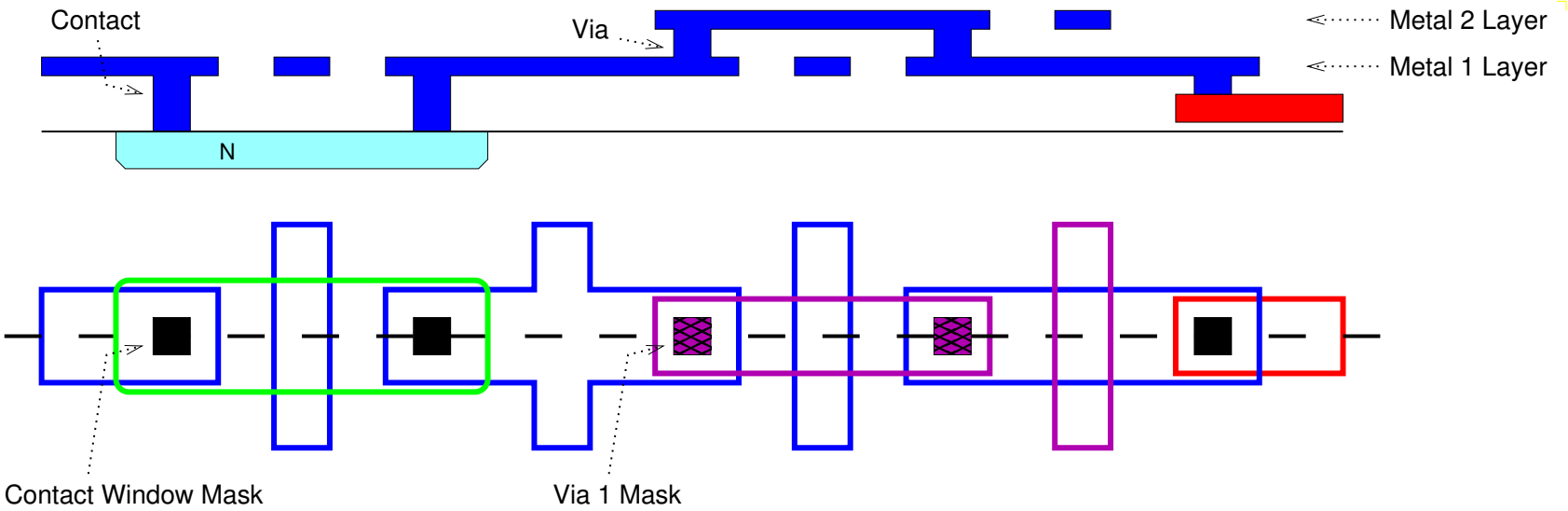

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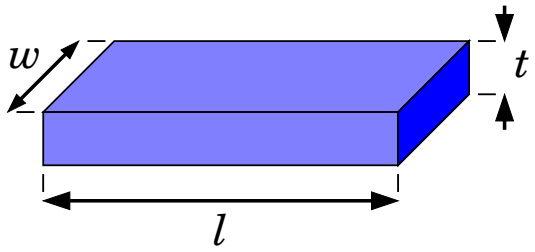
Resistance



$$R = \left(\frac{\rho}{t}\right)\left(\frac{l}{w}\right)$$

where ρ is the resistivity constant

$3.2 \times 10^{-8}\Omega m$ for aluminium

$1.7 \times 10^{-8}\Omega m$ for copper

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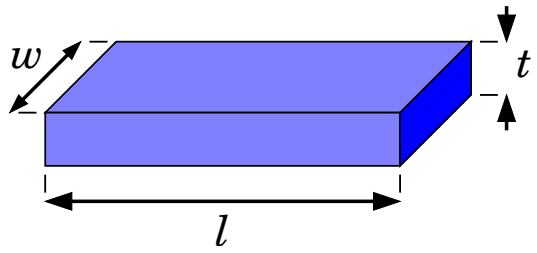

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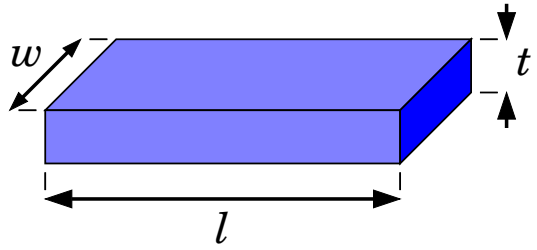

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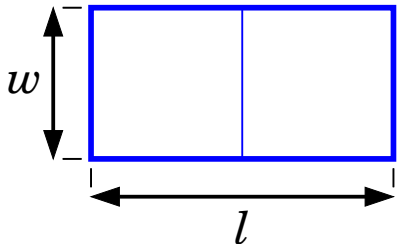


$$R = R_s\left(\frac{l}{w}\right)$$

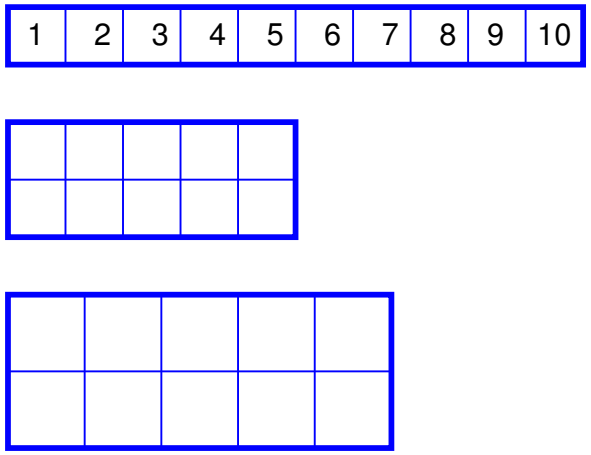
where R_s is sheet resistance
$0.1\Omega/\square$ for $170nm$ thick copper

R_s = resistance of a square (i.e. $w = l$) so the units for R_s are $\Omega/\square$ (ohms per square).

Components for IC Design

Resistors

Examples for Metal
assuming Rs = 0.1 ohms per square

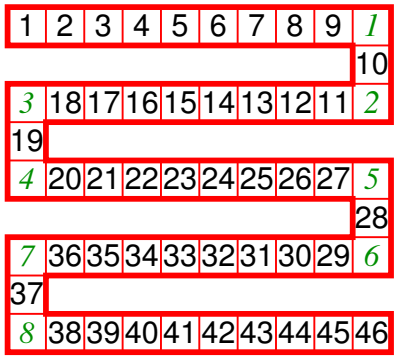


R = 1 Ω

R = Ω

R = Ω

Example for Polysilicon
assuming Rs = 200 ohms per square



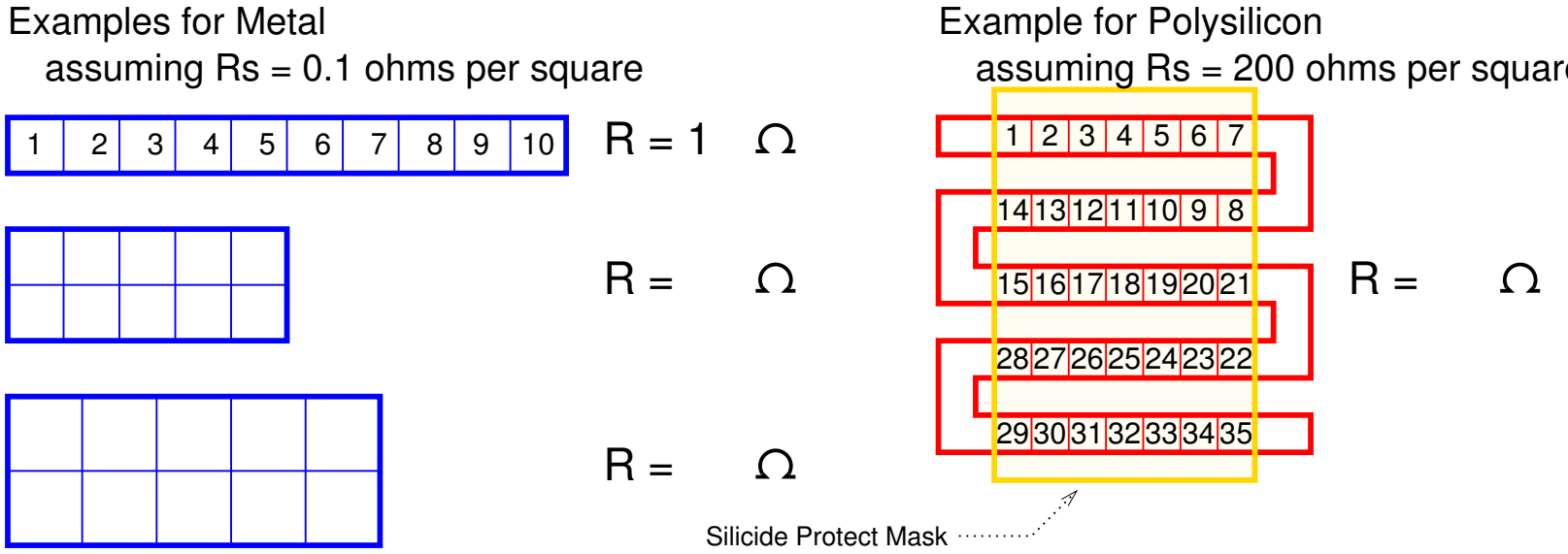
R = Ω

- for larger resistances we need minimum width poly (often combined with a *serpantine* shape) to save on area
- corner squares count as half[2] squares
- for predicatability and matching we may need wider tracks without corners

[2] effective resistance $\approx 0.56 R_s$

Components for IC Design

Resistors



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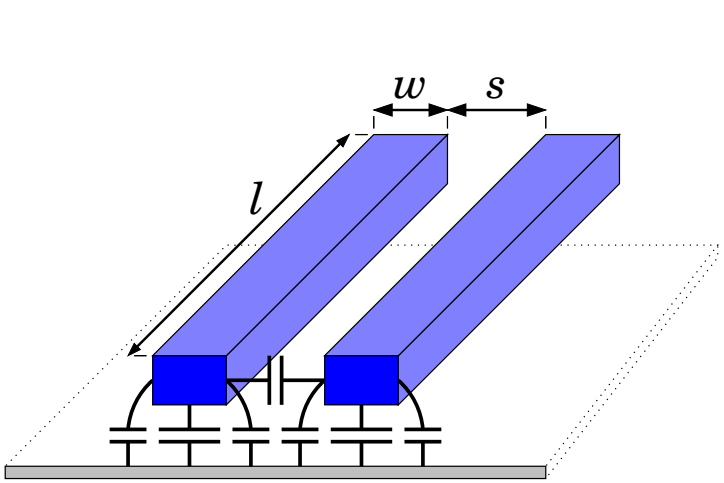
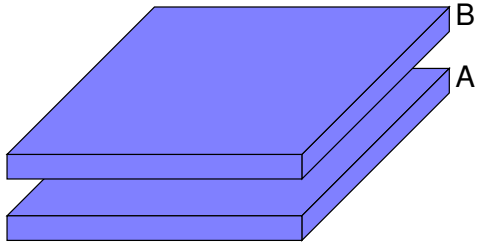
Components for IC Design

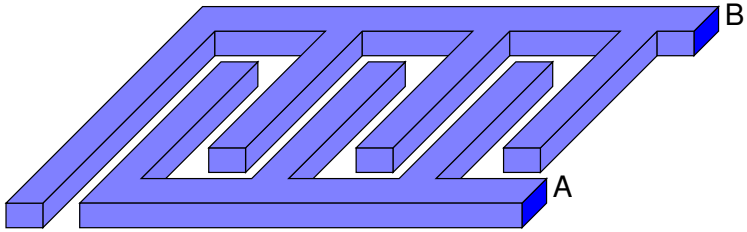
Capacitors



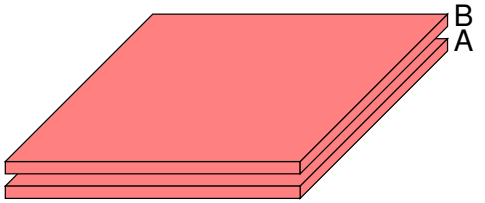
parallel tracks over underlying conductor
(e.g. bulk silicon)



metal–insulator–metal capacitor



fringe capacitor



poly–insulator–poly capacitor
(specialist analog process with 2 poly layers)

- Capacitance to underlying conductor $C = C_a\ w\ l + 2\ C_f\ l$
- Coupling capacitance to adjacent track $C = C_c\ l/s$
  where C_a, C_f, C_c are constants for a given layer and process

*in digital designs our only aim is to minimise **parasitic** capacitance*

Components for IC Design

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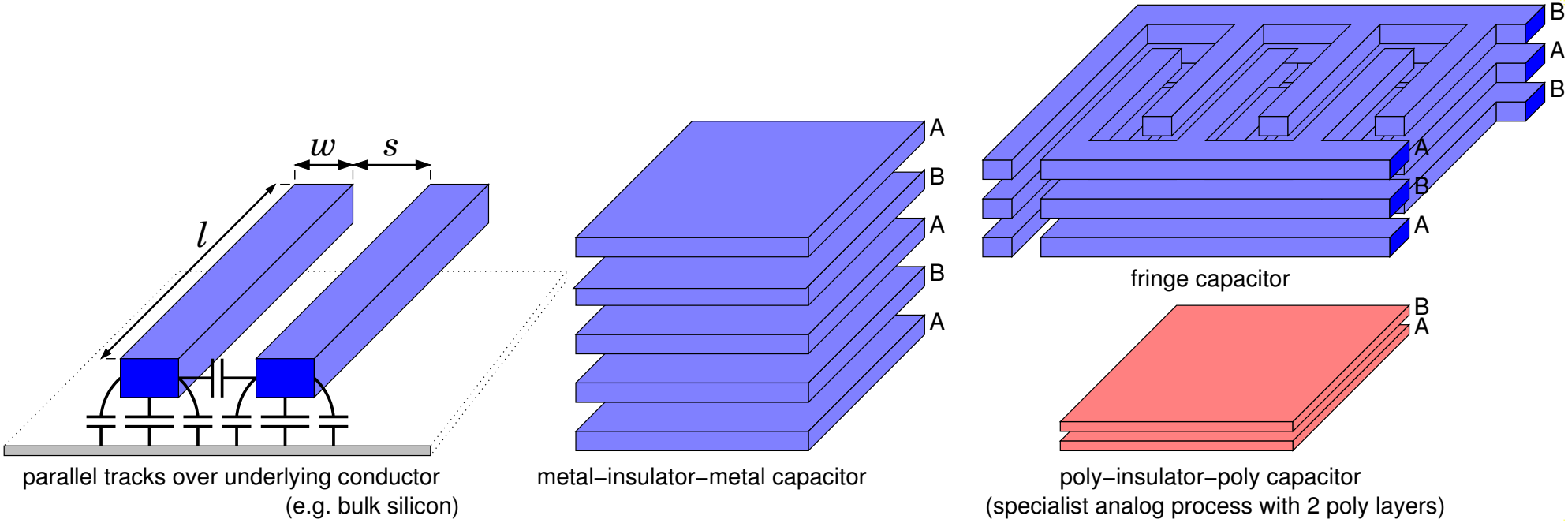

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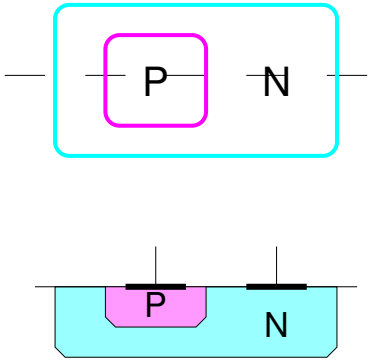
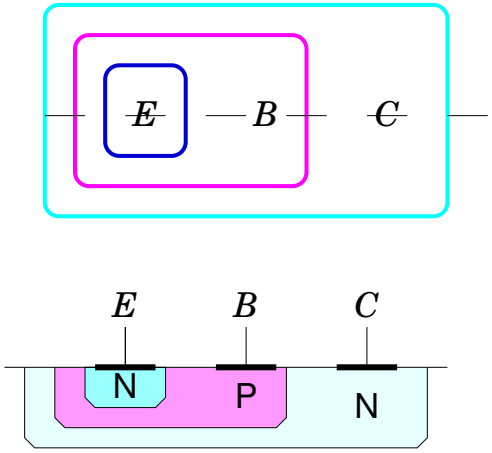
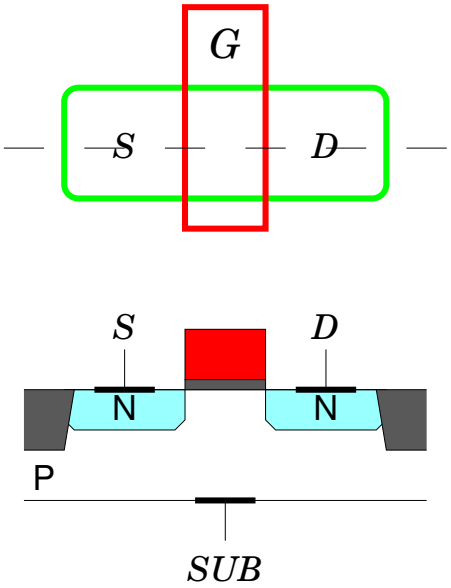


NPN Transistor

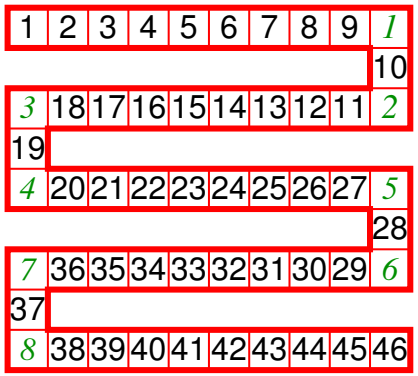


NMOS Enhancement transistor

NMOS Process



Resistor



Capacitors