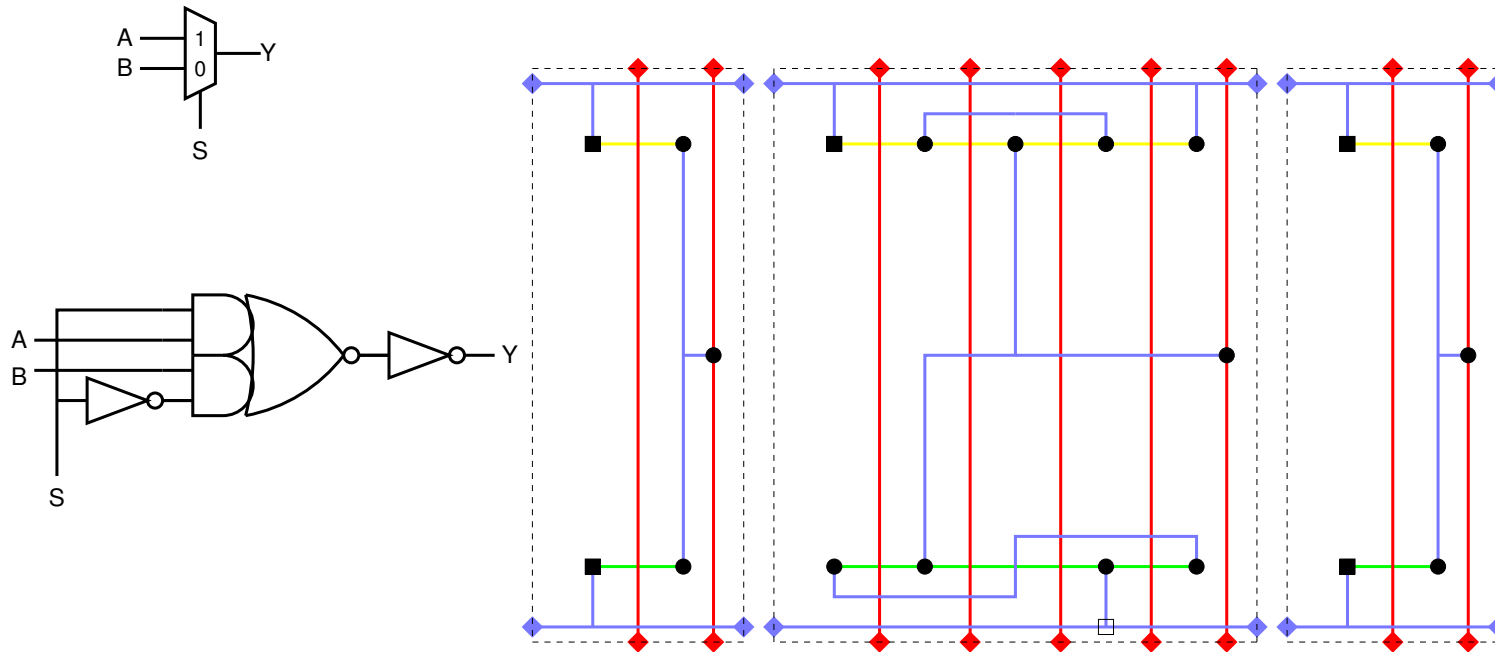


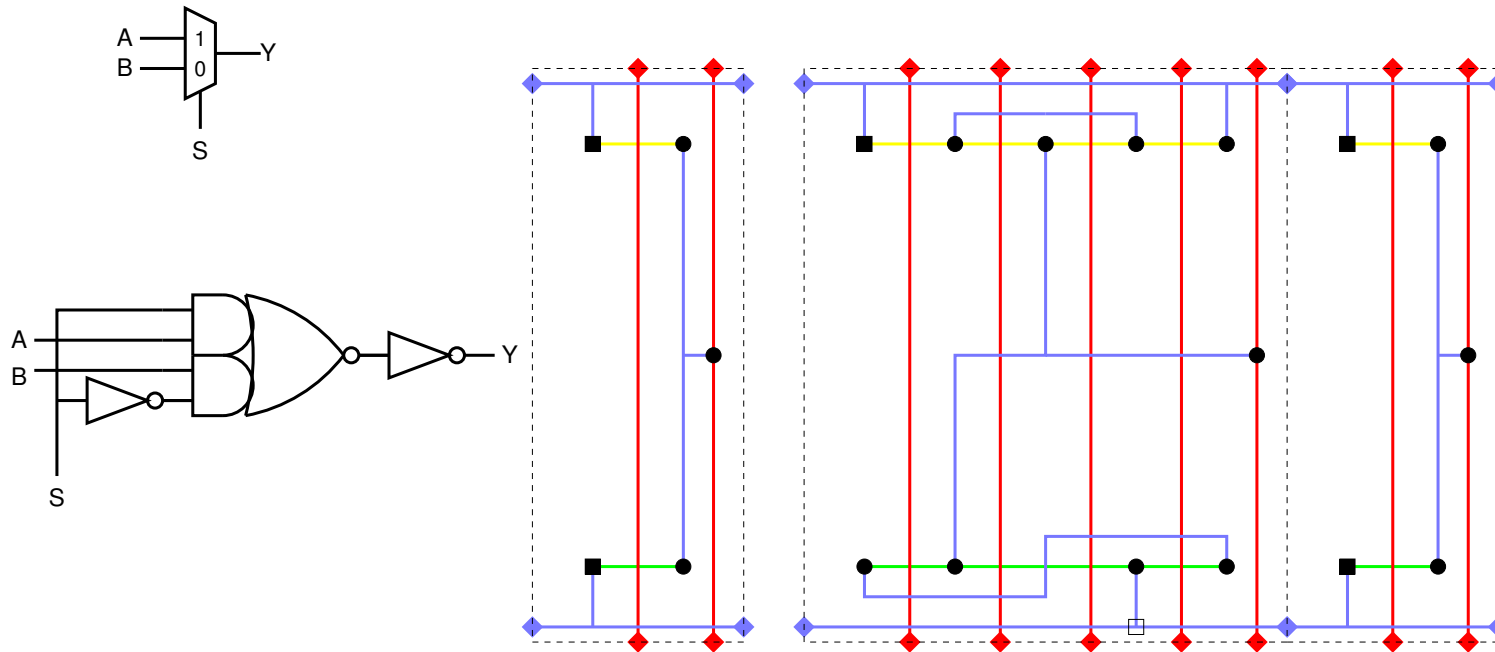
Digital CMOS Design

Multiple gates



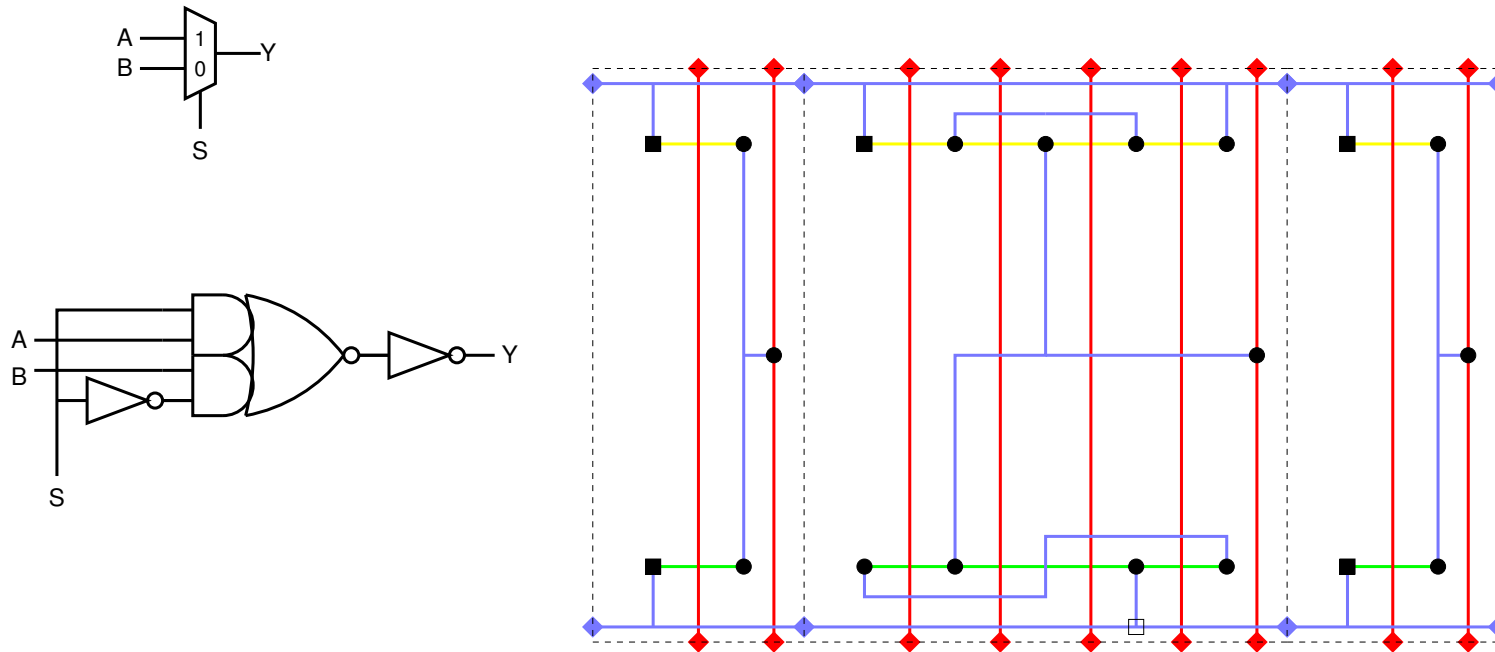
Digital CMOS Design

Multiple gates



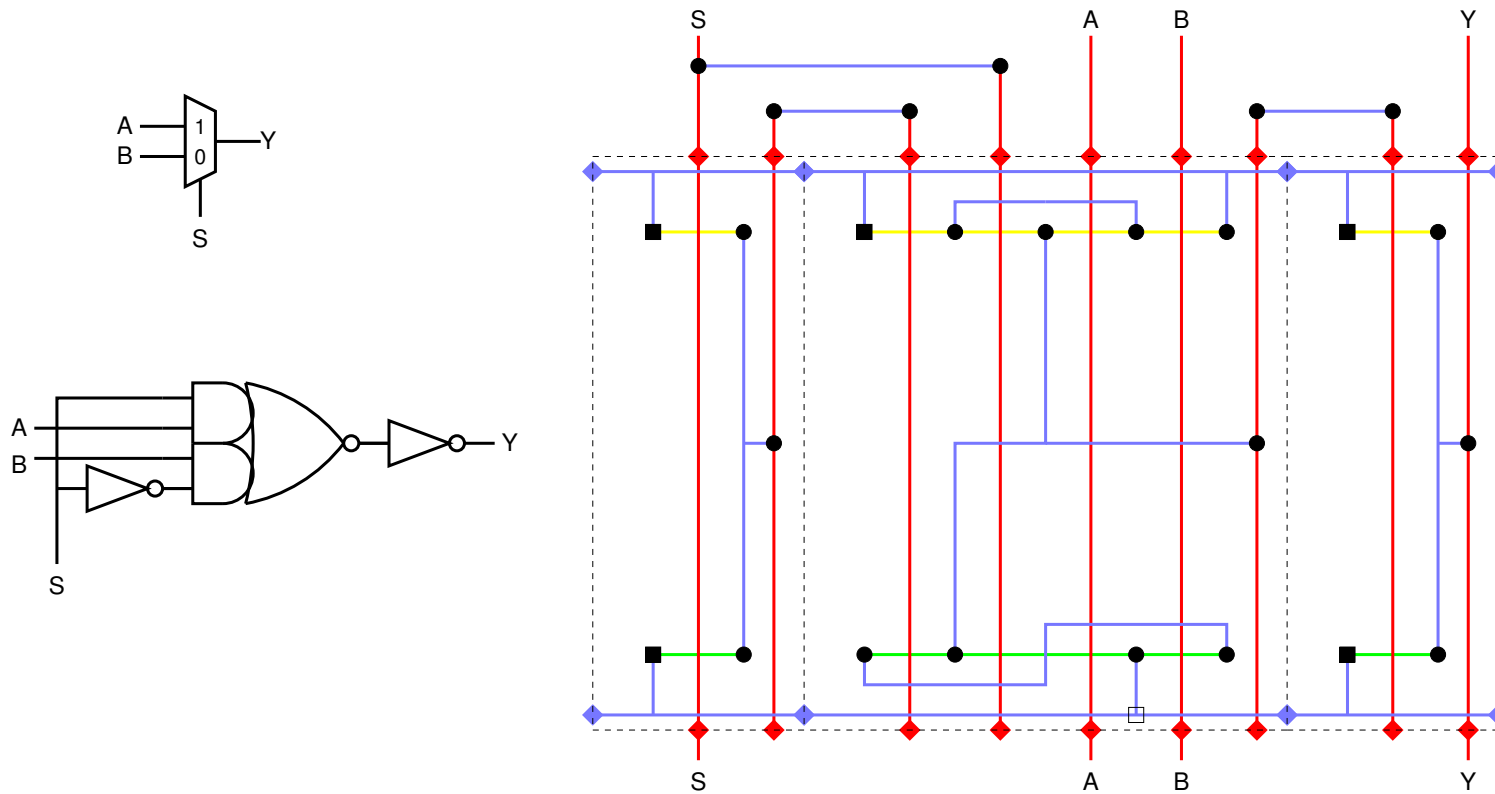
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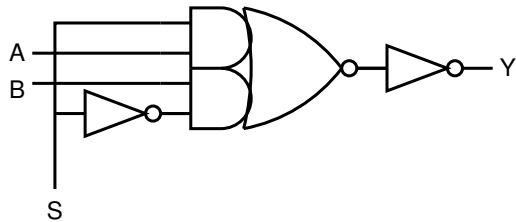
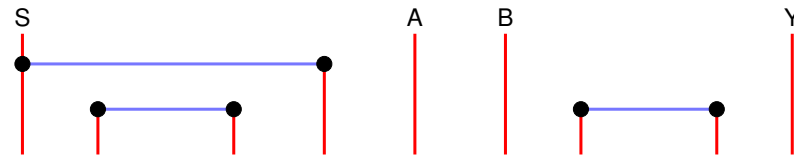
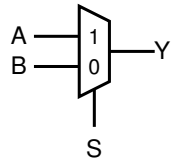
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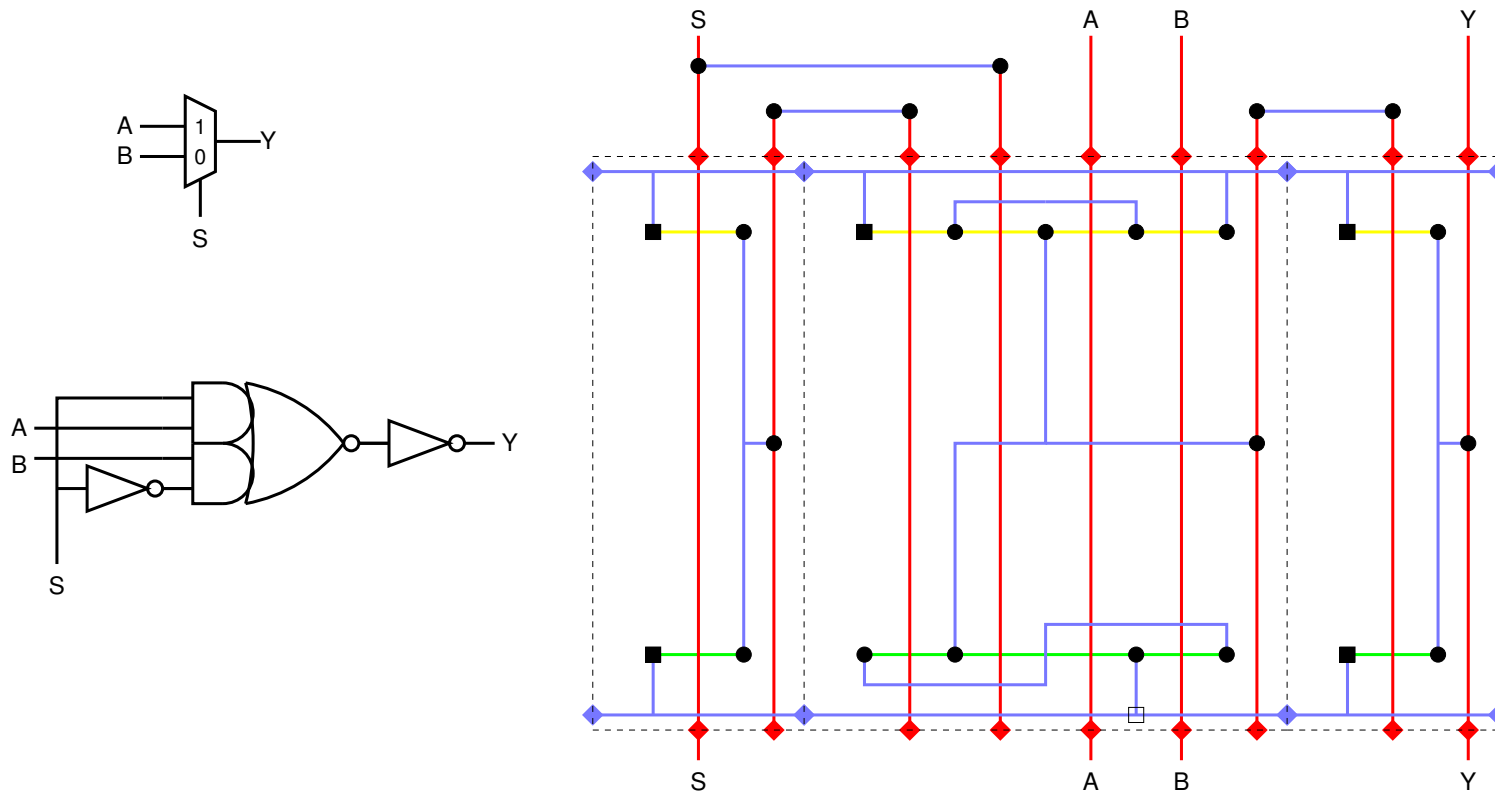
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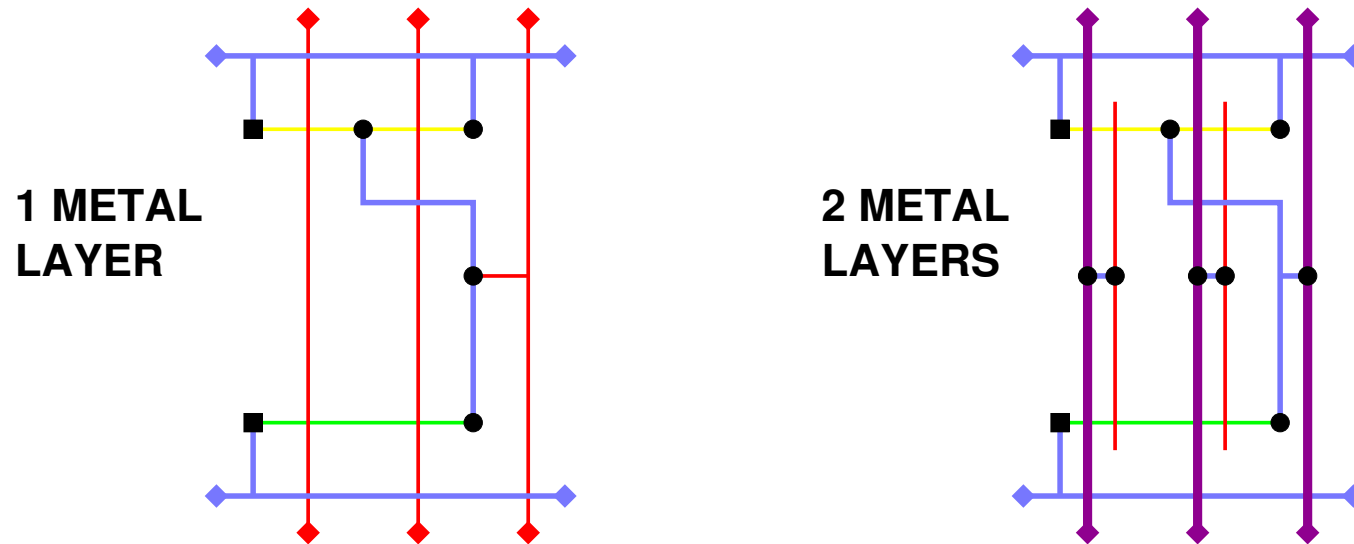
Digital CMOS Design

Multiple gates

- Gates should all be of same height.
 - Power and ground rails will then line up when butted.
- All gate inputs and outputs are available at top and bottom.
 - All routing is external to cells.
 - Preserves the benefits of hierarchy.
- Interconnect is via *two conductor routing*.
 - In this case Polysilicon vertically and Metal horizontally.

Digital CMOS Design

Two-layer Metal



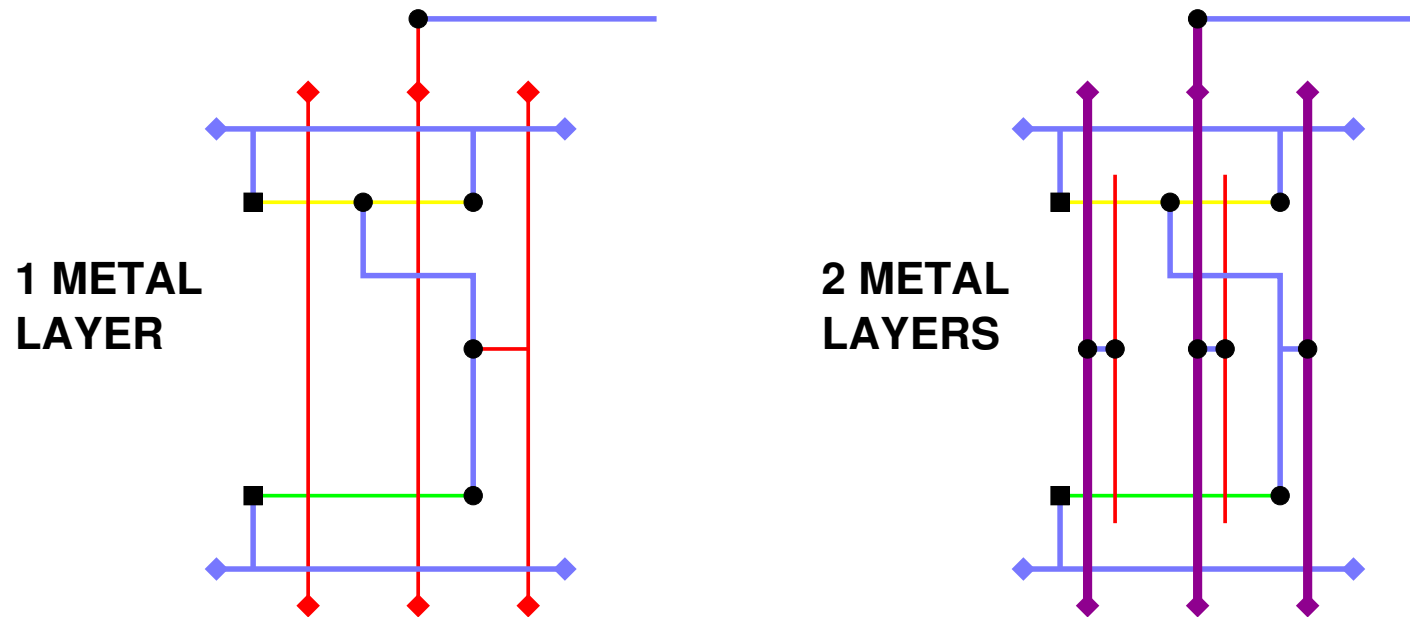
Most modern VLSI processes support two or more metal layers.

The norm is to use only metal for inter-cell routing.

usually Metal1 for horizontal inter-cell routing (and for power rails)
Metal2 for vertical inter-cell routing (and for cell inputs and outputs).

Digital CMOS Design

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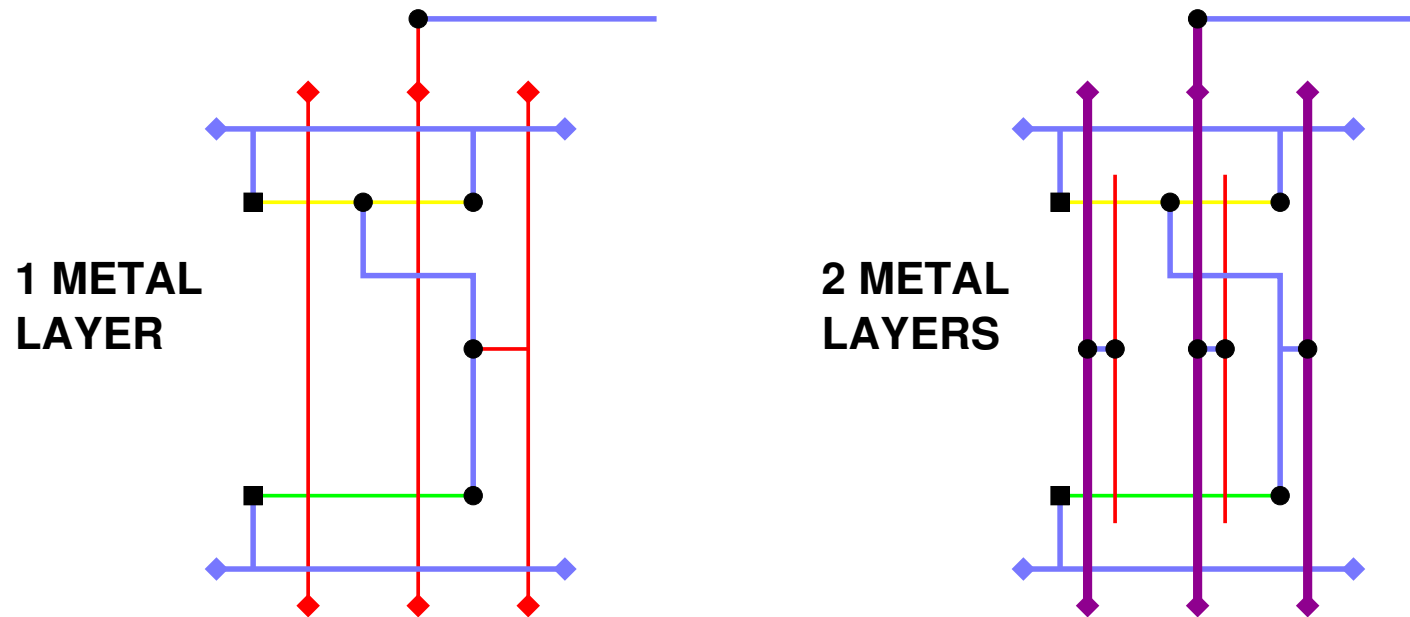
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Standard Cell Design

Many ICs are designed using the standard cell method.

- Cell Library Creation

A cell library, containing commonly used logic gates¹ is created for a process. This is often carried out by or on behalf of the foundry.

- ASIC² Design

The ASIC designer must design a circuit using the logic gates available in the library.

The ASIC designer usually has no access to the full layout of the standard cells and doesn't create any new cells for the library.

Layout work performed by the ASIC designer is divided into two stages:

- Placement
- Routing

¹note that a standard cell may include transistors from more than one basic function (e.g. NAND + inverter to give AND) but will normally be designed *flat* i.e. without layout hierarchy.

²Application Specific Integrated Circuit

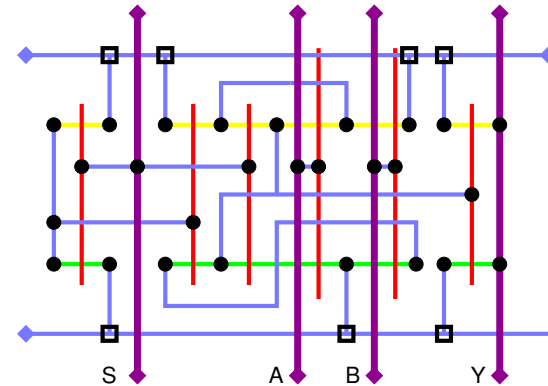
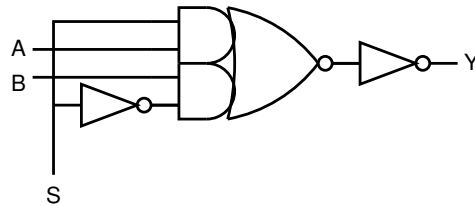
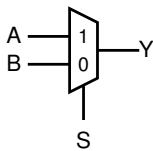
Standard Cell Design

Choosing a set of cells for a cell library

- There is no set size for a cell library.
- Theoretically just one cell () or one type of cell (, , , ...) is sufficient for a cell library.
- The use of more complex cells allows for designs optimised for area and/or performance:

Multiplexer standard cell

(single cell – no hierarchy)



- Which basic gates; which compound gates; which sequential gates?
- Do we provide different versions of the same gate (e.g. small area version, high drive version)? If so, how many different versions?

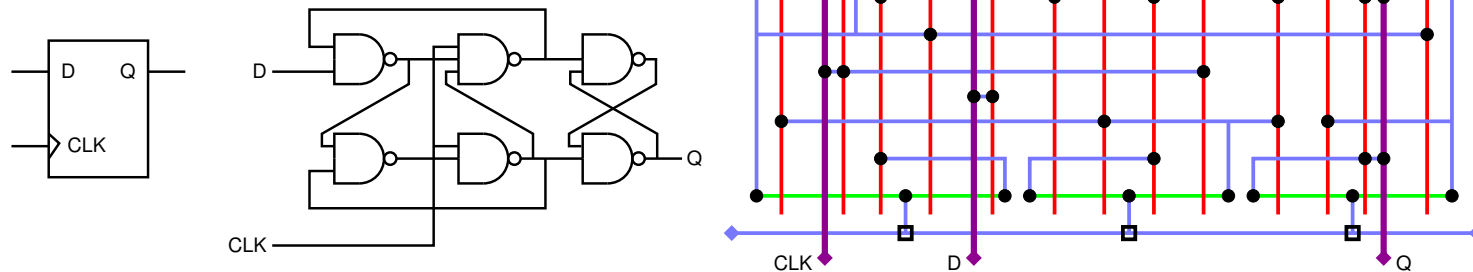
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D-Type standard cell

(single cell with Euler path optimisation)

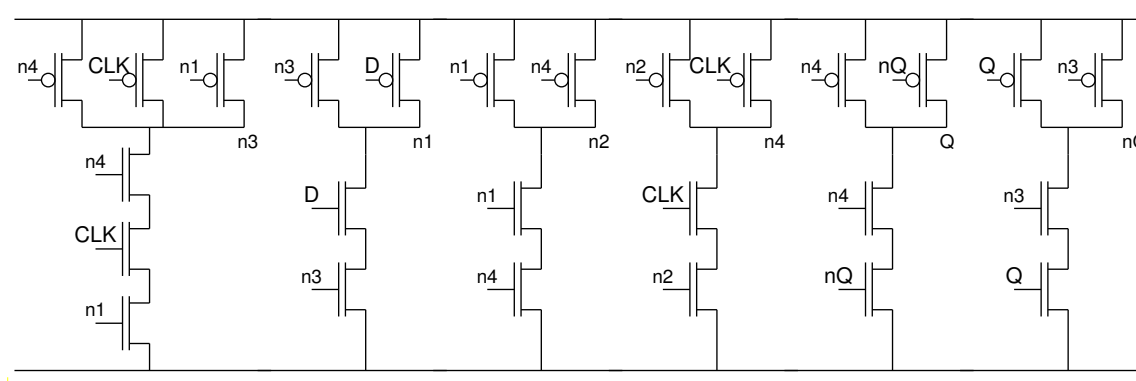


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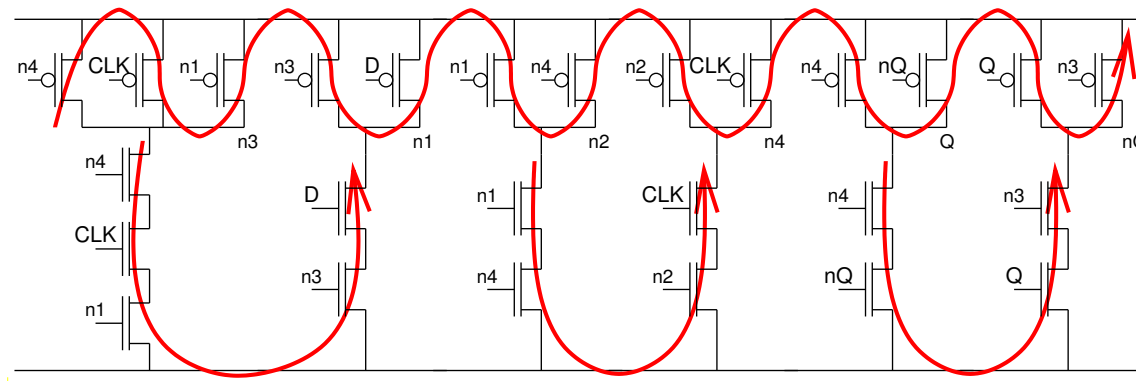


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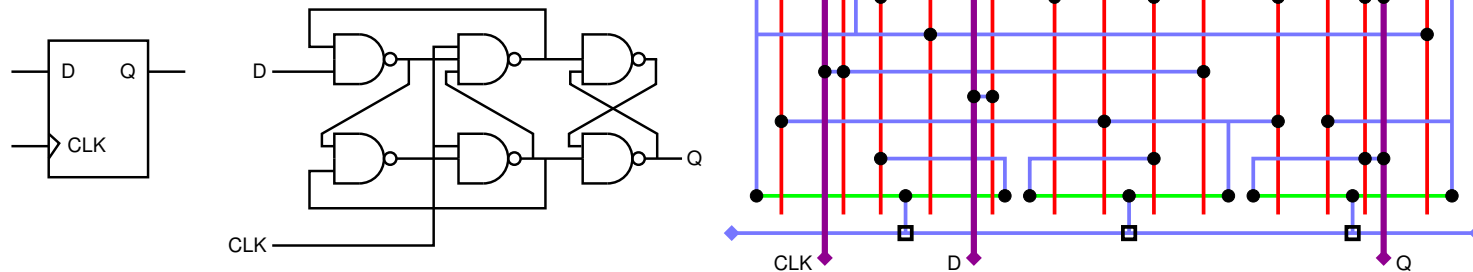
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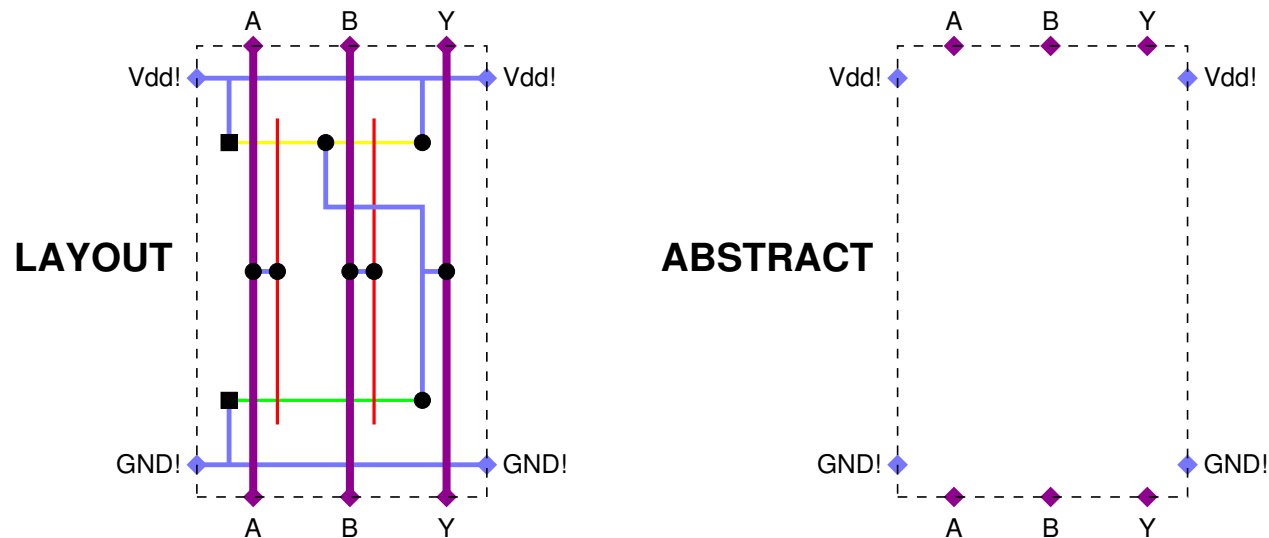
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Standard Cell Design

Layout and Abstract Views of a Standard Cell

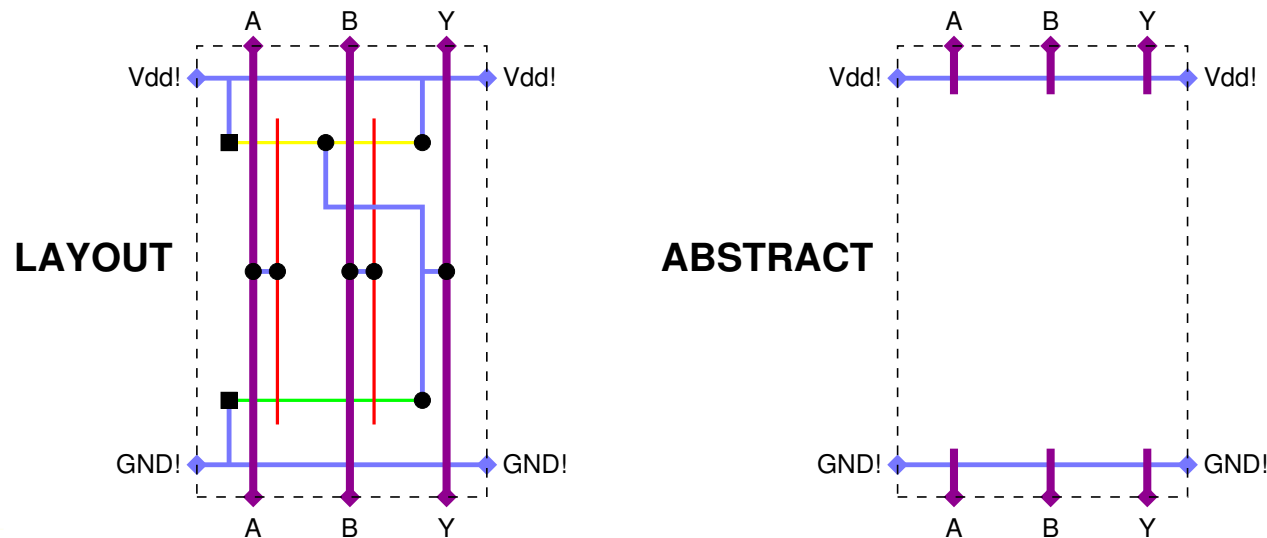


The partial cell layout usually given to the ASIC designer is known as a black box or *abstract* view. The abstract:

- must include cell ports and a cell boundary
- may include some or all of the metal mask information

Standard Cell Design

Layout and Abstract Views of a Standard Cell

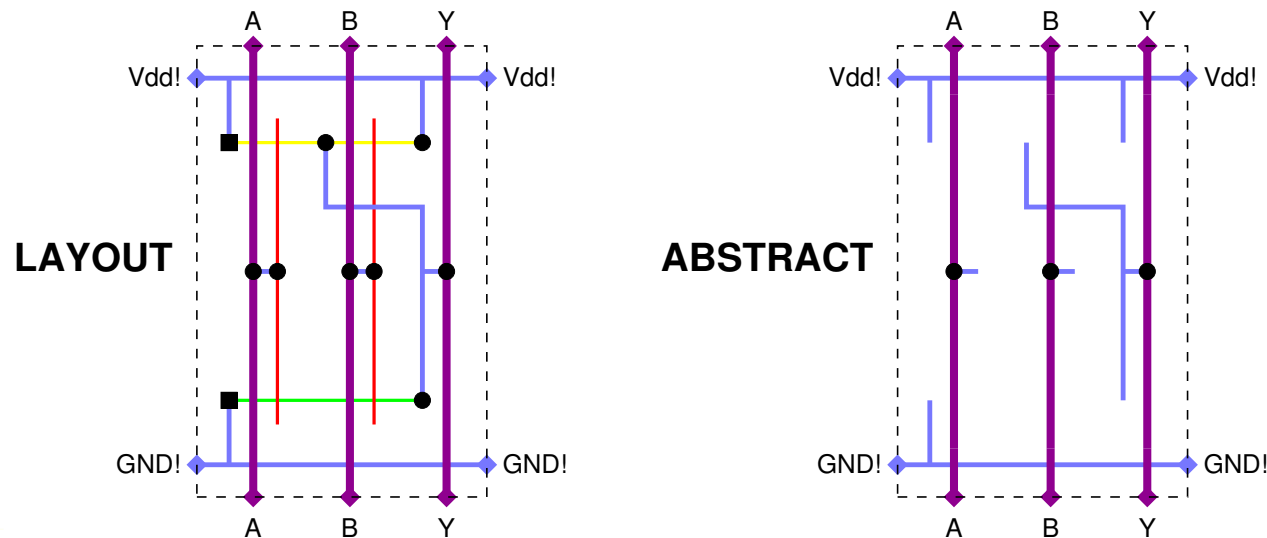


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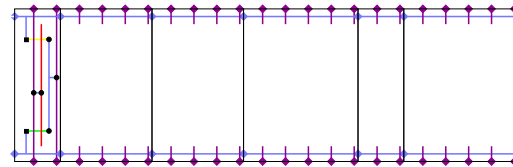


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Placement & Routing

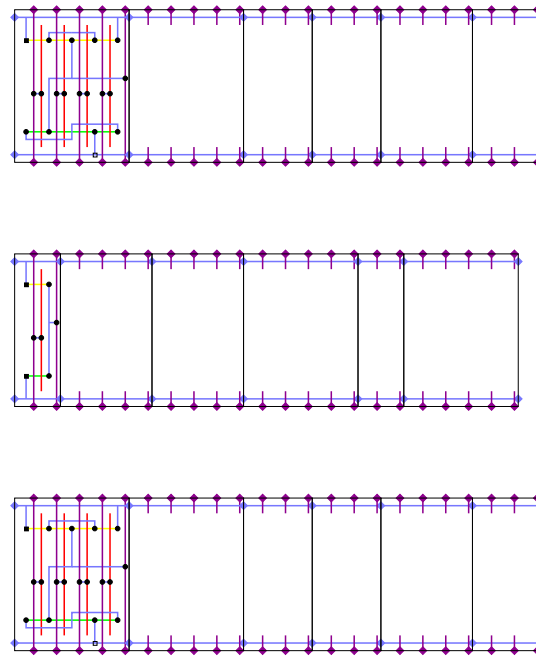
Placement



Cells are placed in one or several equal length lines with inter-digitated power and ground rails.

Placement & Routing

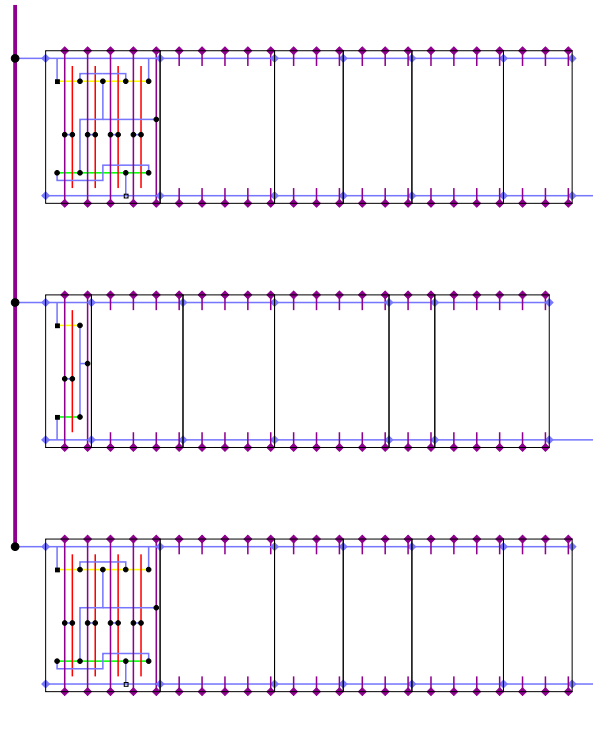
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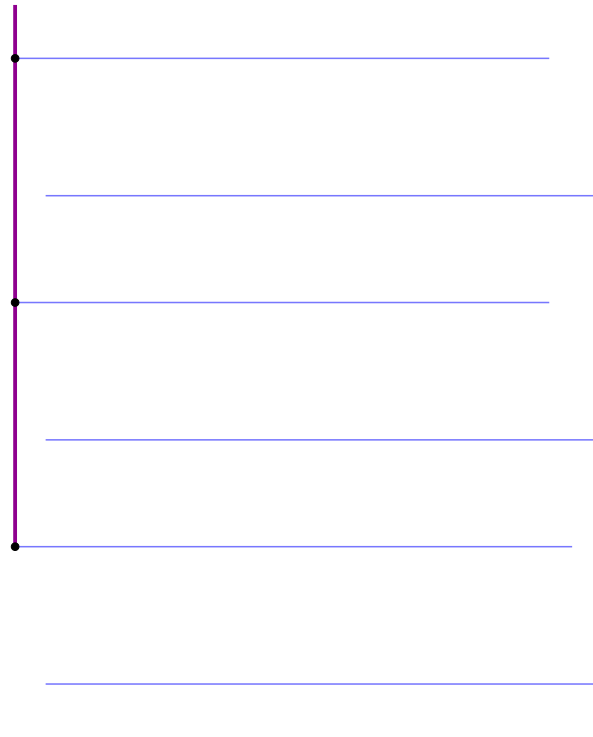
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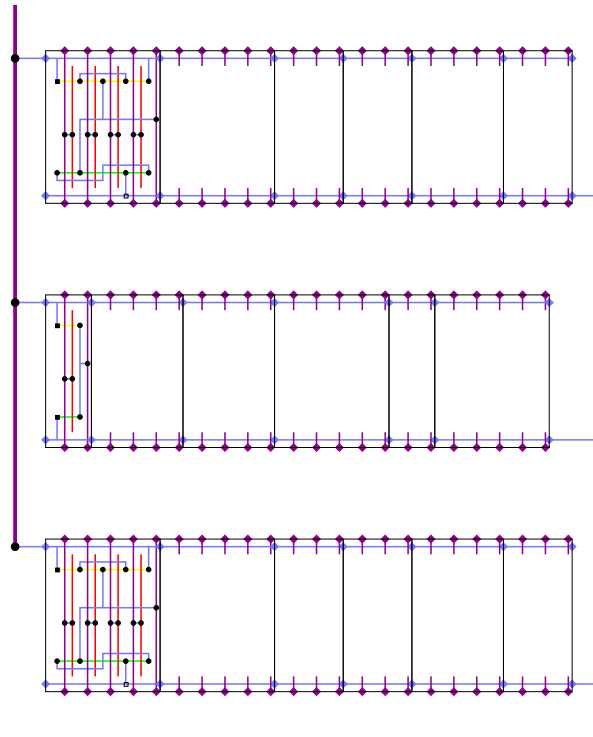
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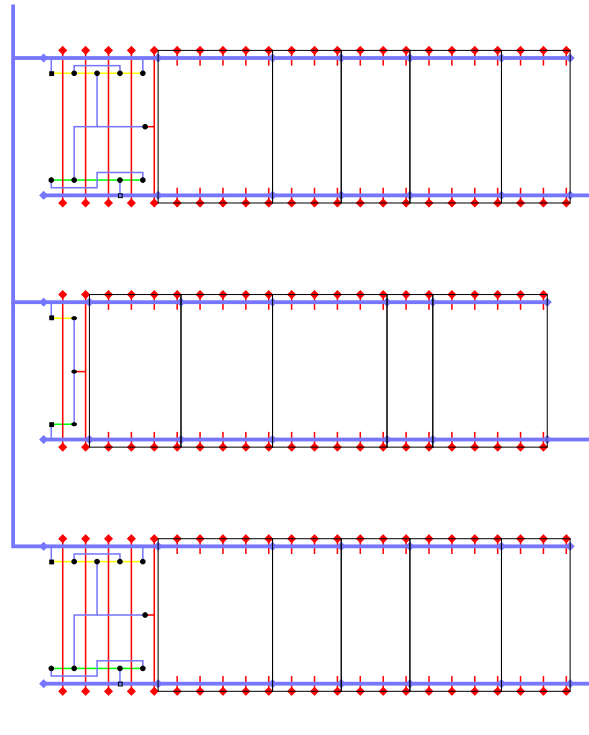
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Placement & Routing

Inter-Digitated Power and Ground

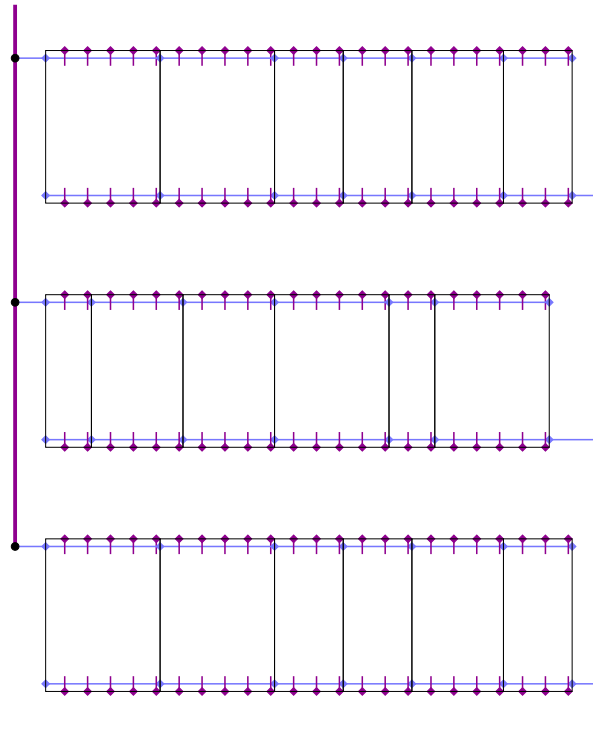


Inter-digitated power and ground rails can be routed using only one metal layer.³

³note – poly may not be used in power routing - see latch-up rules

Placement & Routing

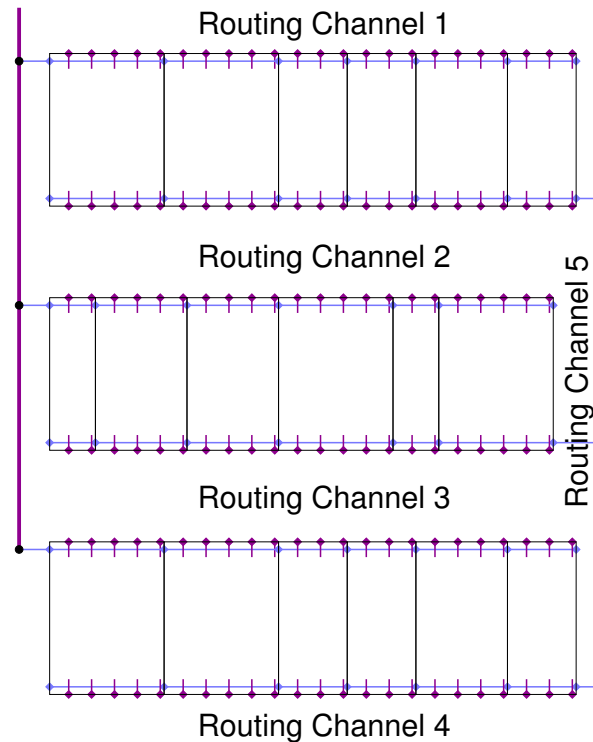
Routing



In the routing channels between the cells we route metal1 horizontally and metal2 vertically.

Placement & Routing

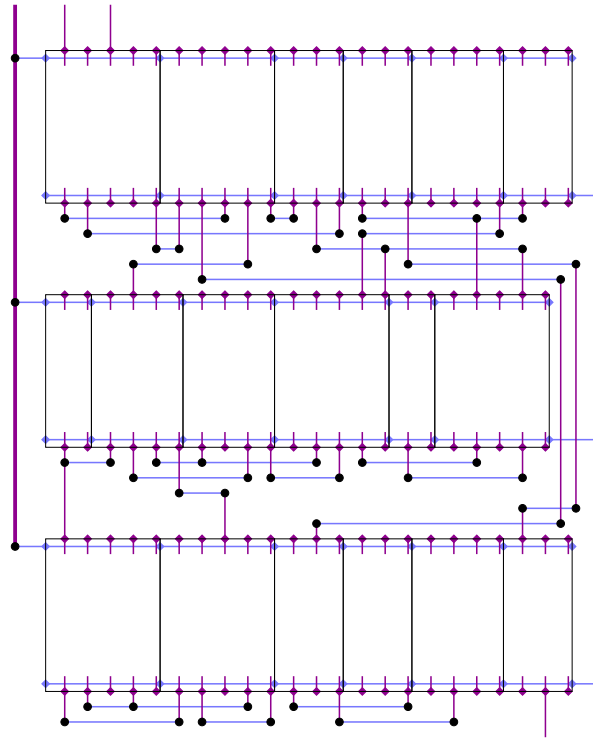
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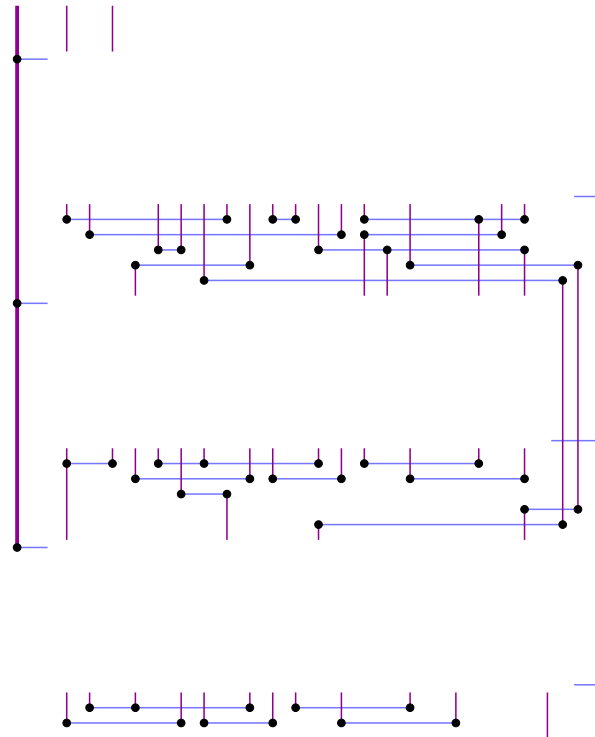
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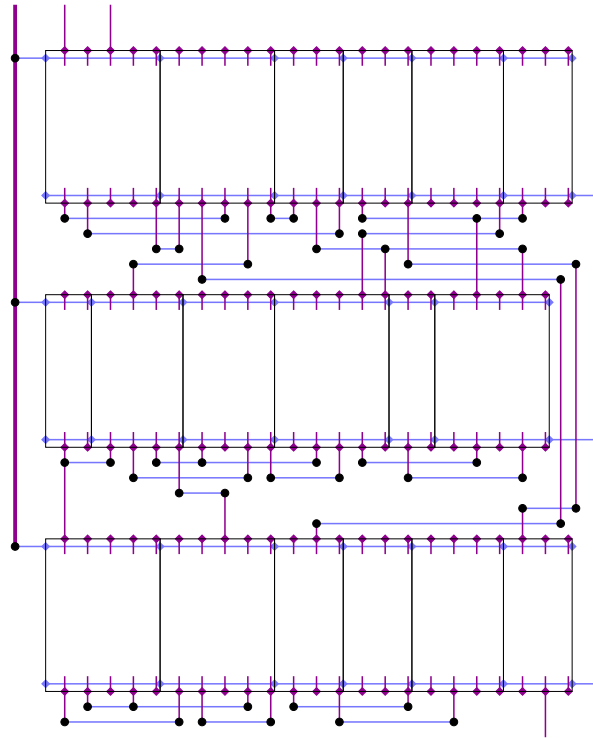
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Placement & Routing

Routing



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Placement & Routing

Two conductor routing

- Conductor A for horizontal inter-cell routing ⁴
Conductor B for vertical
- This logical approach means that we should never have to worry about signals crossing.
This makes life considerably easier for a computer (or even a human) to complete the routing.
- We must only ensure that two signals will not meet in the same horizontal or vertical channel.
- Computer algorithms can be used to ensure placement of cells such that wires are short.⁵
- Further computer algorithms can be used to optimize the routing itself.

⁴In the two-metal example Conductor A is Metal1 and Conductor B is Metal2

⁵In VLSI circuits we often find that inter-cell wiring occupies more area than the cells themselves.

Standard Cell Design

More Metal Layers

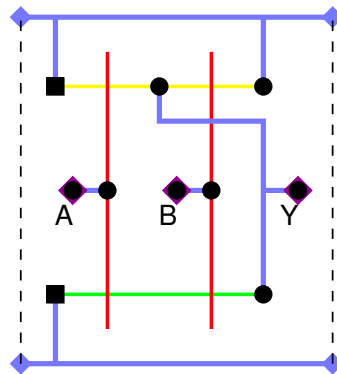
With three or more metal layers it is possible to take a different approach. The simplest example uses three metal layers.

- Standard Cells

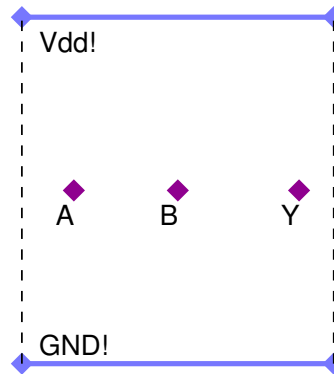
Use only metal1 except for I/O which is in metal2

- Two Conductor Routing

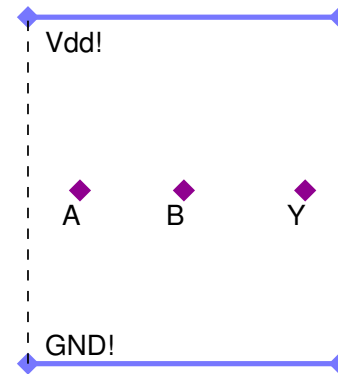
Uses metal2 and metal3



LAYOUT



ABSTRACT



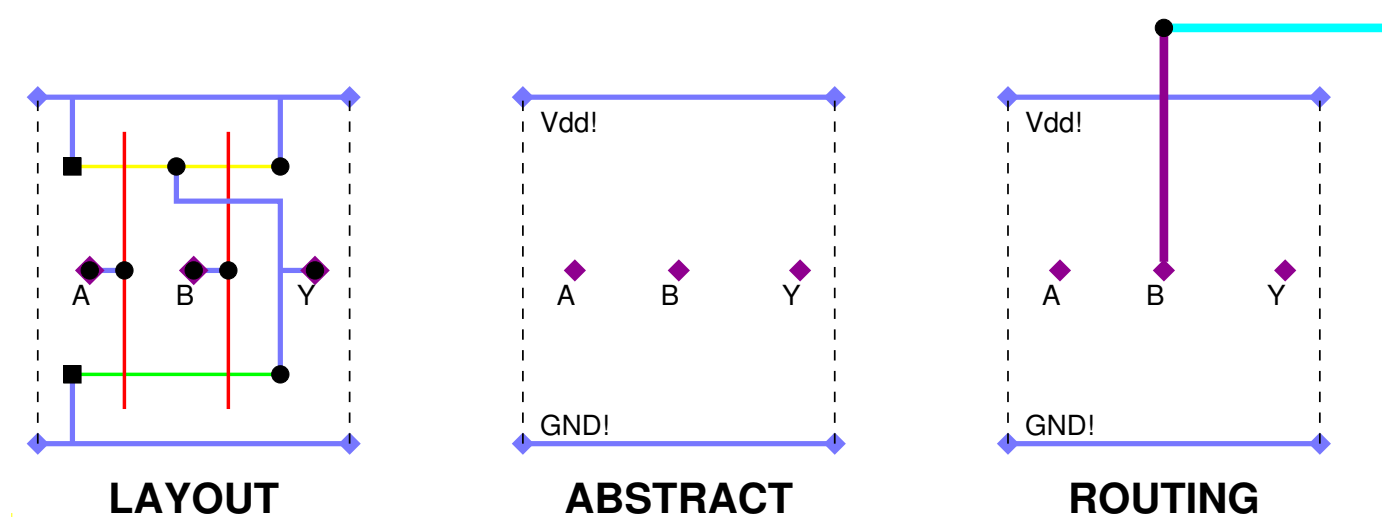
ROUTING

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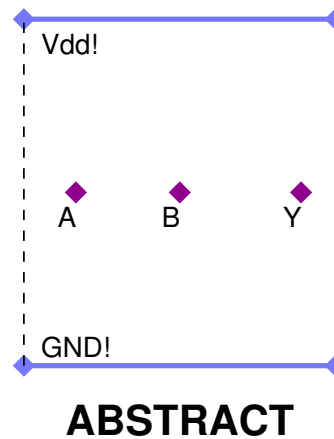
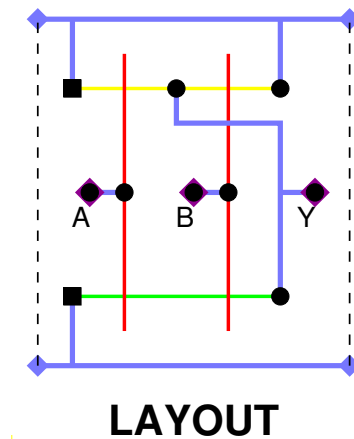


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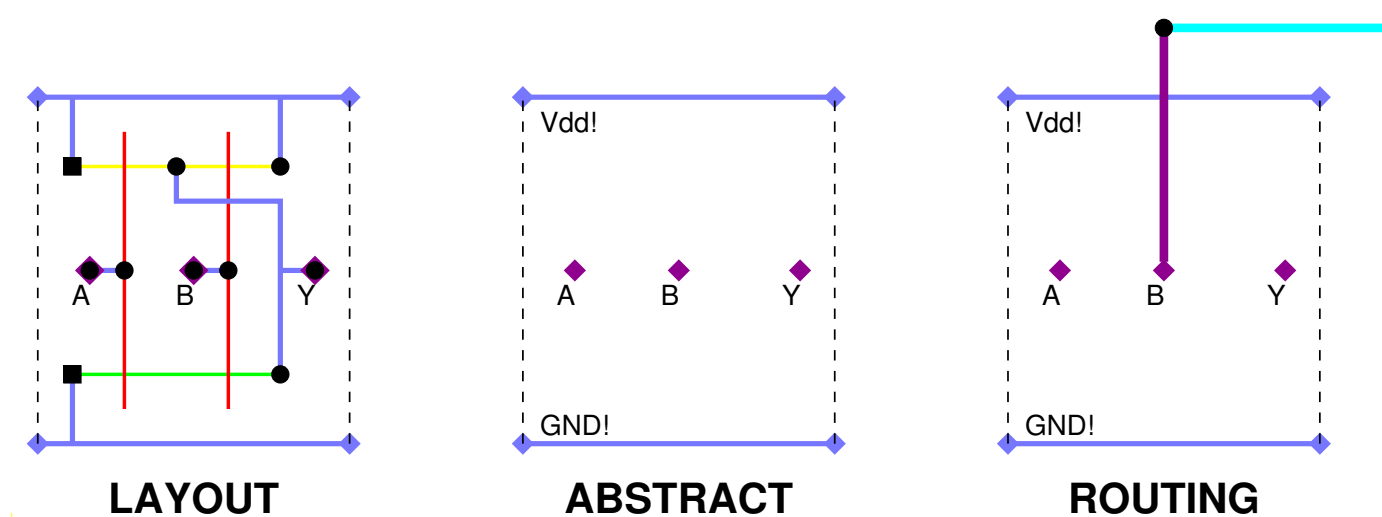


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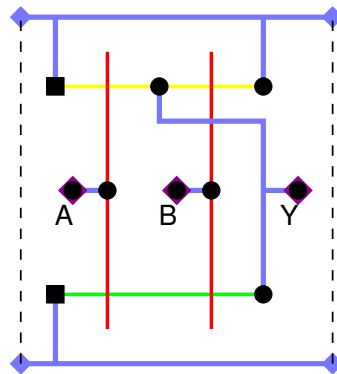


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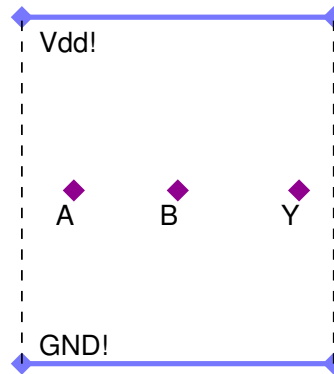
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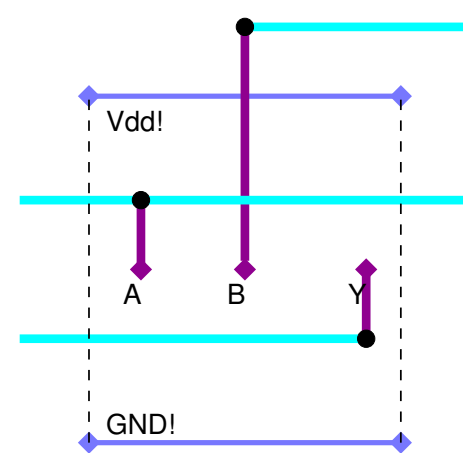
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LAYOUT



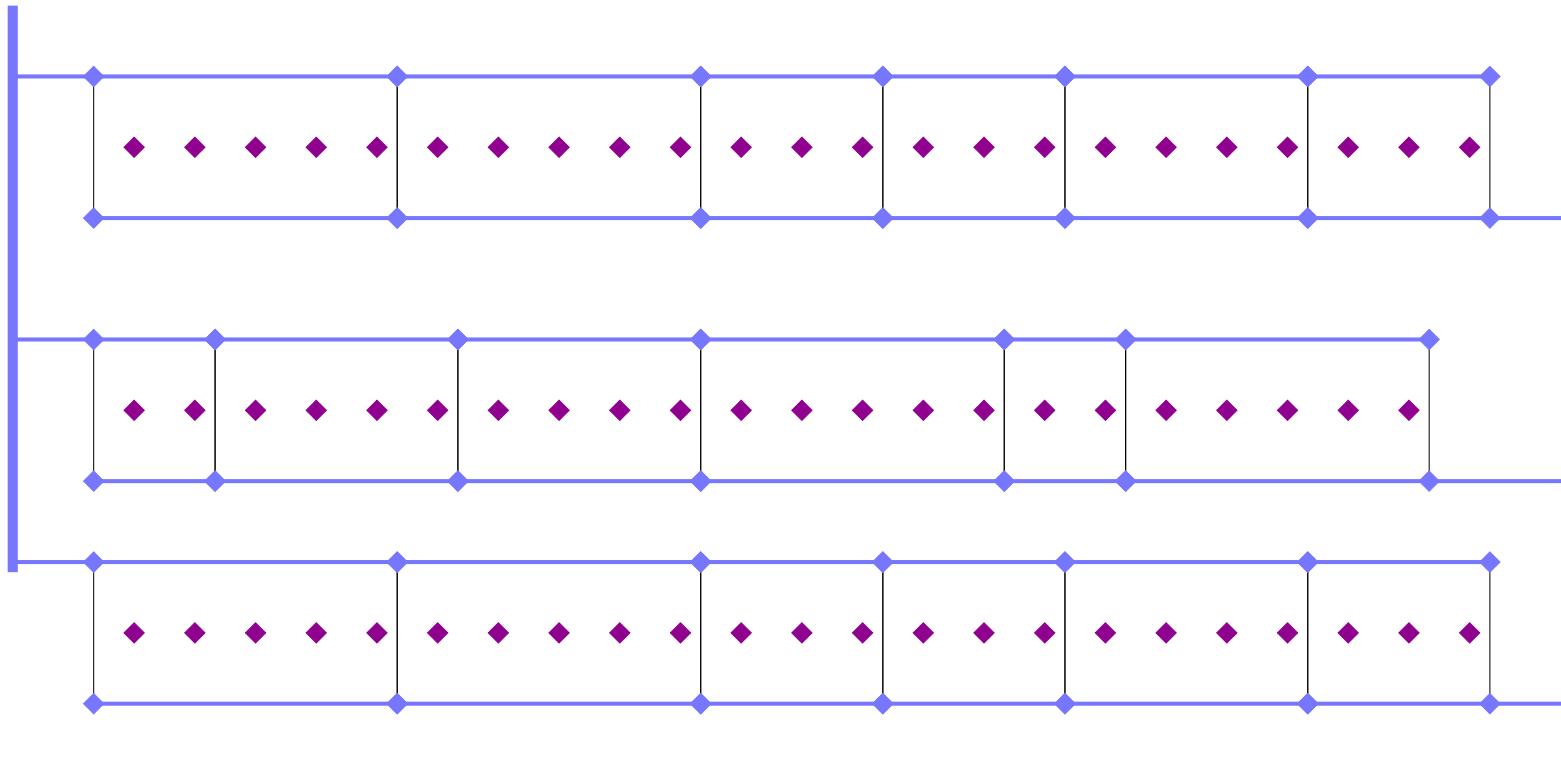
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ROUTING

Standard Cell Design

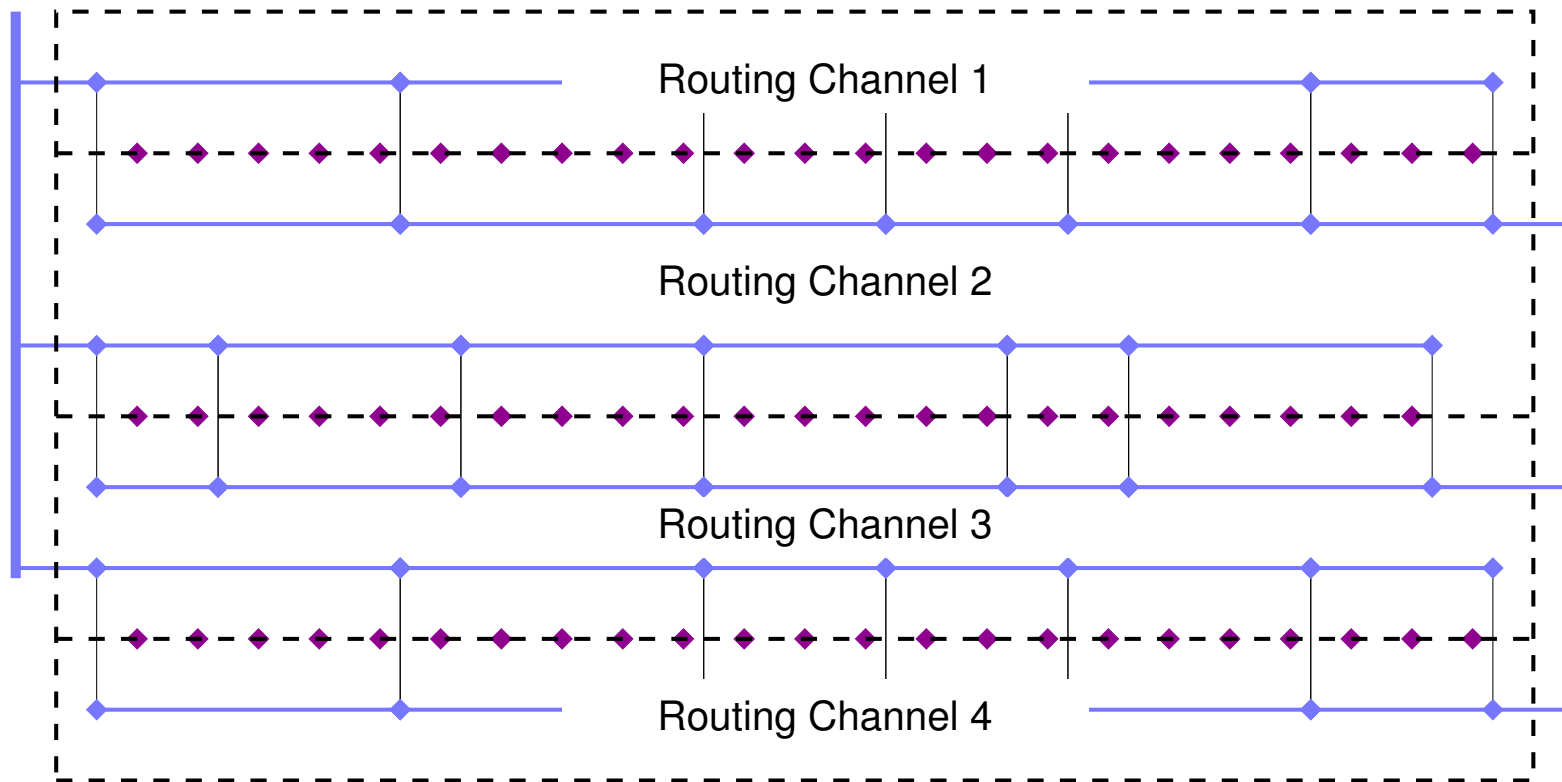
More Metal Layers



With this approach we can route safely over the cell to the specified pins leading to much smaller gaps between cell rows.

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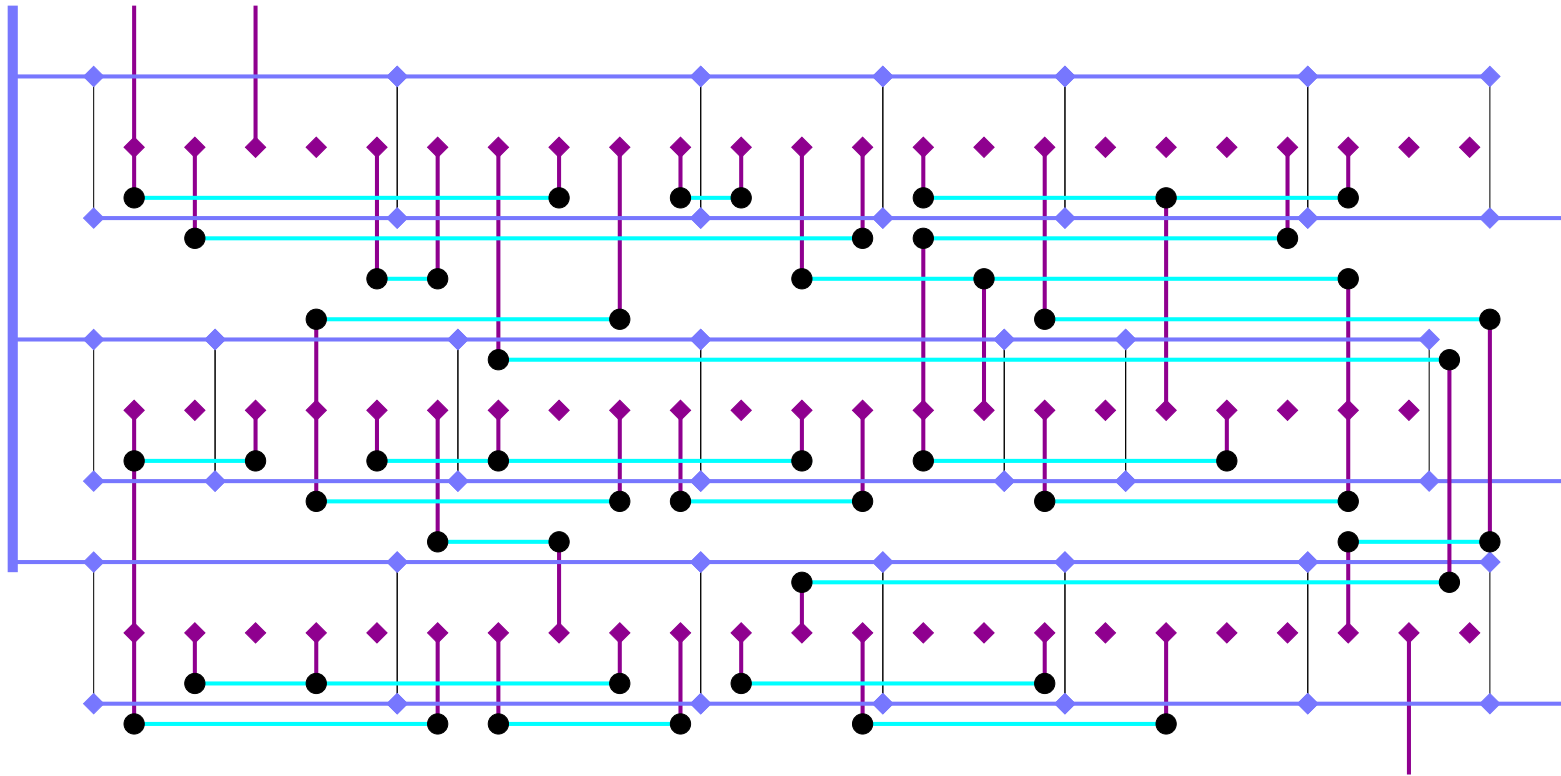
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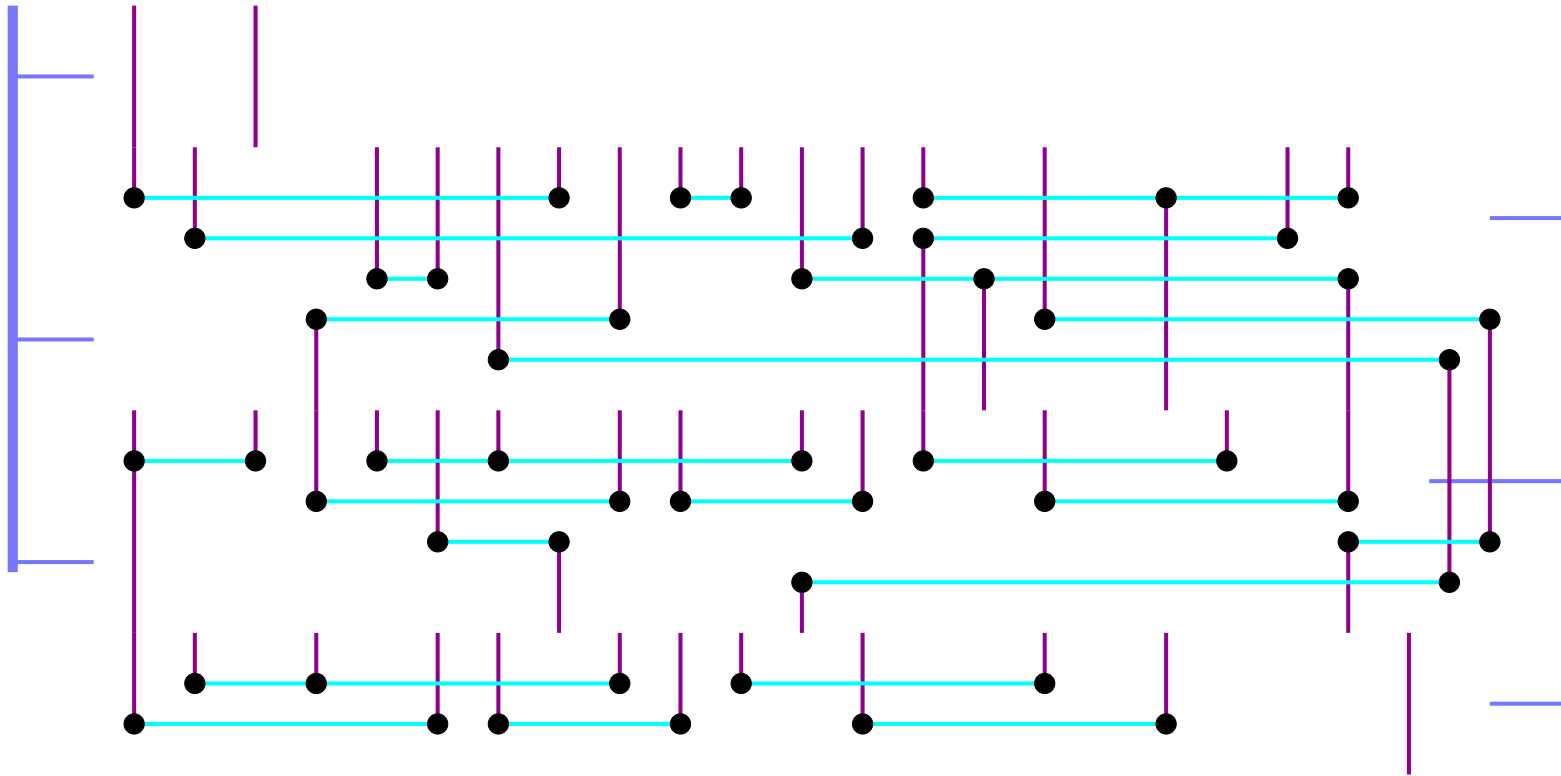
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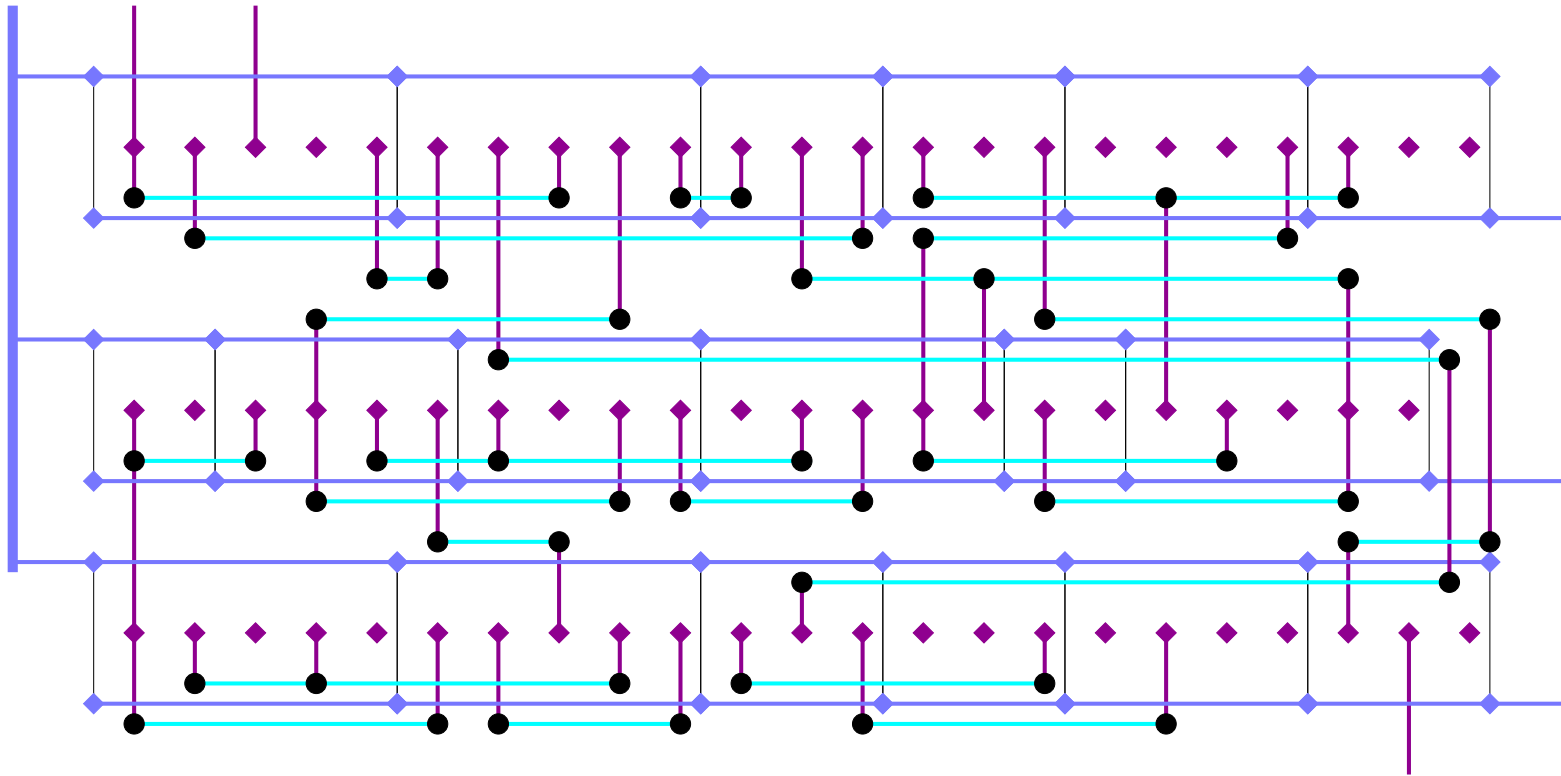
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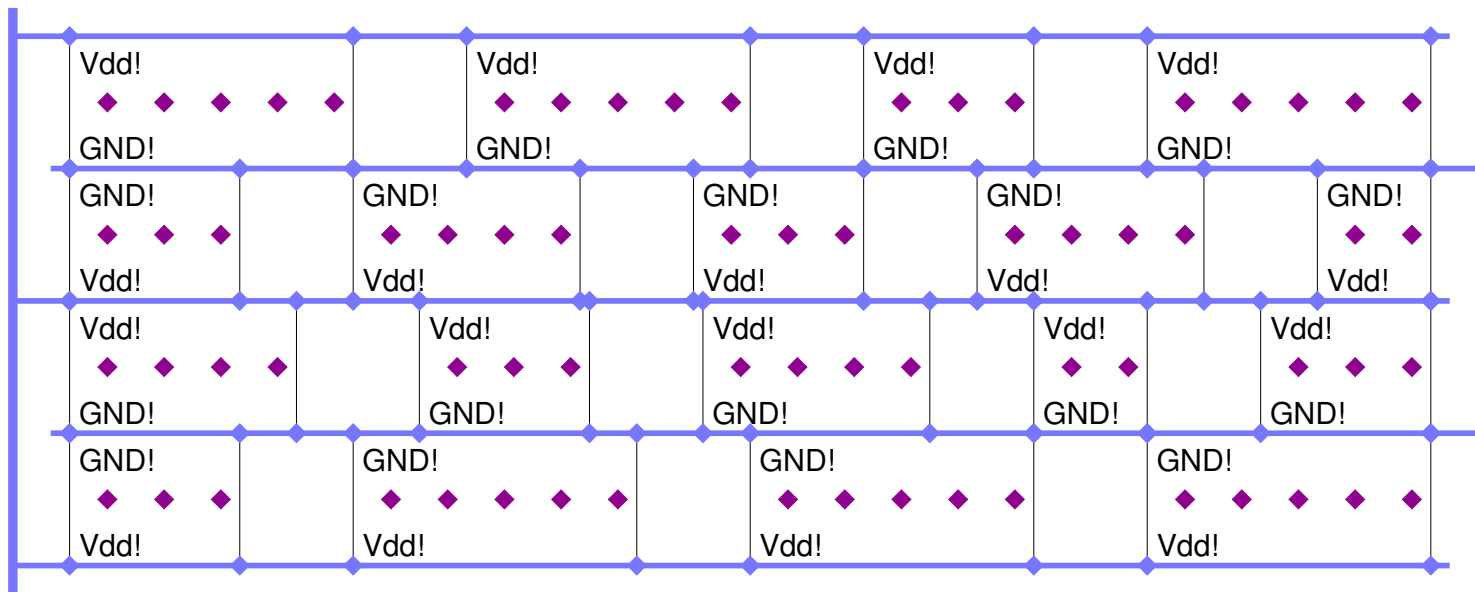
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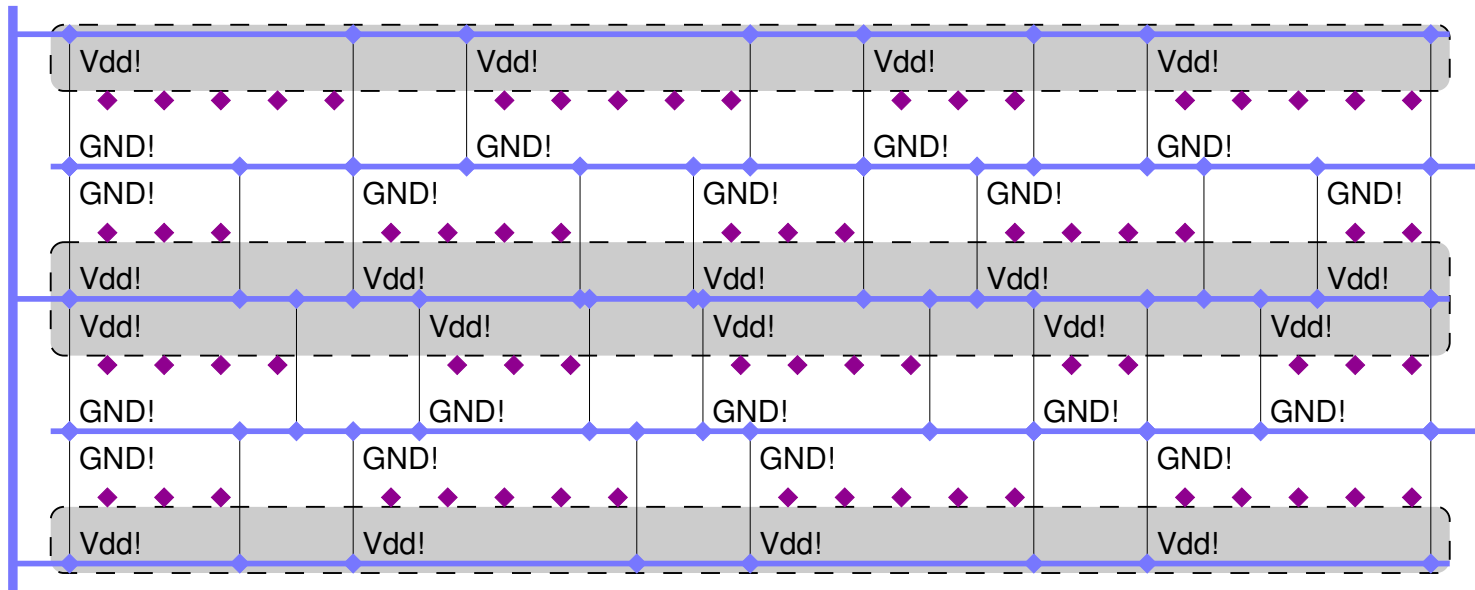
Alternative Placement Style



By flipping every second row it may be possible to eliminate gaps between rows. N-wells are merged and power or ground rails are shared. This approach is normally associated with sparse rows and non channel based routing algorithms.

Standard Cell Design

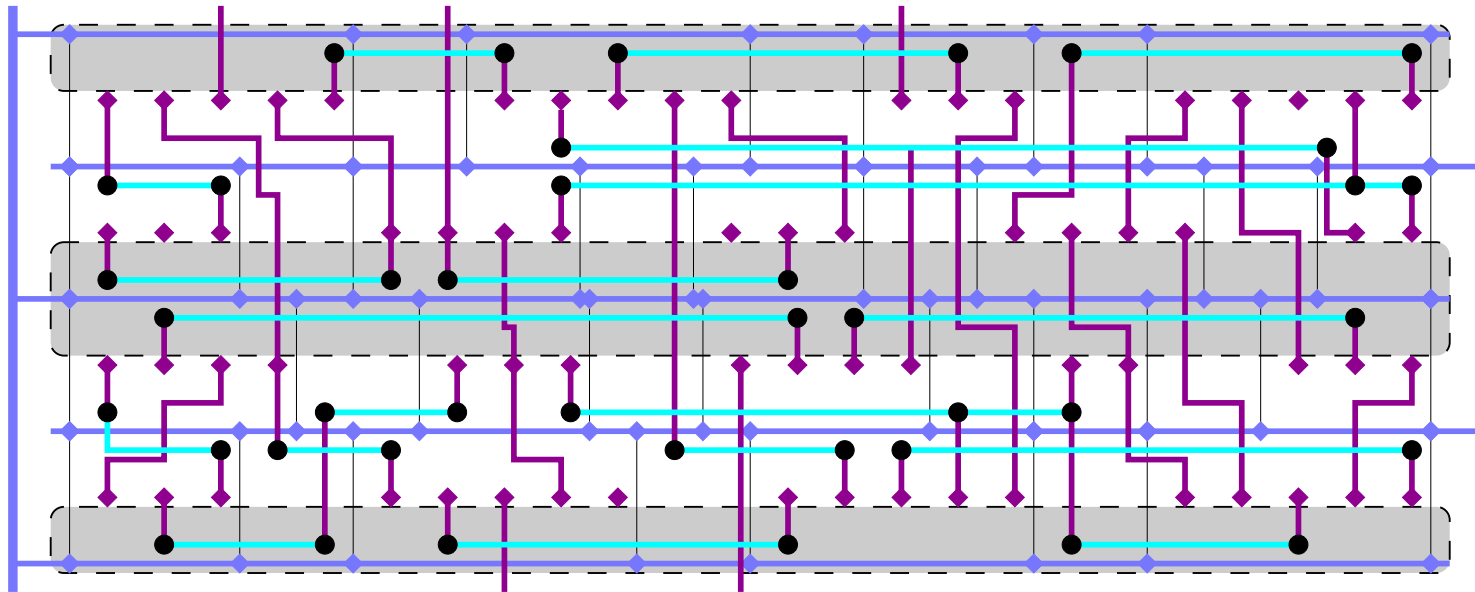
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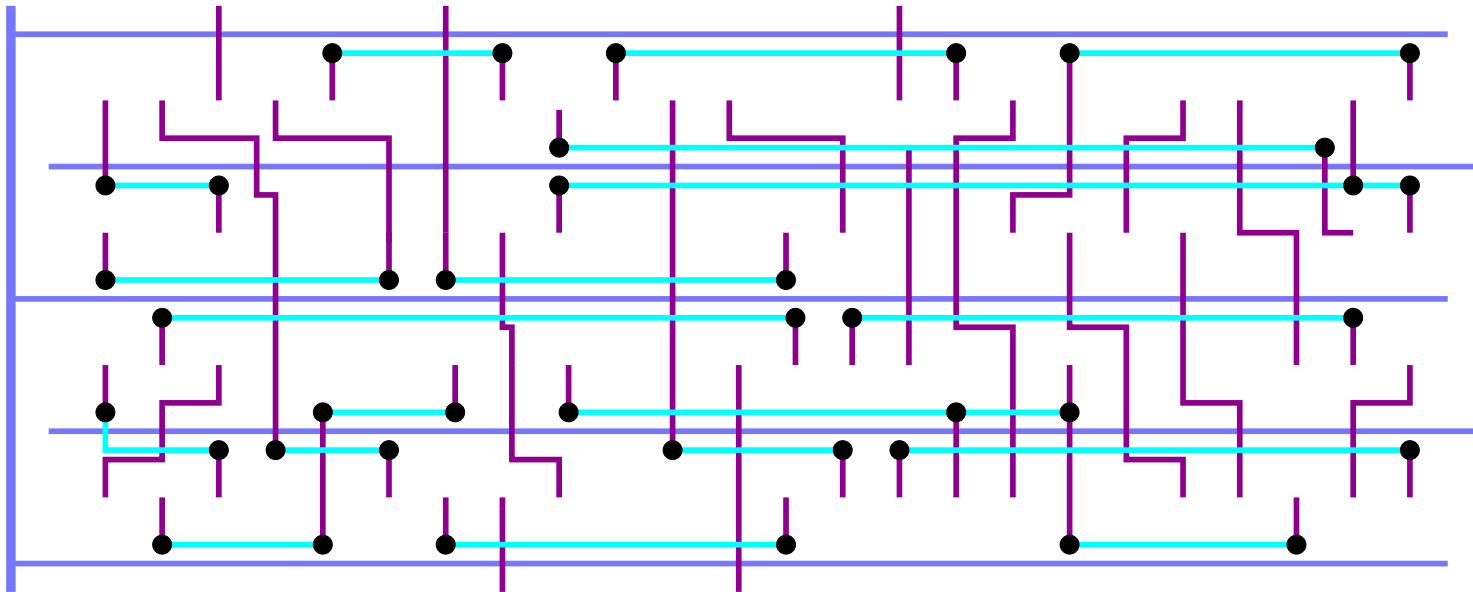
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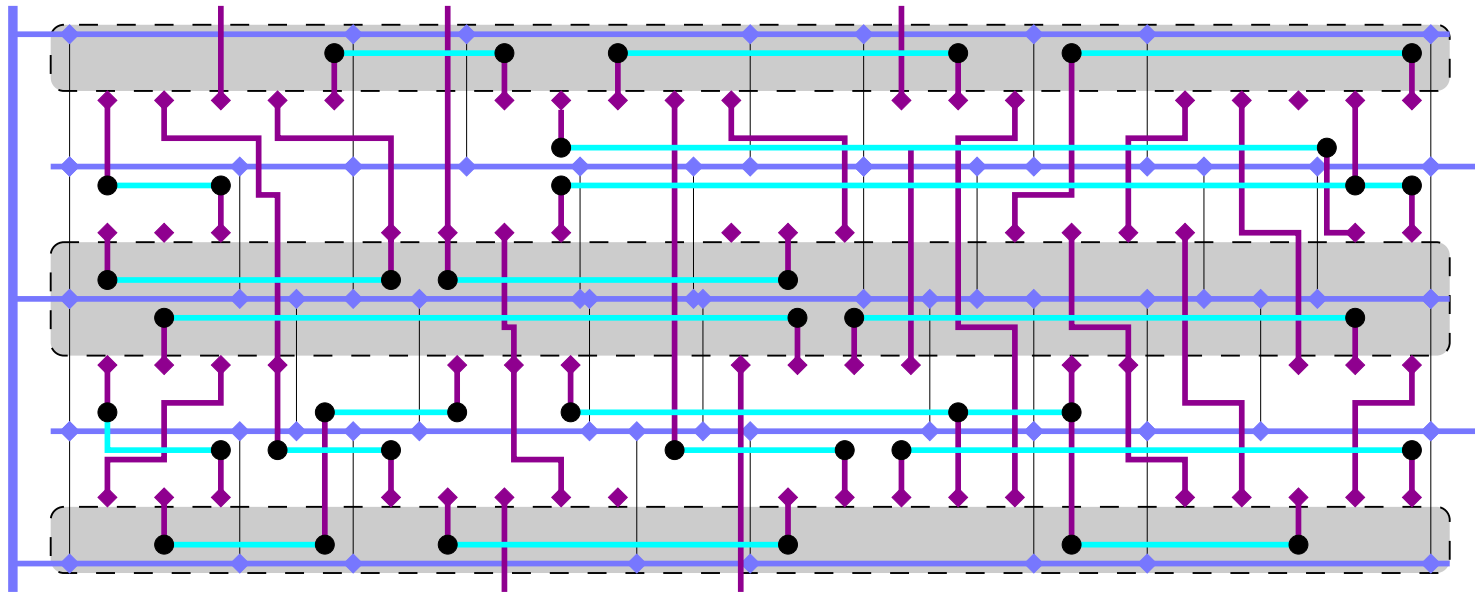
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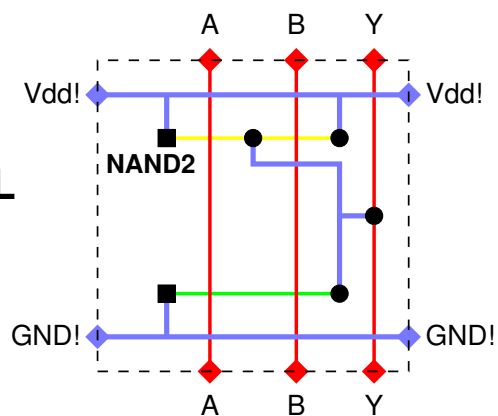
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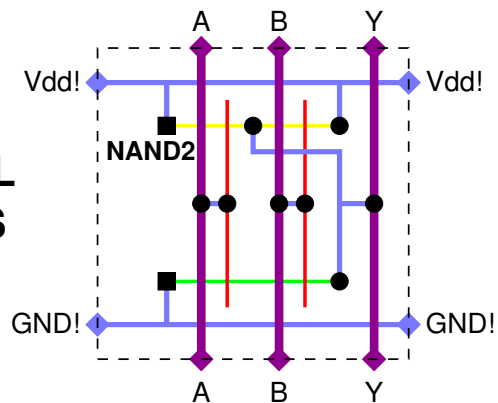


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1 METAL LAYER



2 METAL LAYERS



3 METAL LAYERS

