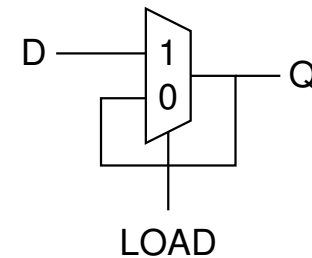
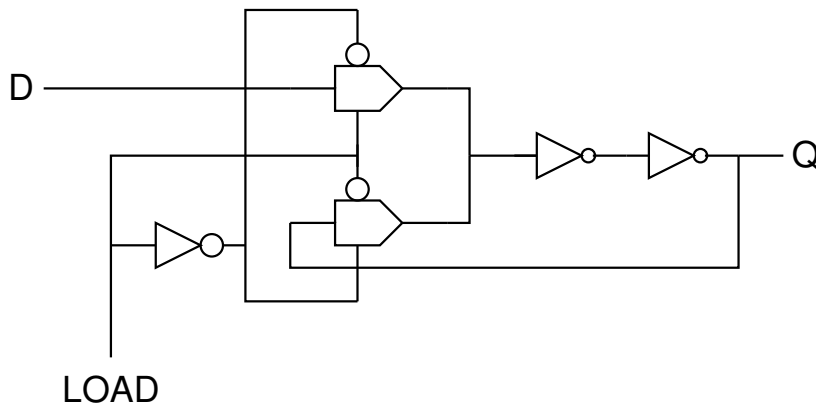


Latches and Flip-Flops

- CMOS transmission gate latch

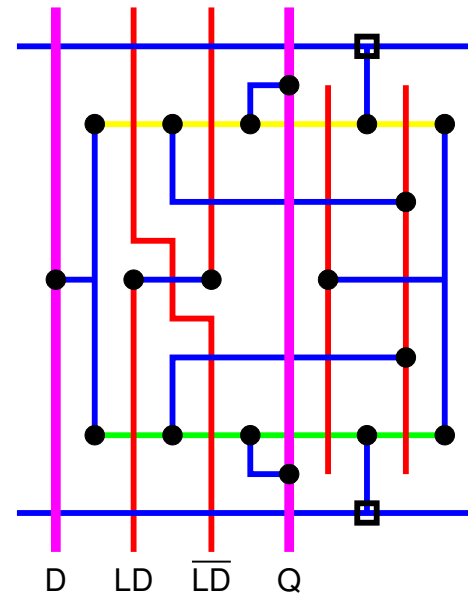
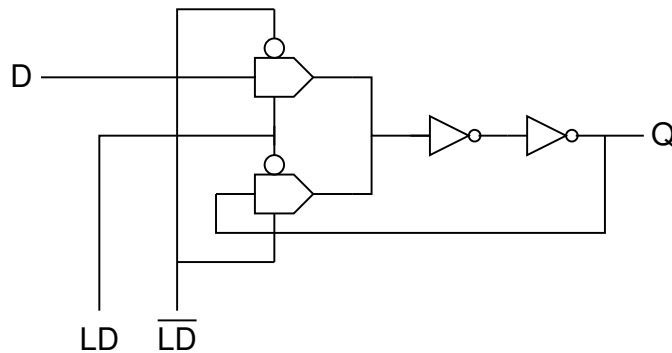


A simple transparent latch can be build around a transmission gate multiplexor

- transparent when load is high
- latched when load is low
- two inverters are required since the transmission gate cannot drive itself

Latches and Flip-Flops

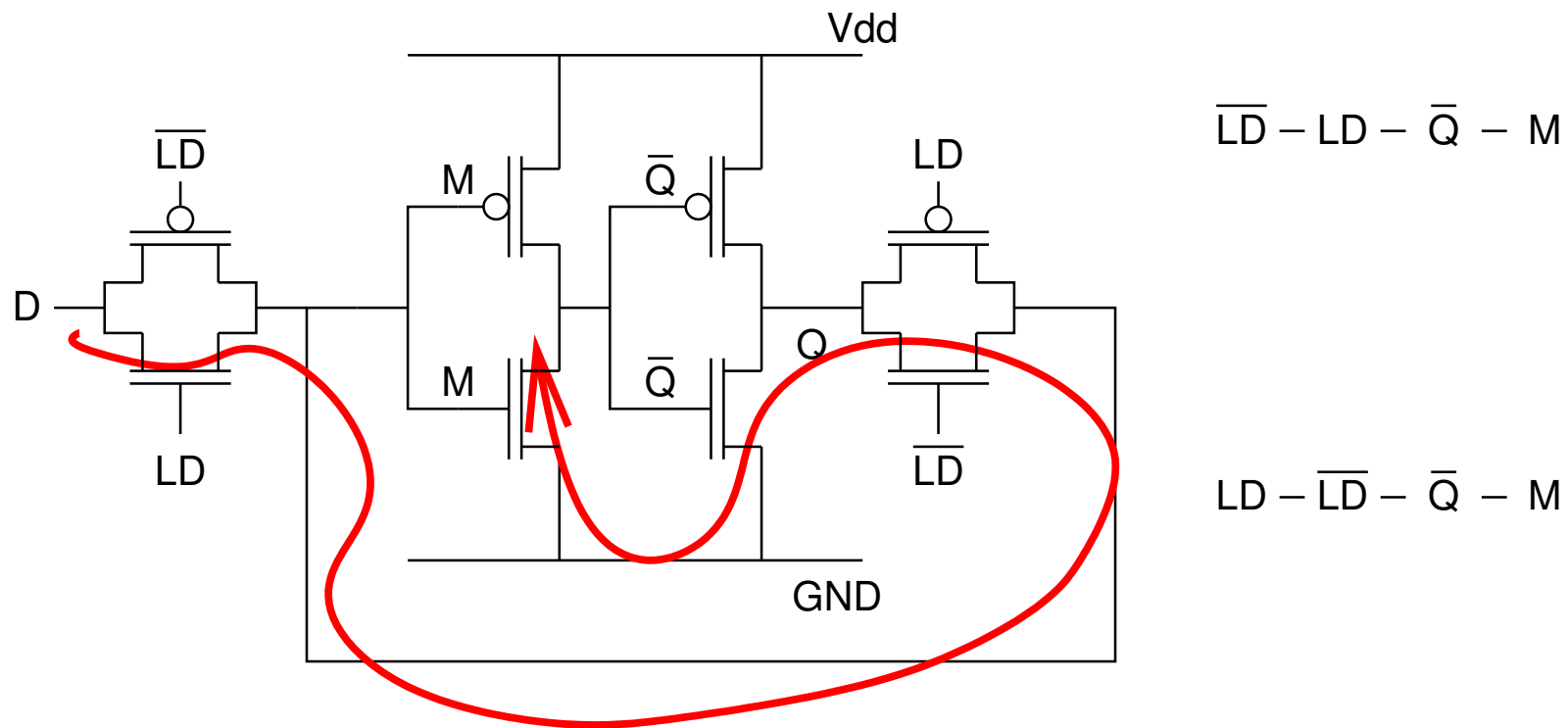
- Transmission gate latch layout



- a compact layout is possible using 2 layer metal

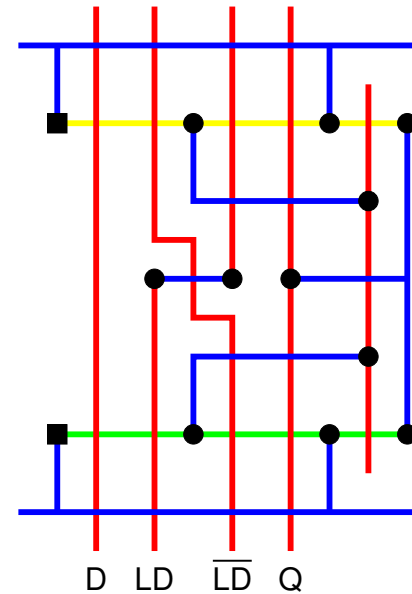
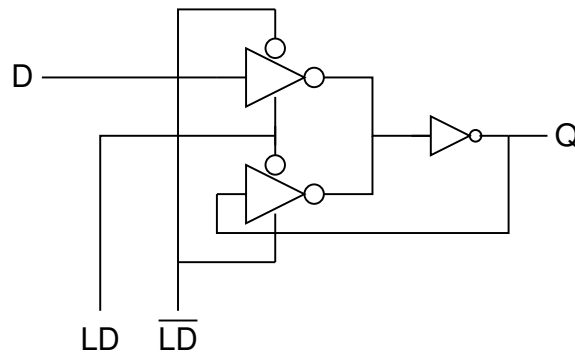
Latches and Flip-Flops

- Euler paths for transmission gate latch



Latches and Flip-Flops

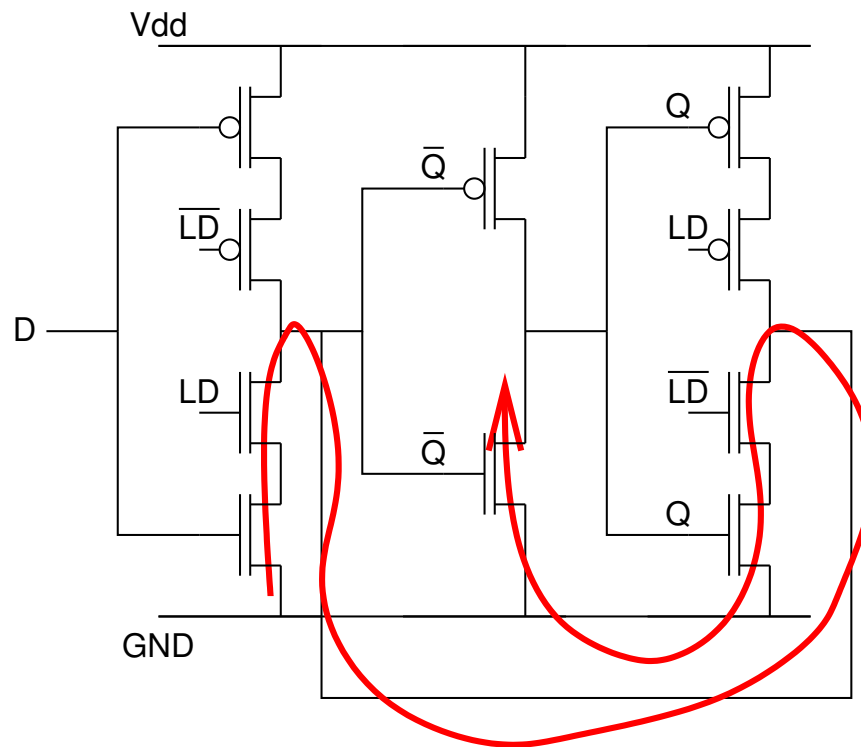
- A simpler layout may be achieved using tristate inverters.



- this design requires two additional transistors but may well be more compact.

Latches and Flip-Flops

- Euler paths for tristate inverter based latch

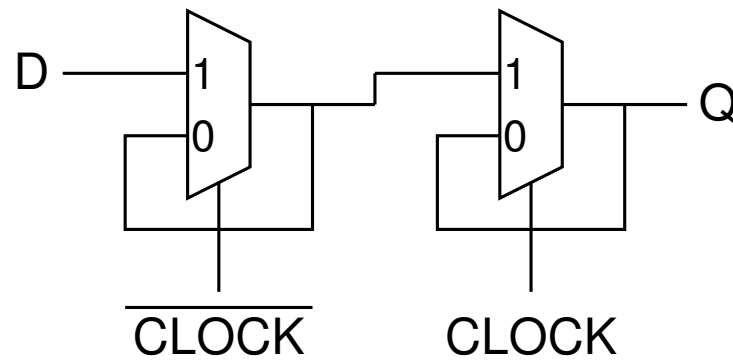


$D - \overline{LD} - LD - Q - \overline{Q}$

$D - LD - \overline{LD} - Q - \overline{Q}$

Latches and Flip-Flops

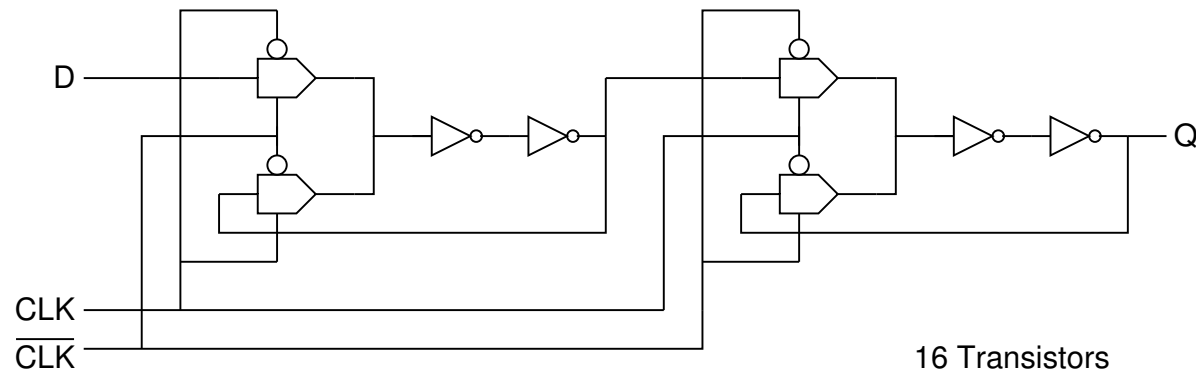
- For use in simple synchronous circuits we use a pair of latches in a master slave configuration.



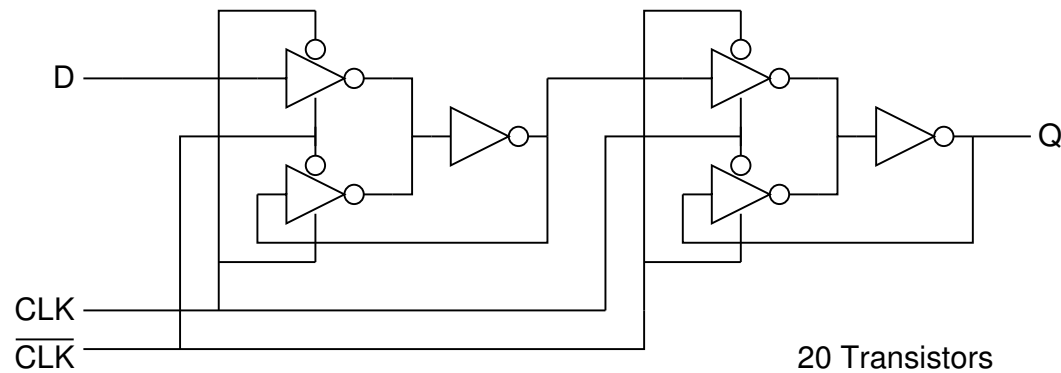
- this avoids the race condition in which a transparent latch drives a second transparent latch operating on the same clock phase.
- the circuit behaves as a rising edge triggered D type flip-flop.

Latches and Flip-Flops

- Transmission gate implementation

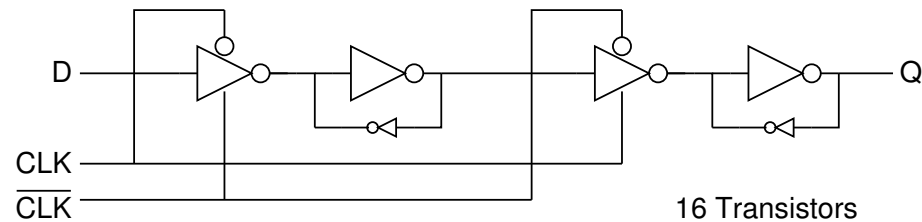


- Tristate inverter implementation



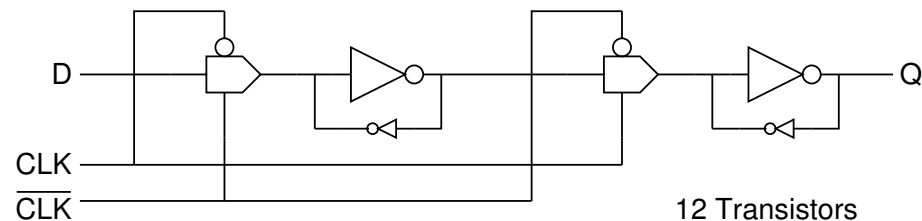
Latches and Flip-Flops

- Tristate inverter implementation based on "Jamb" latches



- the tristate inverter must be strong enough to override the weak inverter

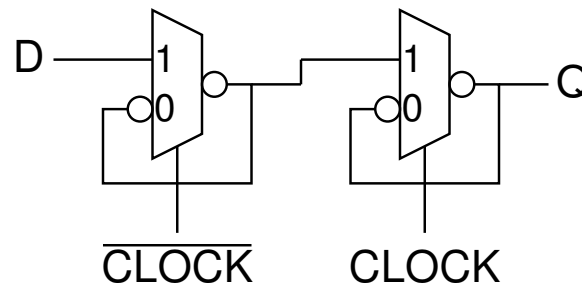
- Transmission gate implementation based on "Jamb" latches



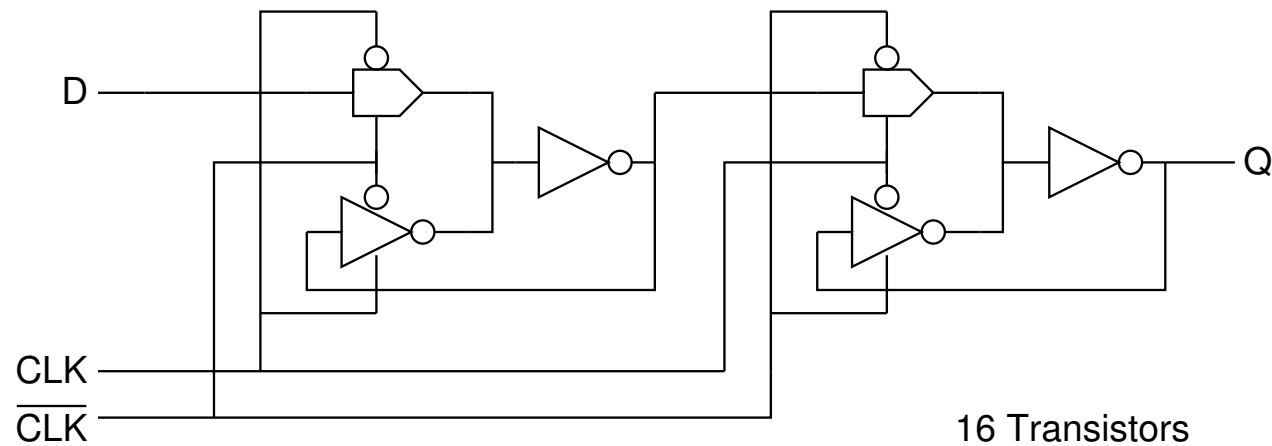
- this is less useful since its functionality depends on the drive strength at D

Latches and Flip-Flops

- Alternative configuration

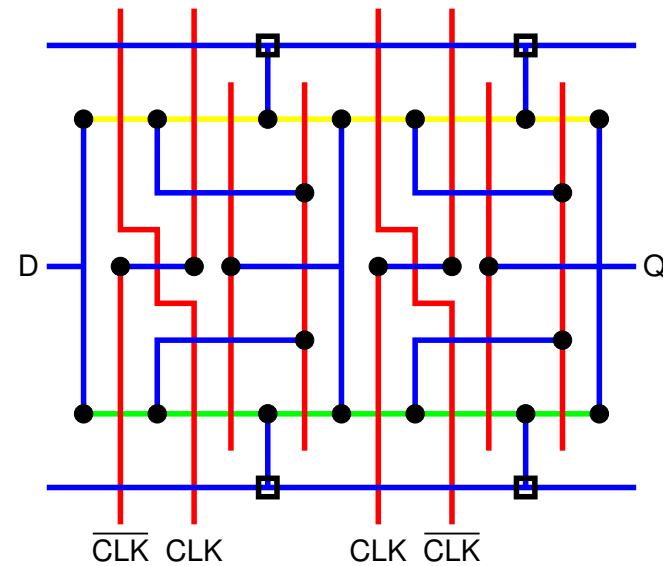
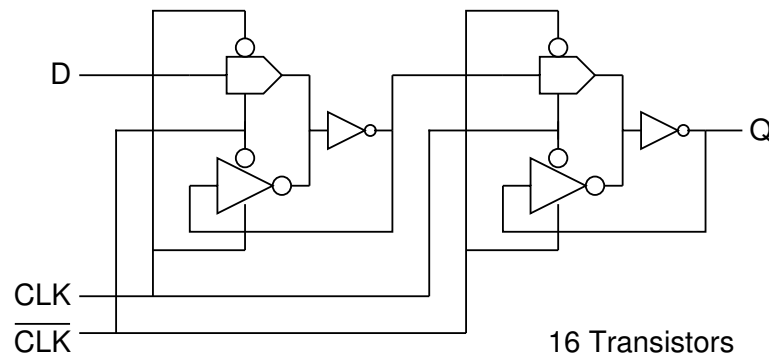


- Implementation



Latches and Flip-Flops

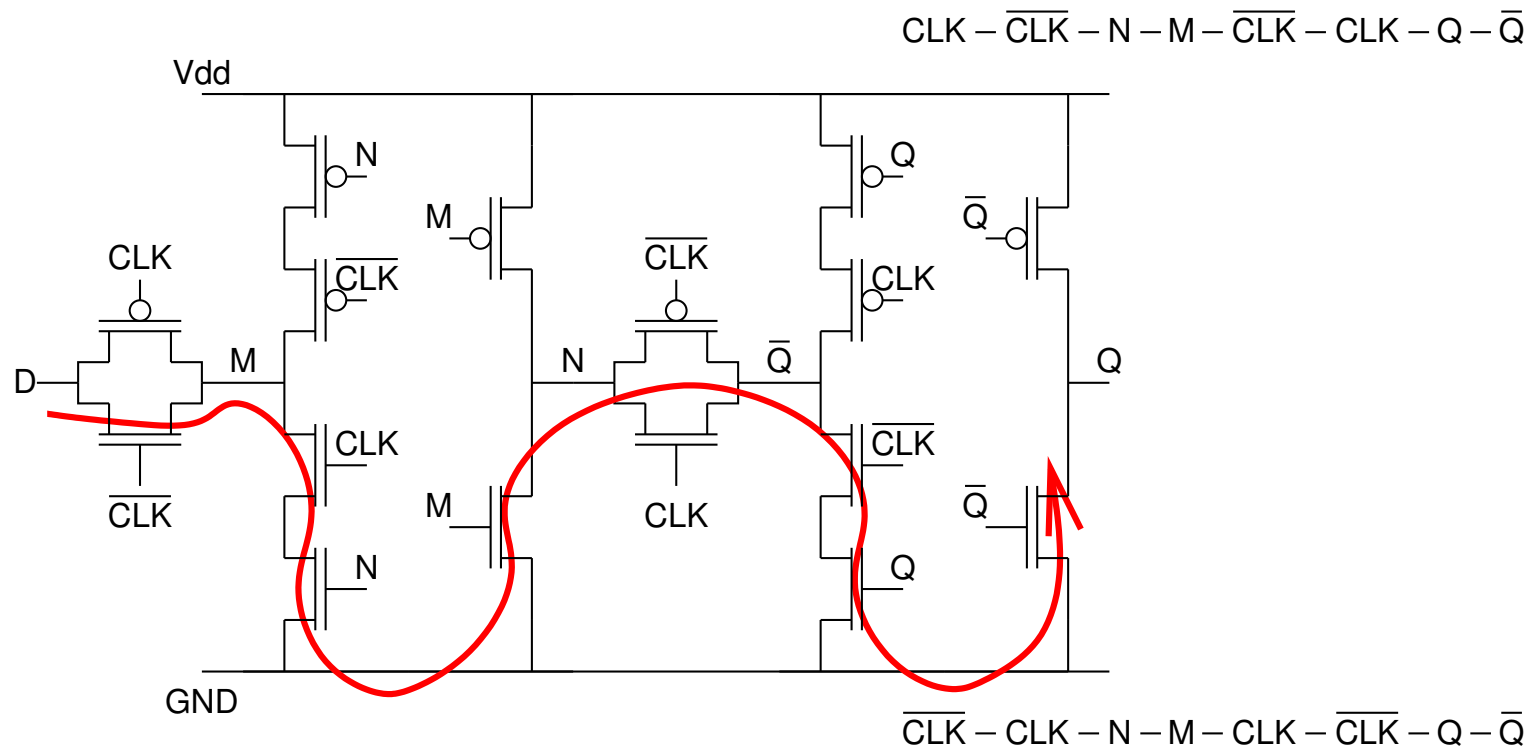
- Layout of master slave D type.



- very compact using alternative configuration.

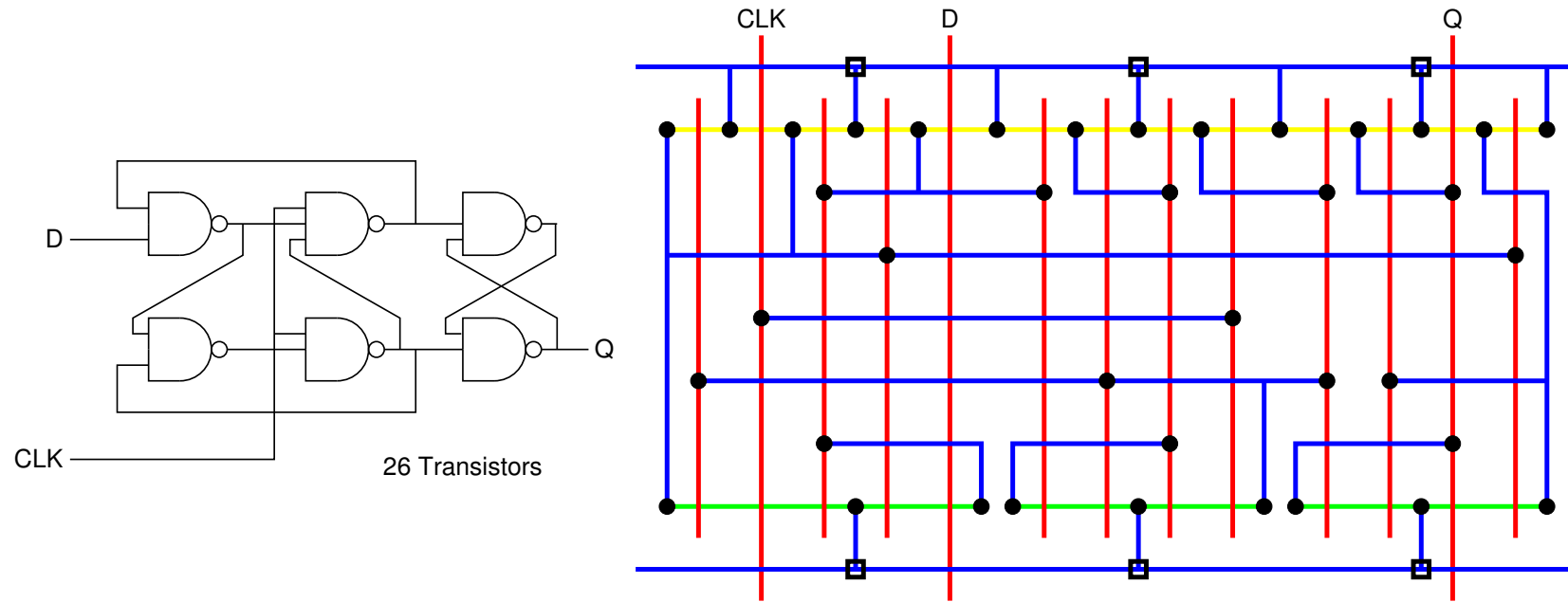
Latches and Flip-Flops

- Euler paths for master slave D type



Latches and Flip-Flops

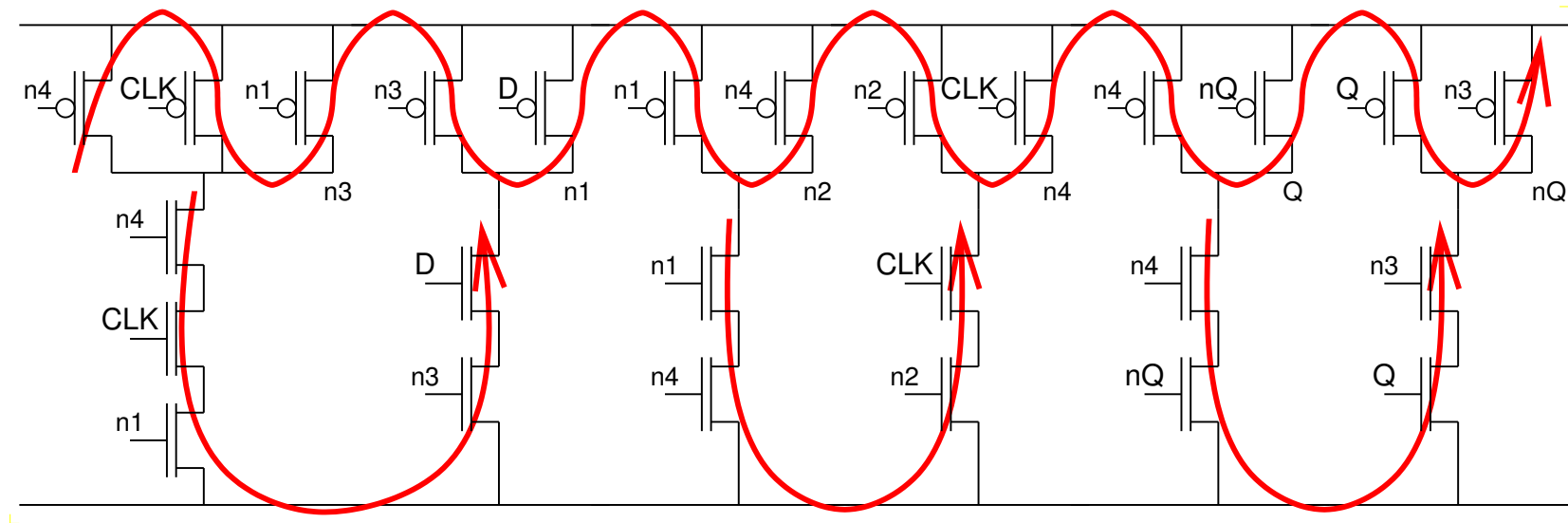
- For the same functionality we could use an edge triggered D type:



- a few more transistors
- more complex wiring
- simpler clock distribution

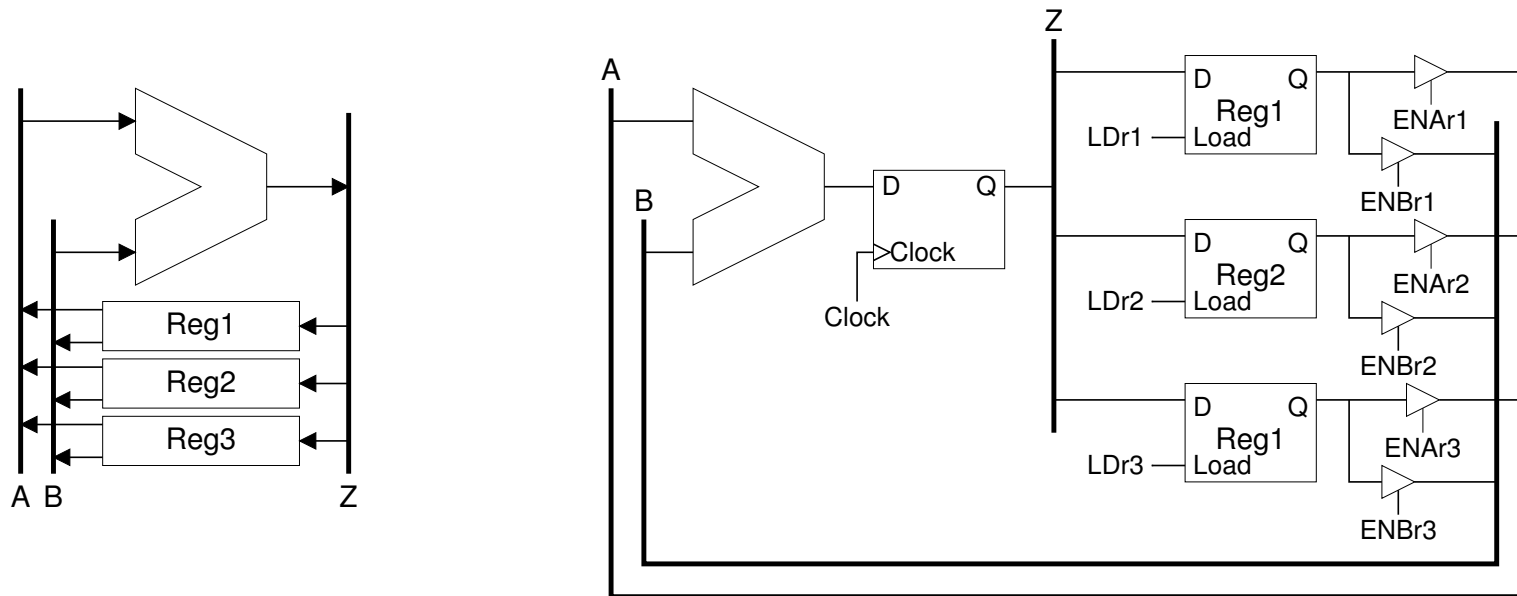
Latches and Flip-Flops

- Partial Euler paths for edge triggered D type



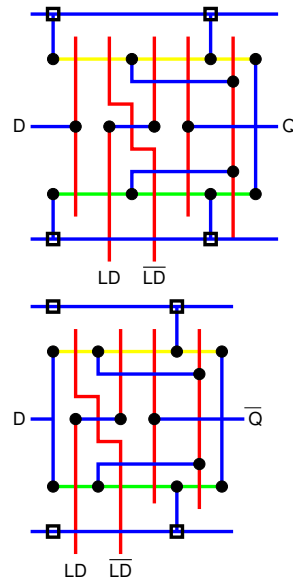
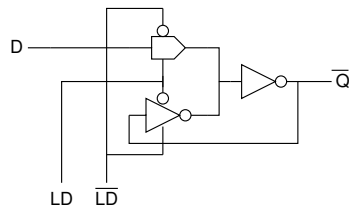
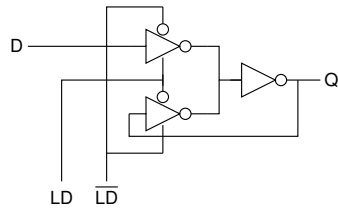
Register File

Where we have large amounts of storage the use of individual latches can lead to space saving.

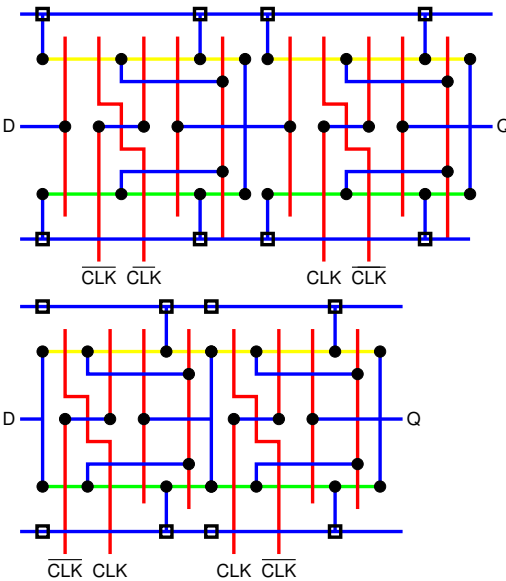
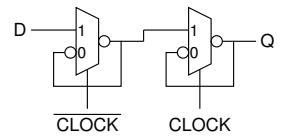
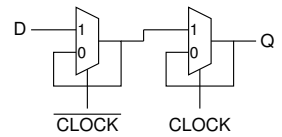


- Load signals must be glitch free with tightly controlled timing.
- Edge Triggered D-type prevents a race condition ($Reg1 \leftarrow Reg1 + Reg2$).

Latch

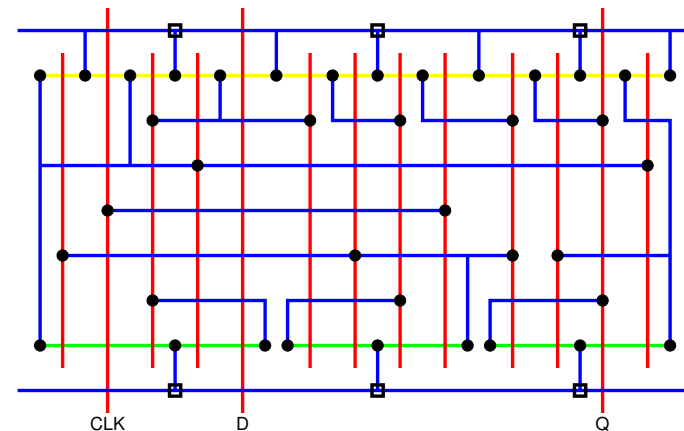
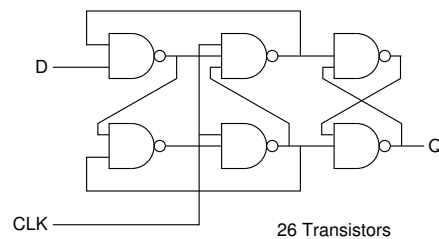


Master Slave D-Type Flip-Flop



*multiplexor based latches and flip-flops include distinctive polysilicon crossover

Edge Triggered D-Type Flip-Flop



Euler path analysis is applied creatively to these multi-gate cells – gates are often linked via the common gnd/pwr node
Final layouts will be more complex where clock buffers, reset circuitry and metal 2 i/o are included