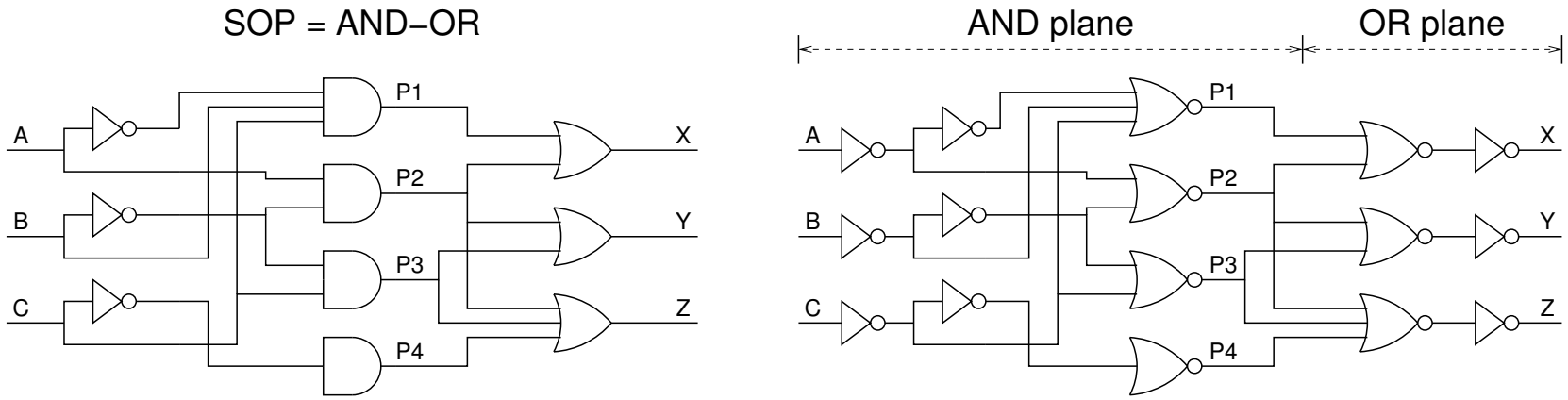
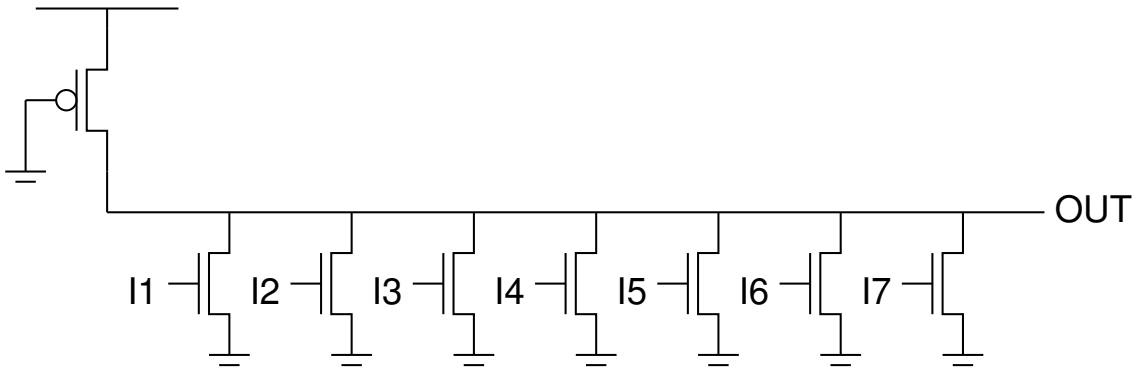
PLA structures

Programmable Logic Array structures provide a logical and compact method of implementing multiple SOP (Sum of Products) or POS expressions.



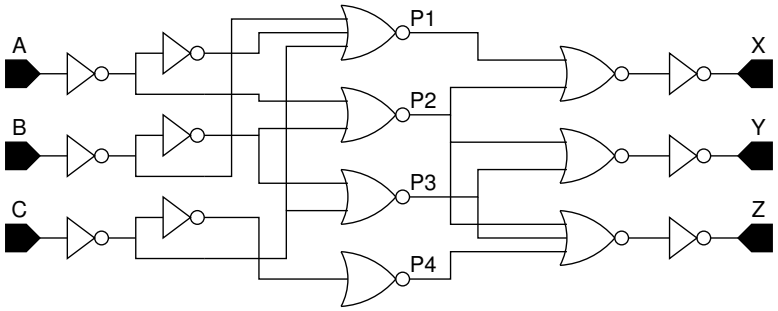
Most PLA structures employ pseudo-NMOS NOR gates using a P-channel device in place of the NMOS depletion load.

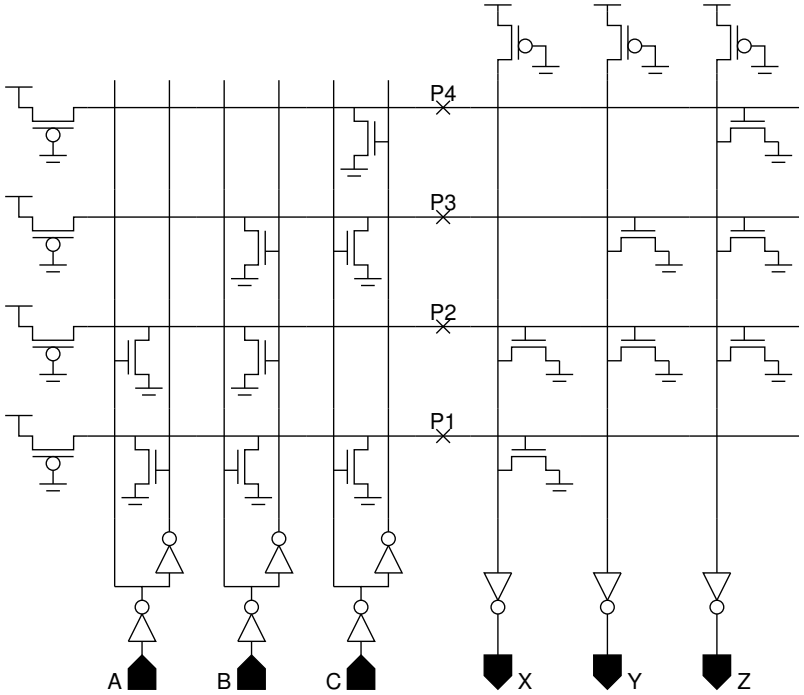
Pseudo-NMOS NOR gate



- Unlike complementary CMOS circuits, these gates will dissipate power under static conditions (since the P device is always on).
- The P and N channel devices must be ratioed in order to create the required low output voltage.
- This ratioing results in a slower gate, although there is a trade-off between gate speed and static power dissipation.

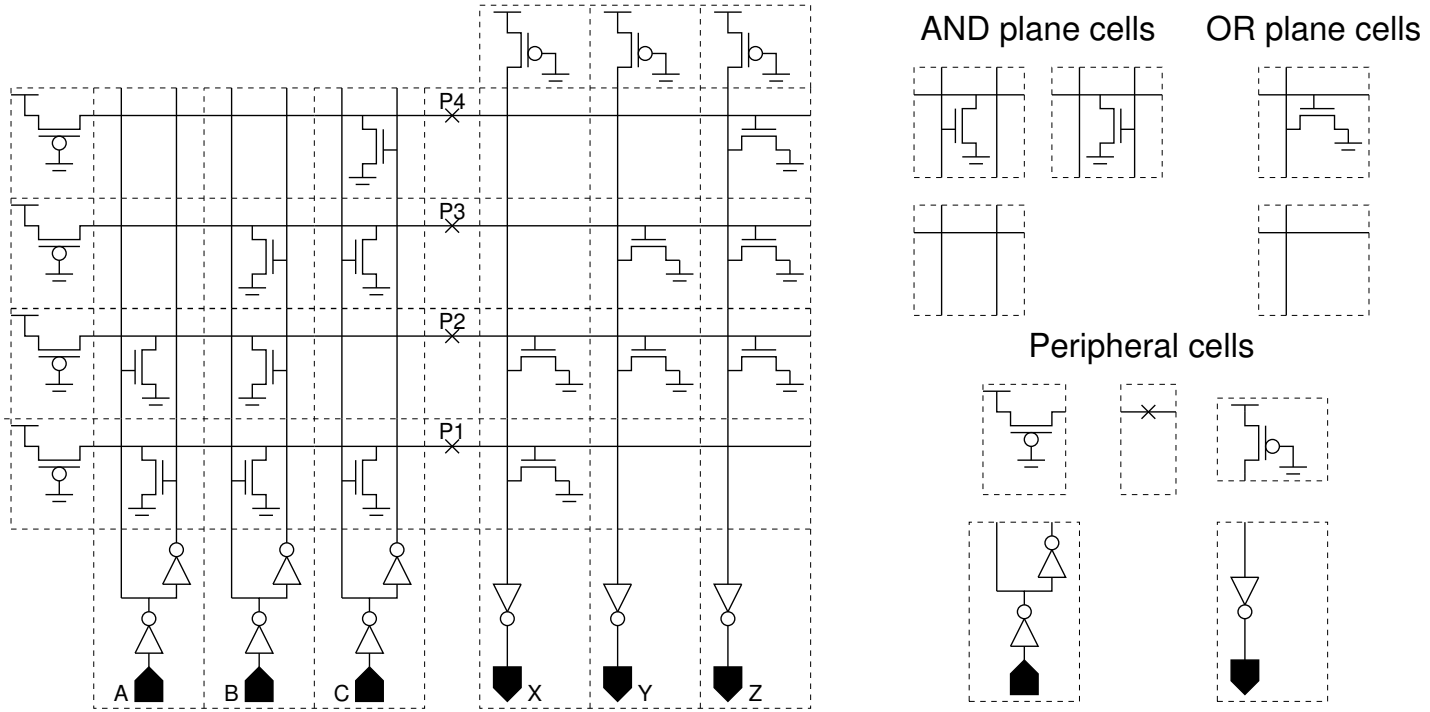
PLA structure





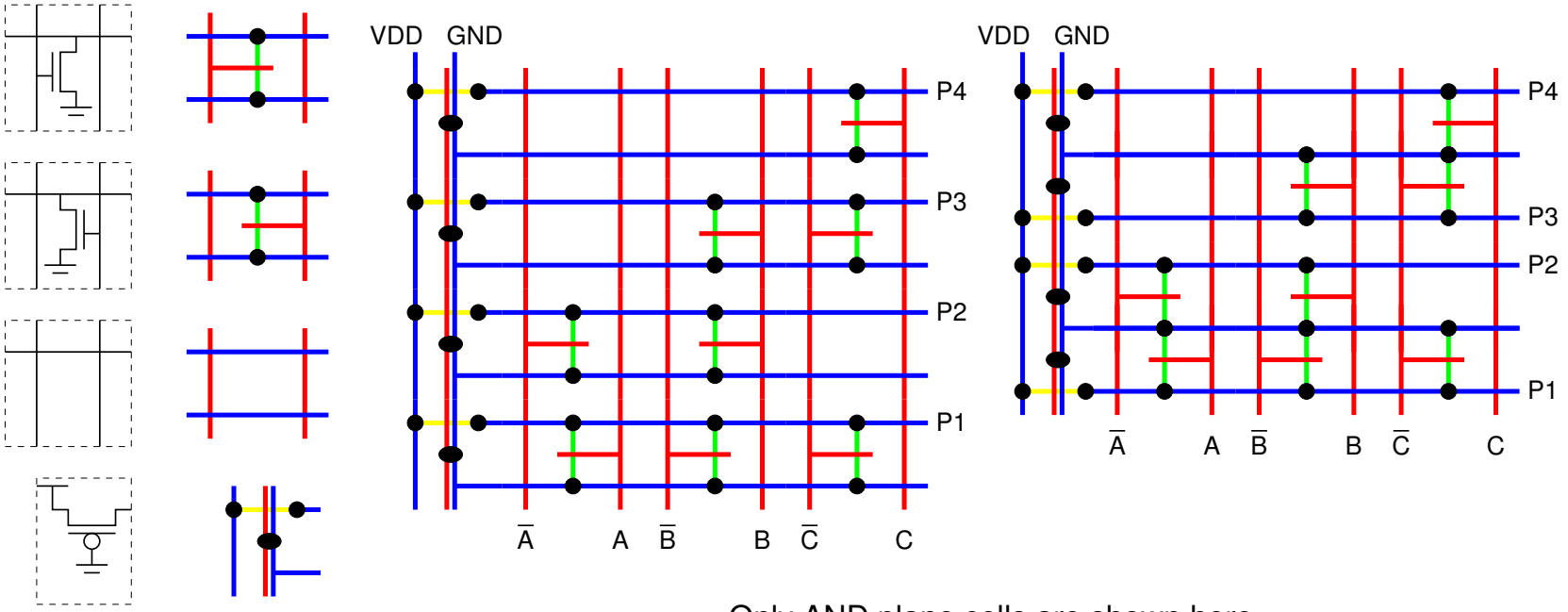
- A regular layout is employed, with columns for inputs and outputs and rows for intermediate expressions.

PLA structure



- Layout is simply a matter of selecting and placing rectangular cells from a limited set.

PLA structure

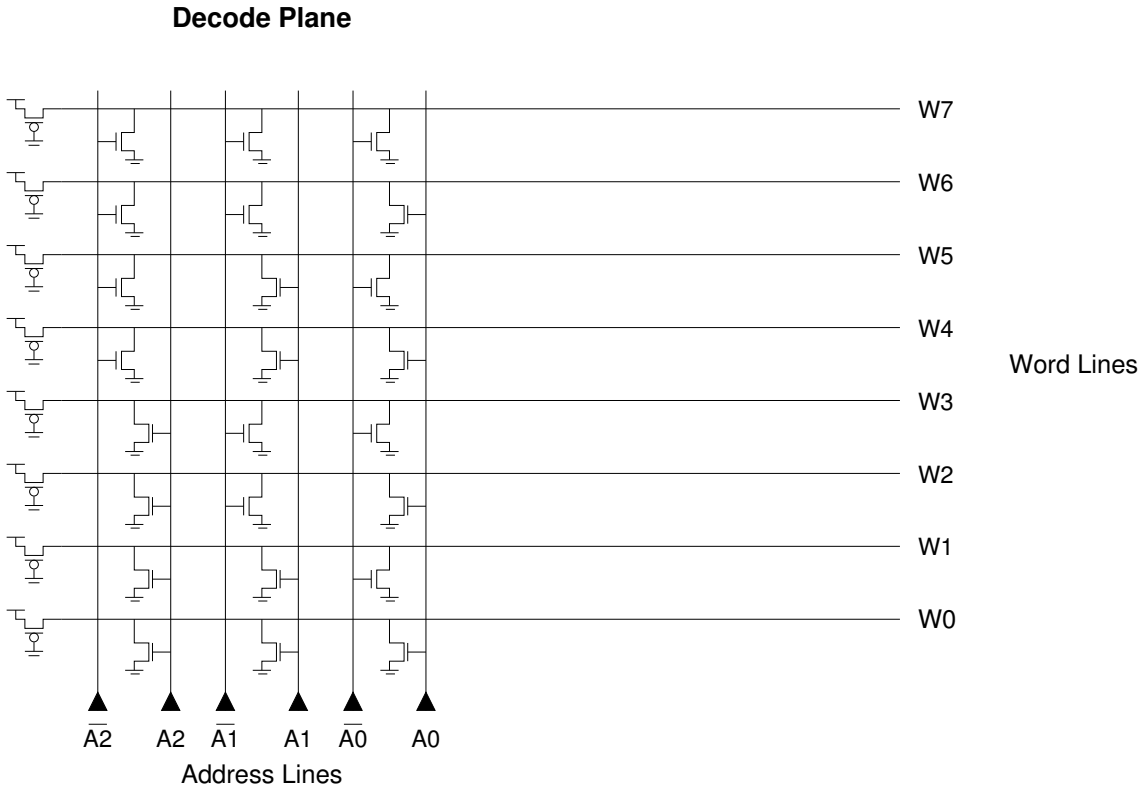


Only AND plane cells are shown here

- Conversion to *sticks* is straight forward with opportunities for further optimization.

ROMs

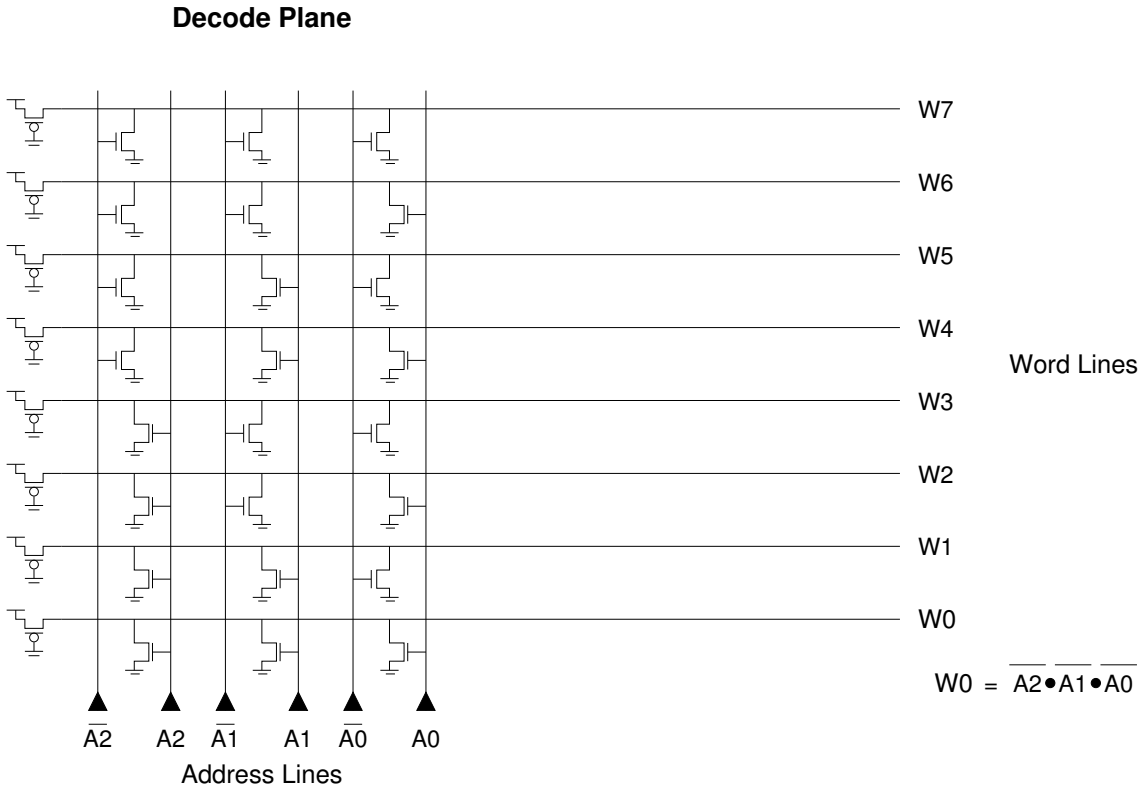
- A ROM may simply be a PLA with fixed decode plane[1]



[1]RAM structures can make use of the same decode plane.

ROMs

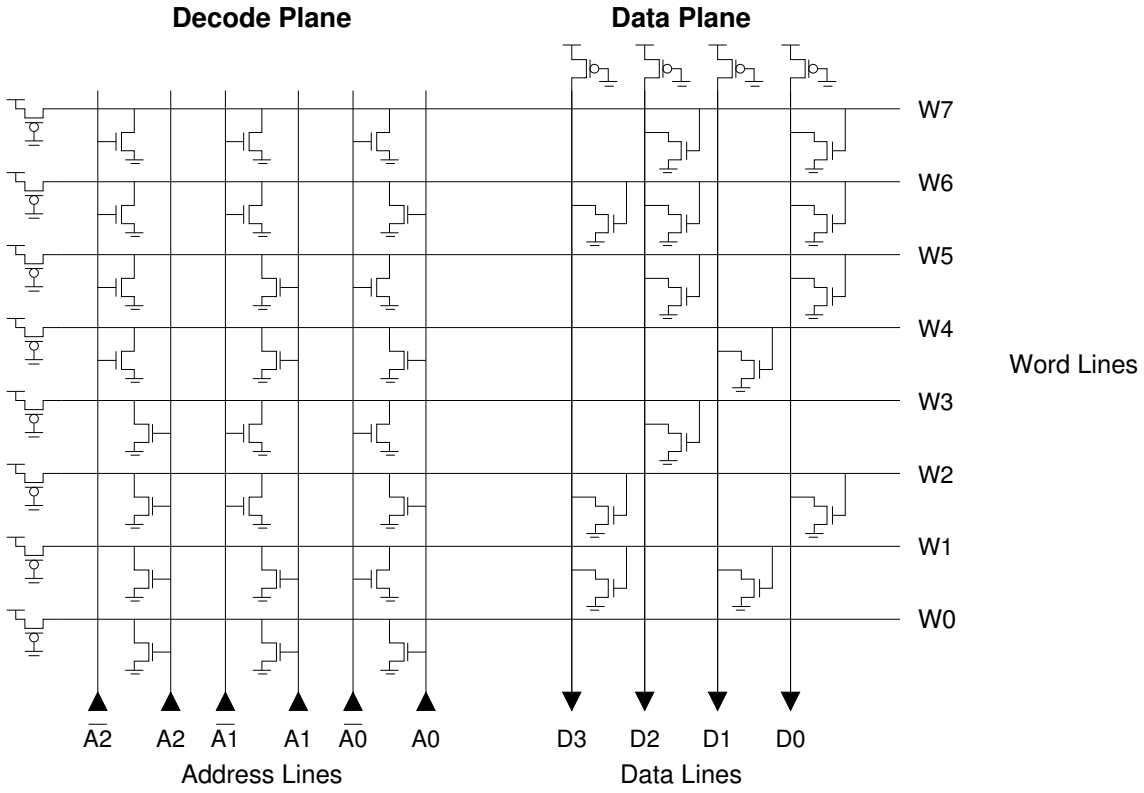
- A ROM may simply be a PLA with fixed decode plane[1]



[1]RAM structures can make use of the same decode plane.

ROMs

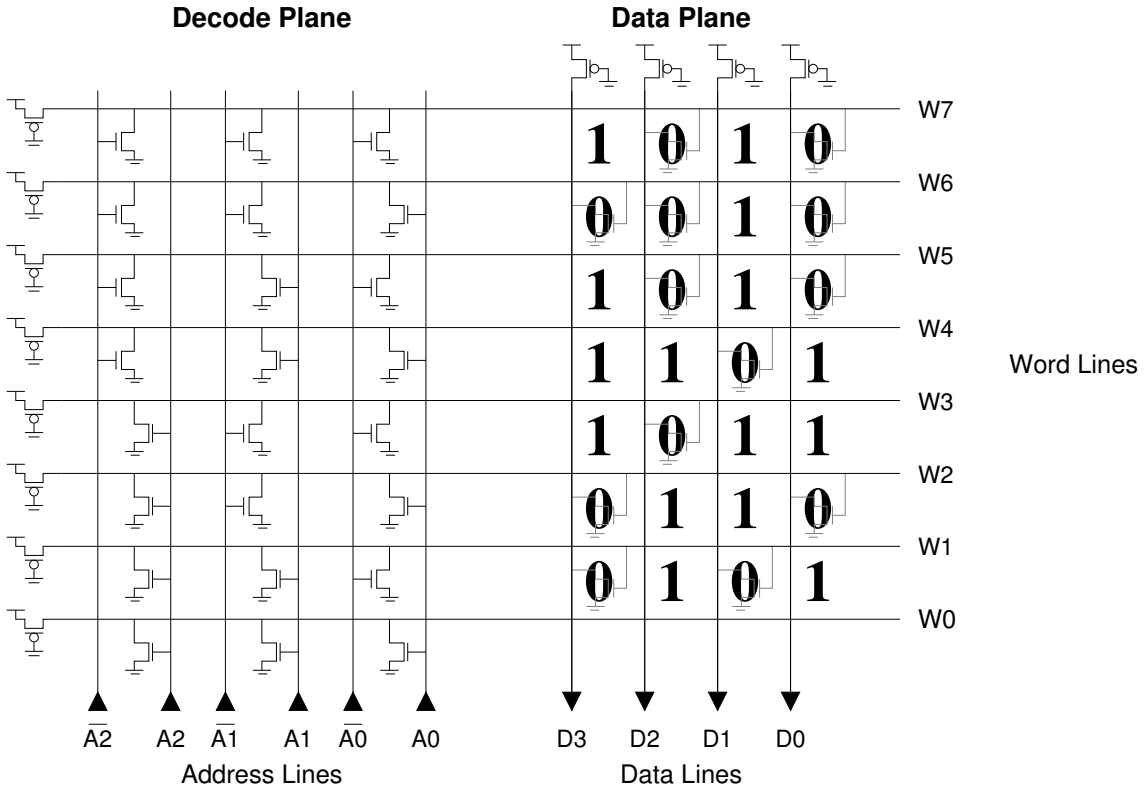
- A ROM may simply be a PLA with fixed decode plane[1] and programmable data plane.



[1]RAM structures can make use of the same decode plane.

ROMs

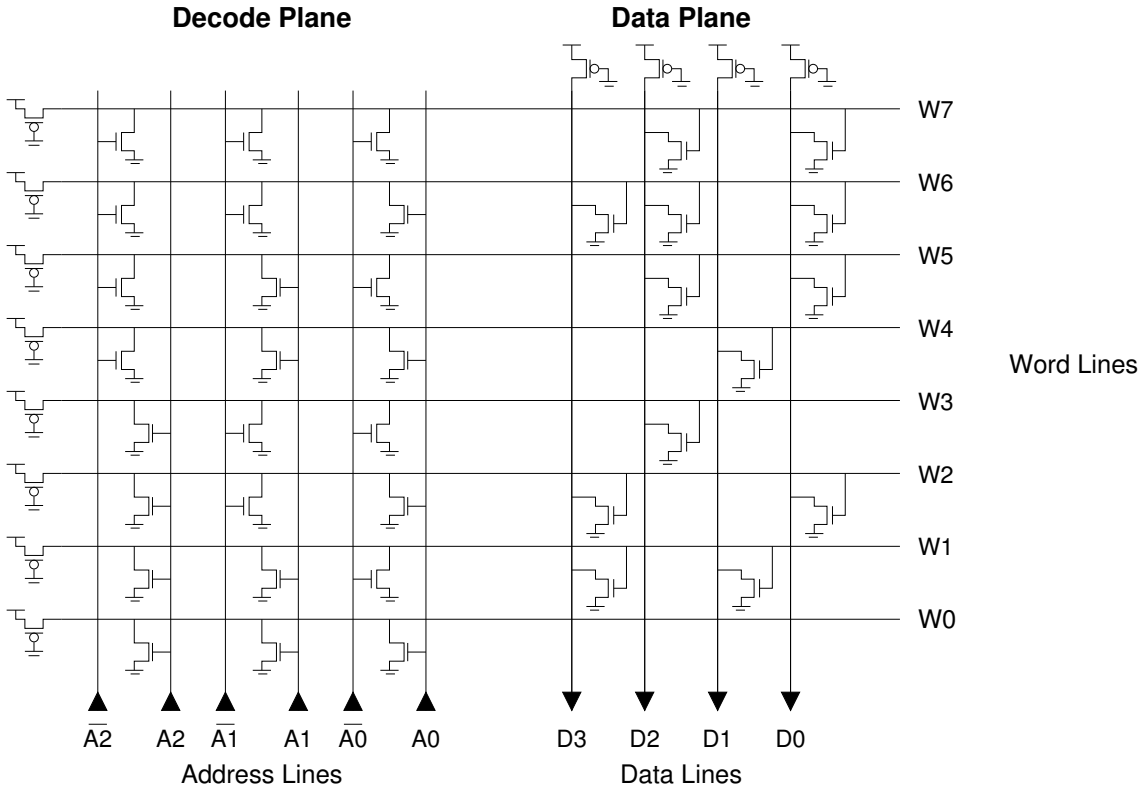
- A ROM may simply be a PLA with fixed decode plane[1] and programmable data plane.



[1]RAM structures can make use of the same decode plane.

ROMs

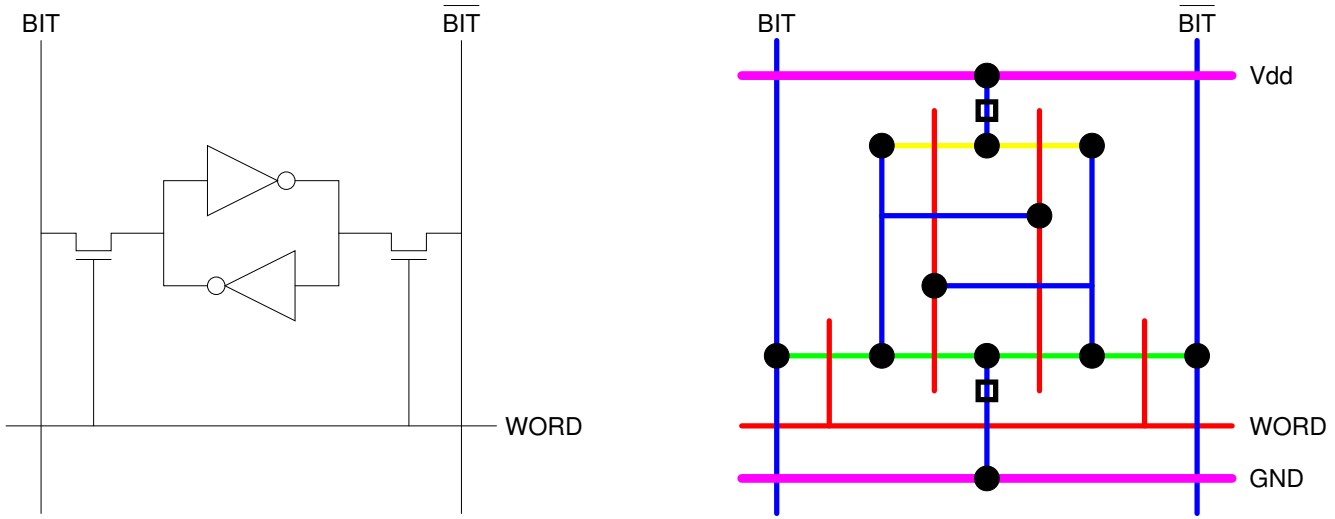
- A ROM may simply be a PLA with fixed decode plane[1] and programmable data plane.



[1]RAM structures can make use of the same decode plane.

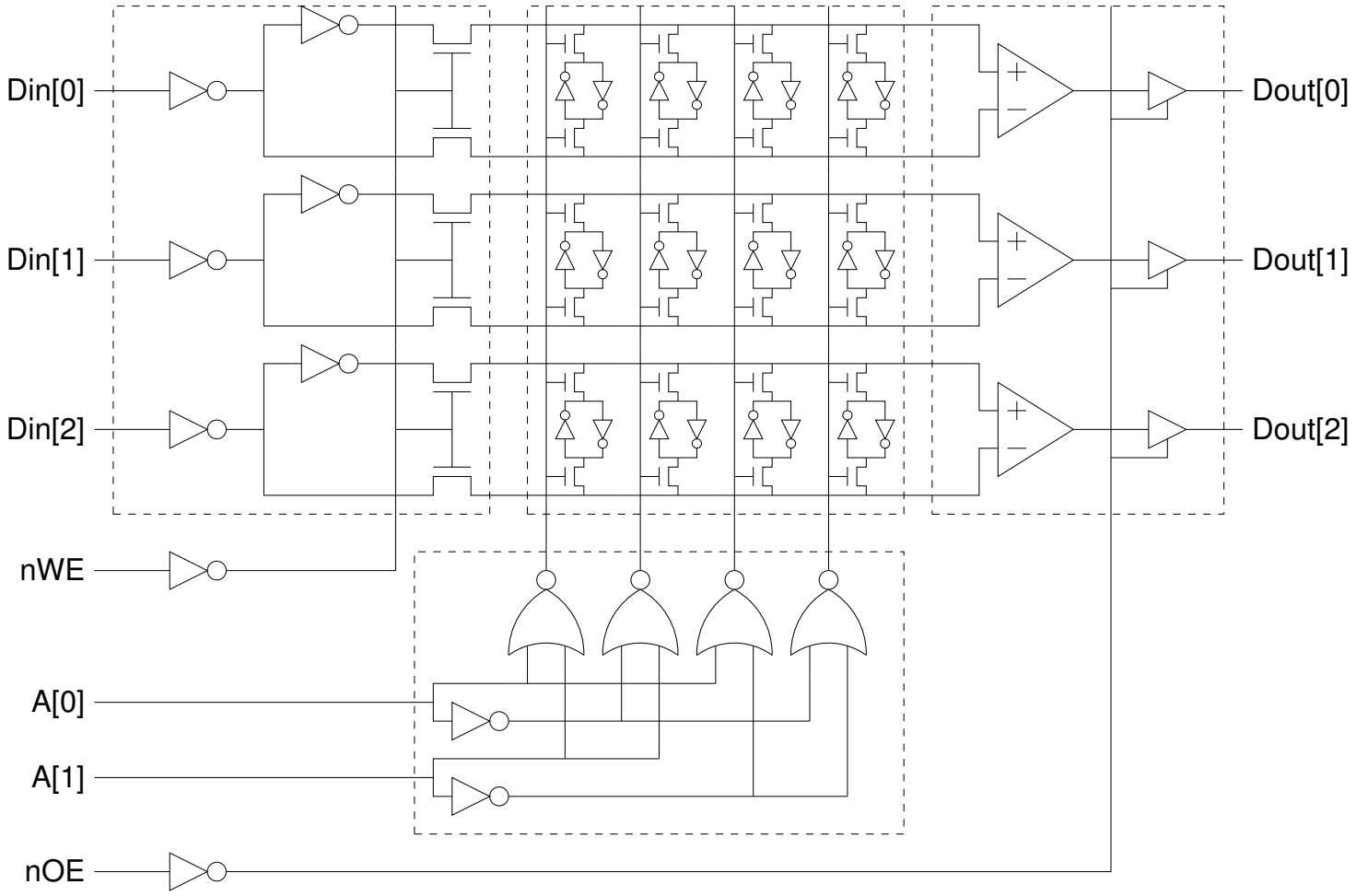
Static RAM

- Used for high density storage on a standard CMOS process.
- Short lived conflict during write - NMOS transistors offer stronger path.
- Differential amplifiers are used for speedy read.

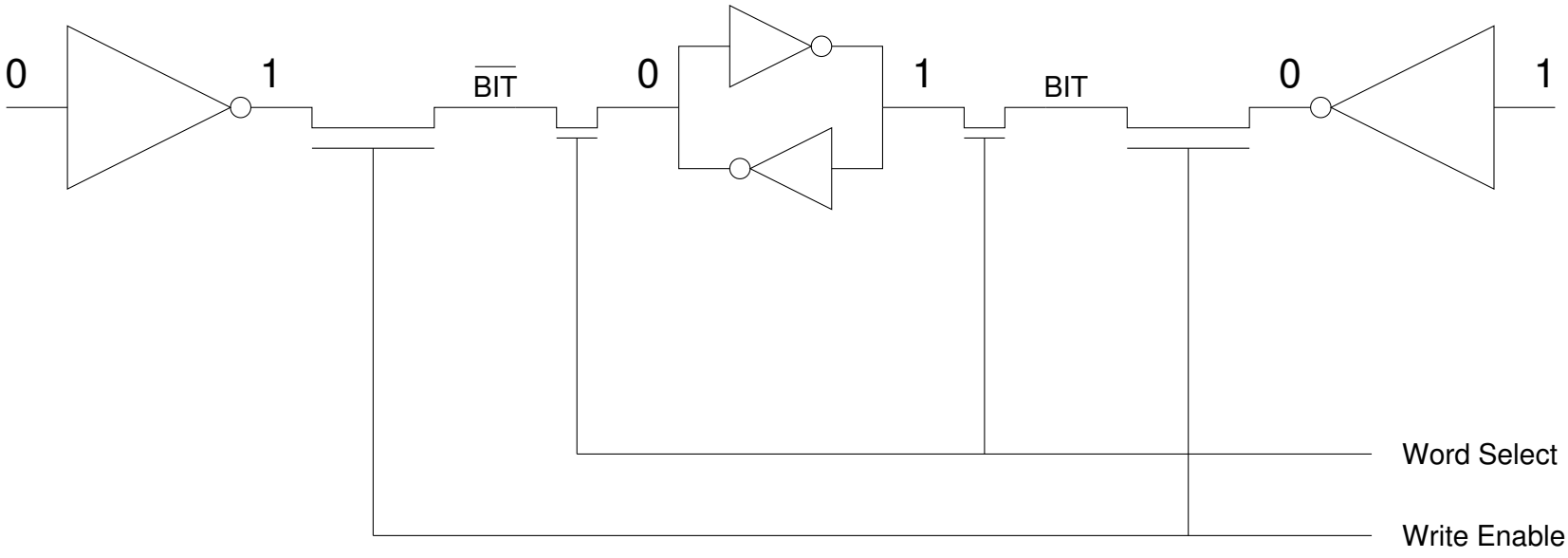


Standard 6 transistor static RAM cell.

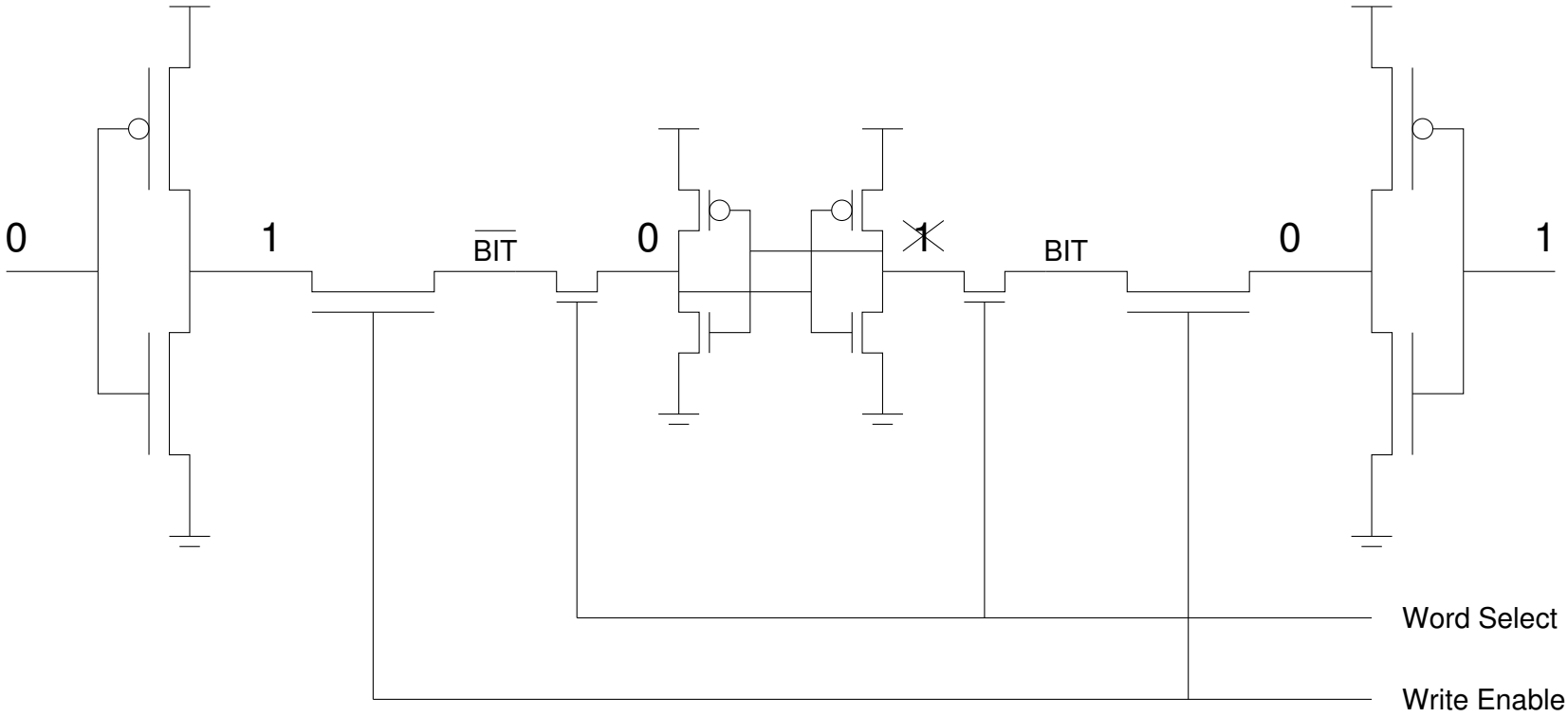
SRAM Structure



SRAM Write

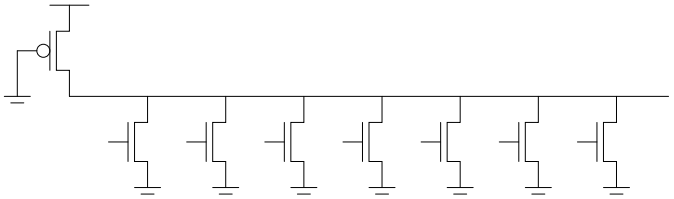


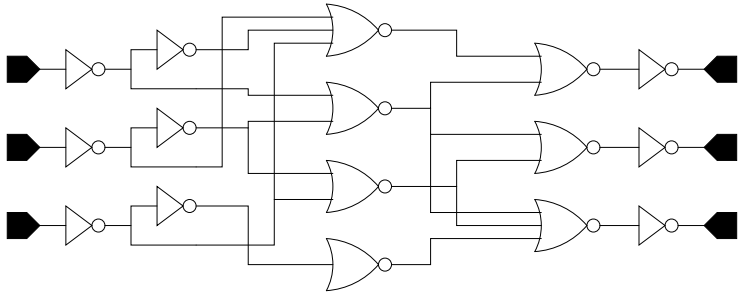
SRAM Write

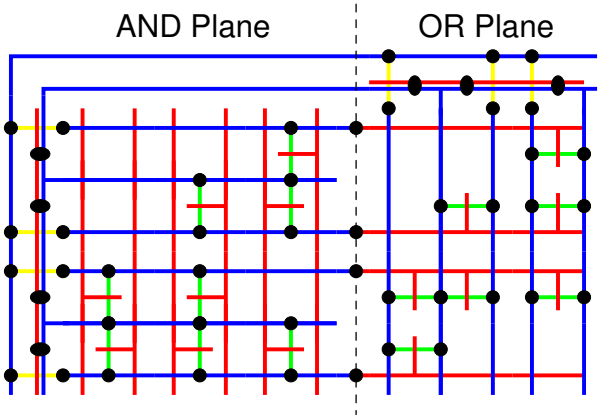


10010

PLA and ROM





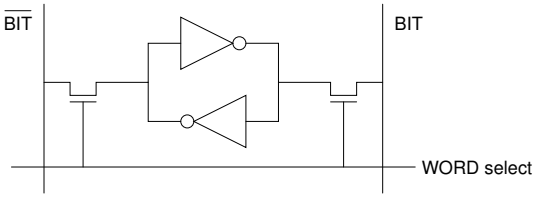


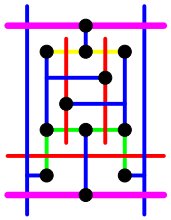
ROM is PLA with

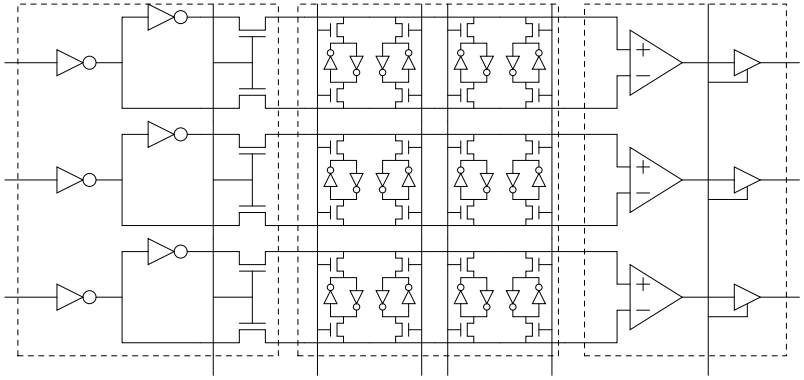
fixed AND (decoder) plane

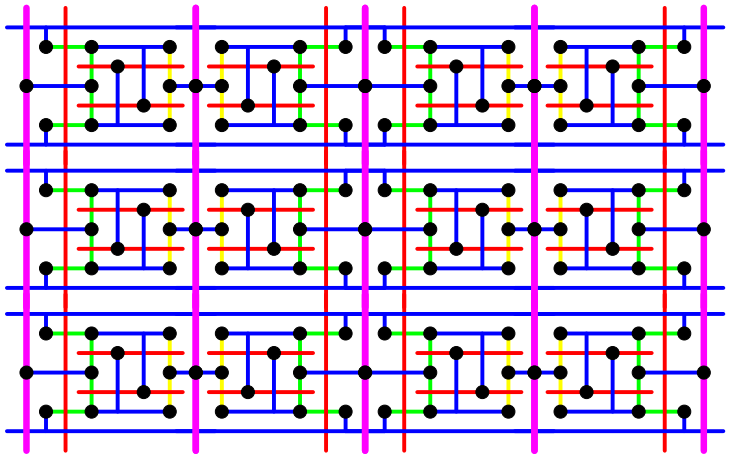
programmable OR (data) plane

SRAM









Cells are designed to butt together in two dimensions leading to efficient layout

PLA layout efficiency will depend on the actual function implemented (e.g. number of common product terms)