

System Design Choices

- Programmable Logic
 - PLD
 - e.g. Lattice ispGAL22V10, Atmel ATF1502 CPLD
 - Field Programmable Gate Array (FPGA)
 - e.g. Intel Cyclone V, Xilinx Artix-7/Zync-7000
- Semi-Custom Design
 - Mask Programmable Gate Array
 - e.g. ECS CMOS Gate Array
 - Intel HardCopy II structured ASICs
 - Standard Cell Design
 - e.g. AMS CORELIB 0.35 μ m cell library
- Full Custom Design

System Design Choices

- Programmable Logic

START HERE

- Best possible design turnaround time
- Cheapest for prototyping
- Best time to market
- Minimum skill required

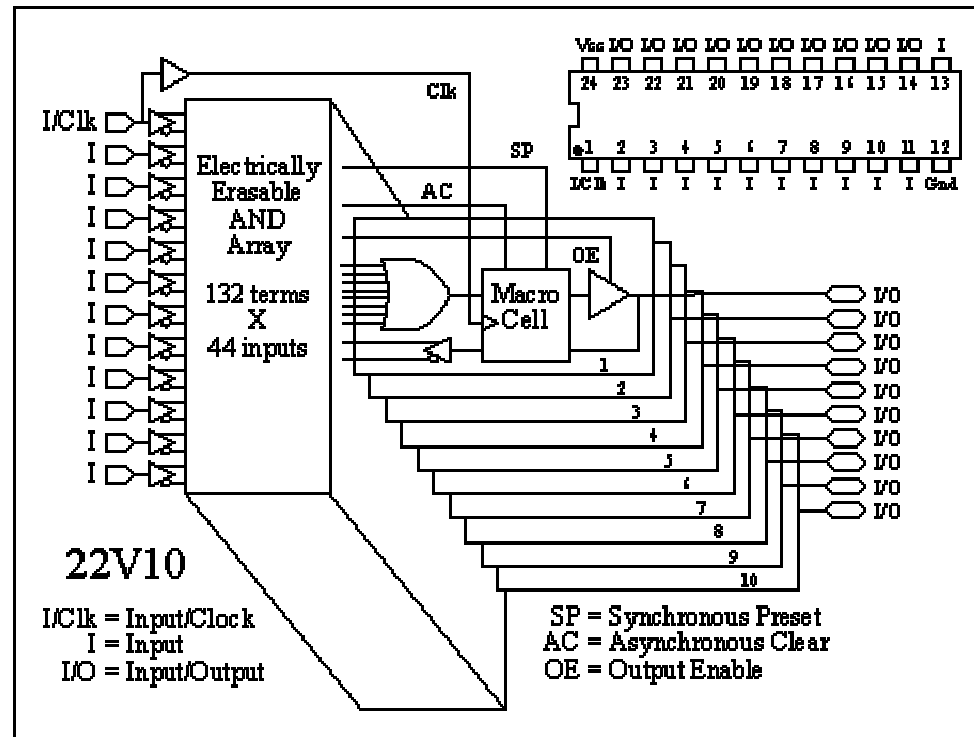
- Semi-Custom Design

- Full Custom Design

- Cheapest for mass production
- Fastest
- Lowest Power
- Highest Density¹
- Most skill required

¹optimization limited by speed/power/area trade off

Programmable Logic

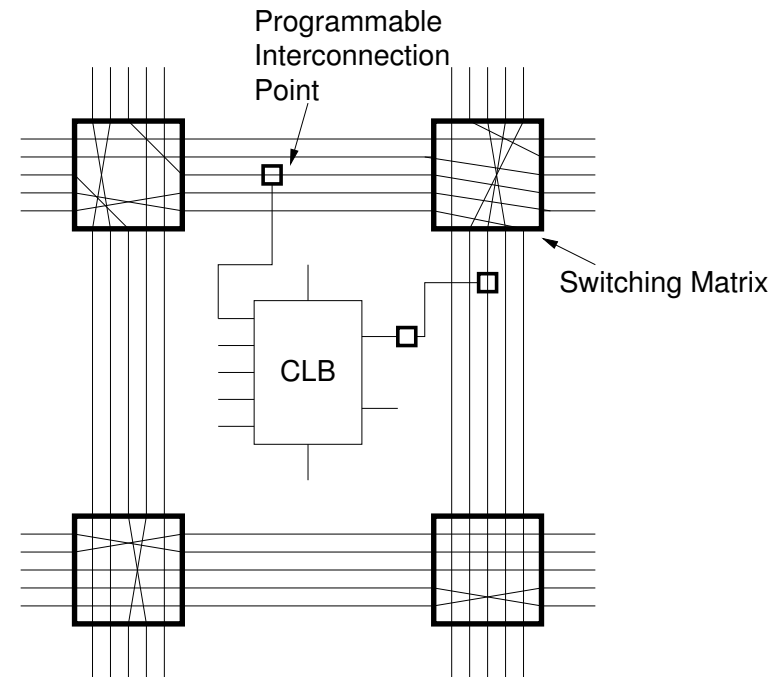
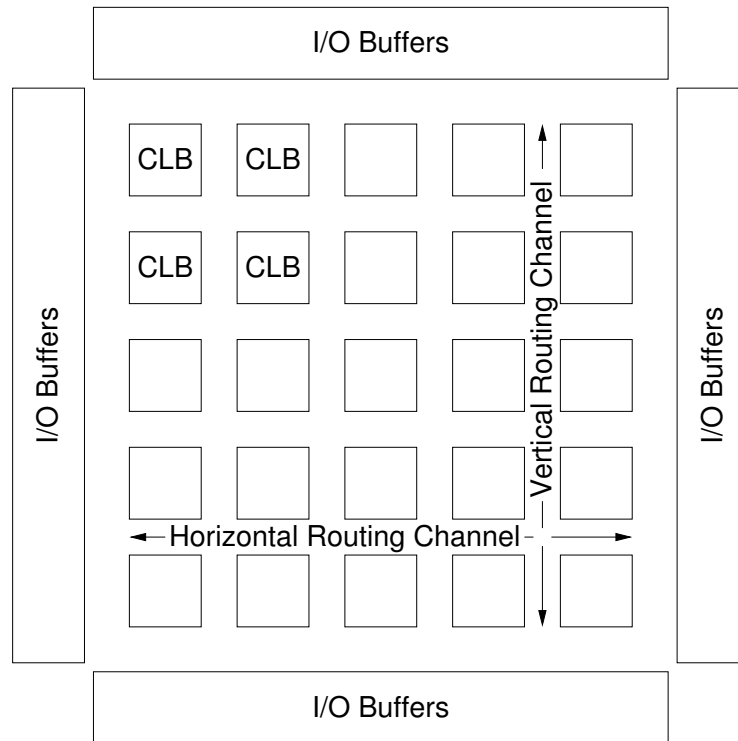


ICT PEEL22CV10

Source: ICT

- One time use - Fuse programmable.
- Reprogrammable - UV/Electrically Erasable.

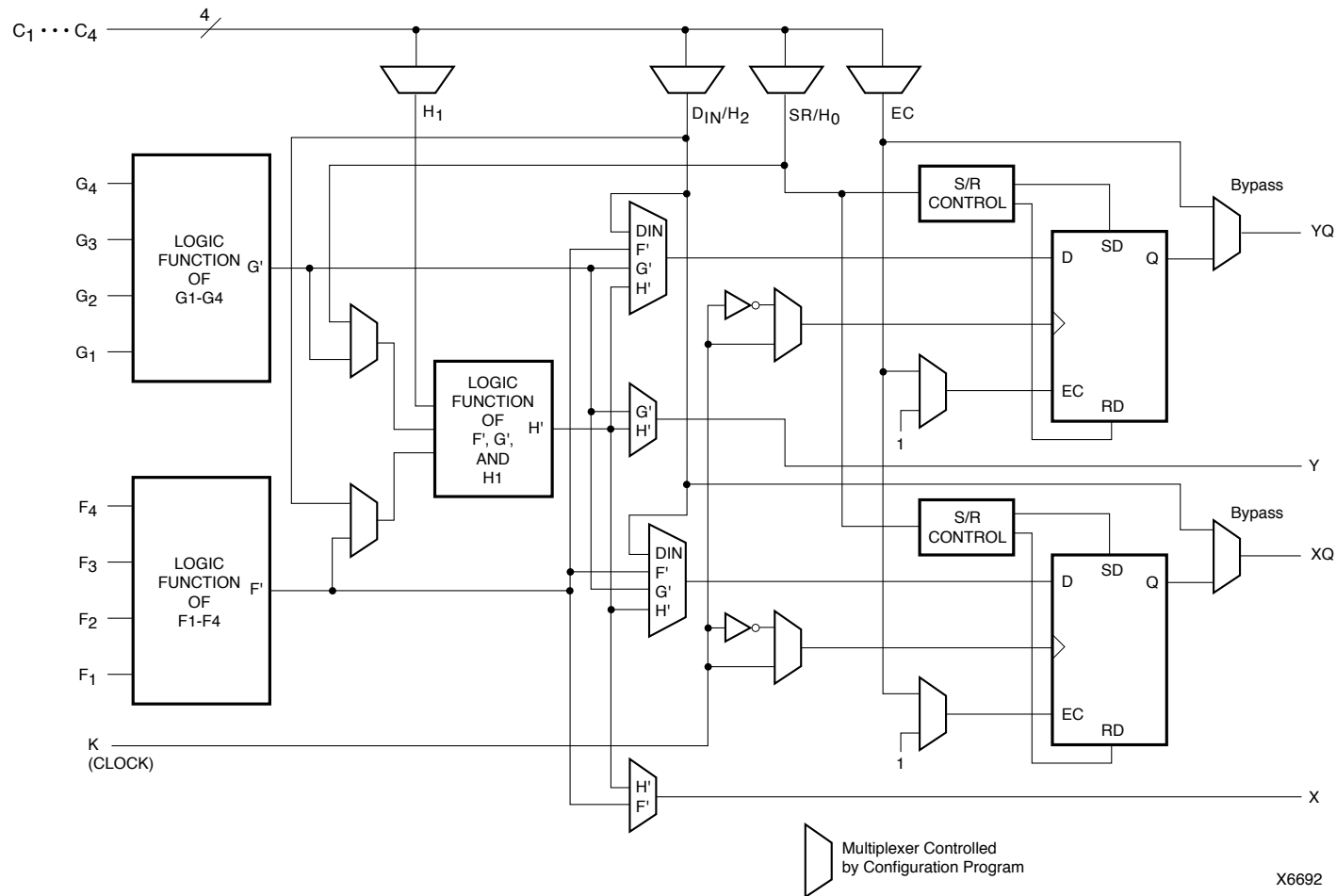
Field Programmable Gate Array – Xilinx XC4000



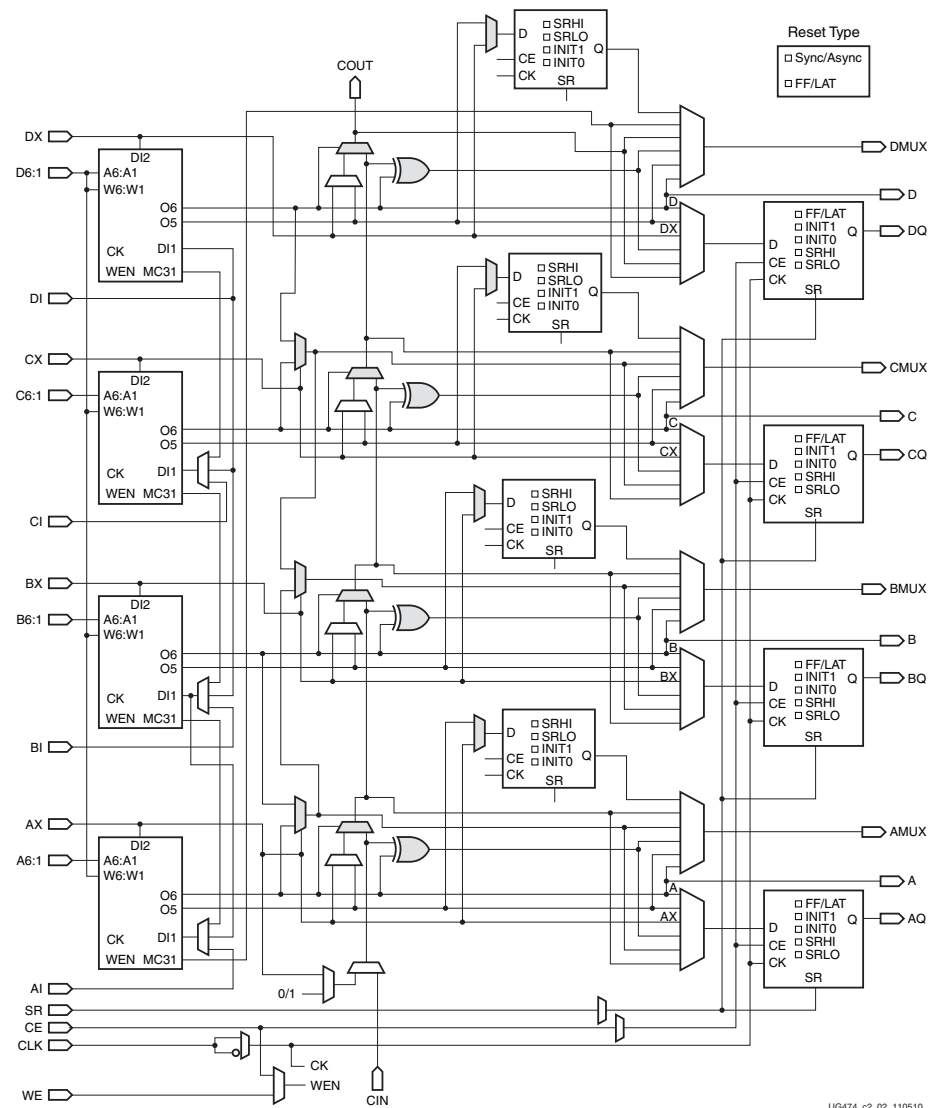
- Configurable Logic Blocks (CLBs) & I/O Blocks²
- Programmable Interconnect

²Xilinx XC4013 has 576 (24×24) CLBs and up to 192 (4×48) user I/O pins.

Field Programmable Gate Array – Xilinx XC4000 CLB



Source: Xilinx

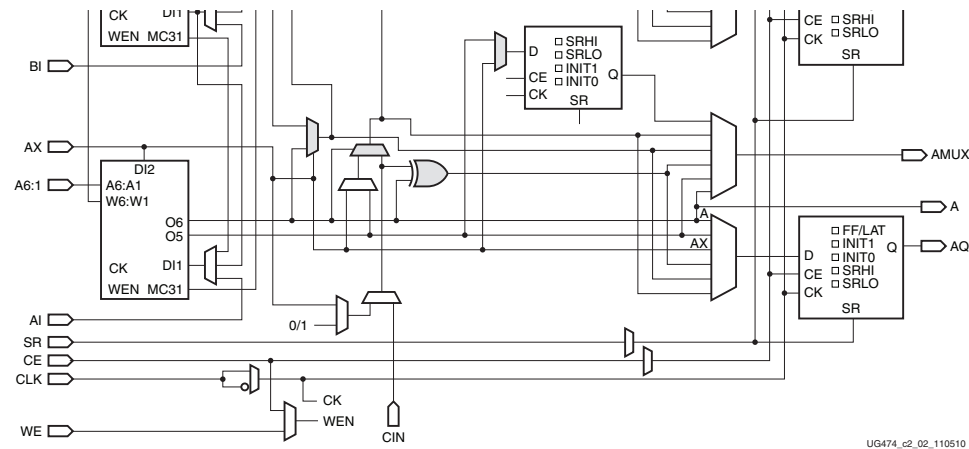


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Artix-7 – SLICEM CLB

Source: Xilinx

Xilinx Artix-7 – SLICEM_{CLB}³



Source: Xilinx

- 4x 6-input Look-Up Tables (LUTs) for combinational logic
- Carry chain supporting fast carry lookahead
- 8x storage elements

LUTs can be alternatively configured as

- 256 bits RAM
- 32-bit shift register

³Xilinx XC7A200T has 16,825 CLBs (each containing 2 slices) and up to 500 user I/O pins.

FPGA - System On Chip

Modern FPGAs are big enough for:

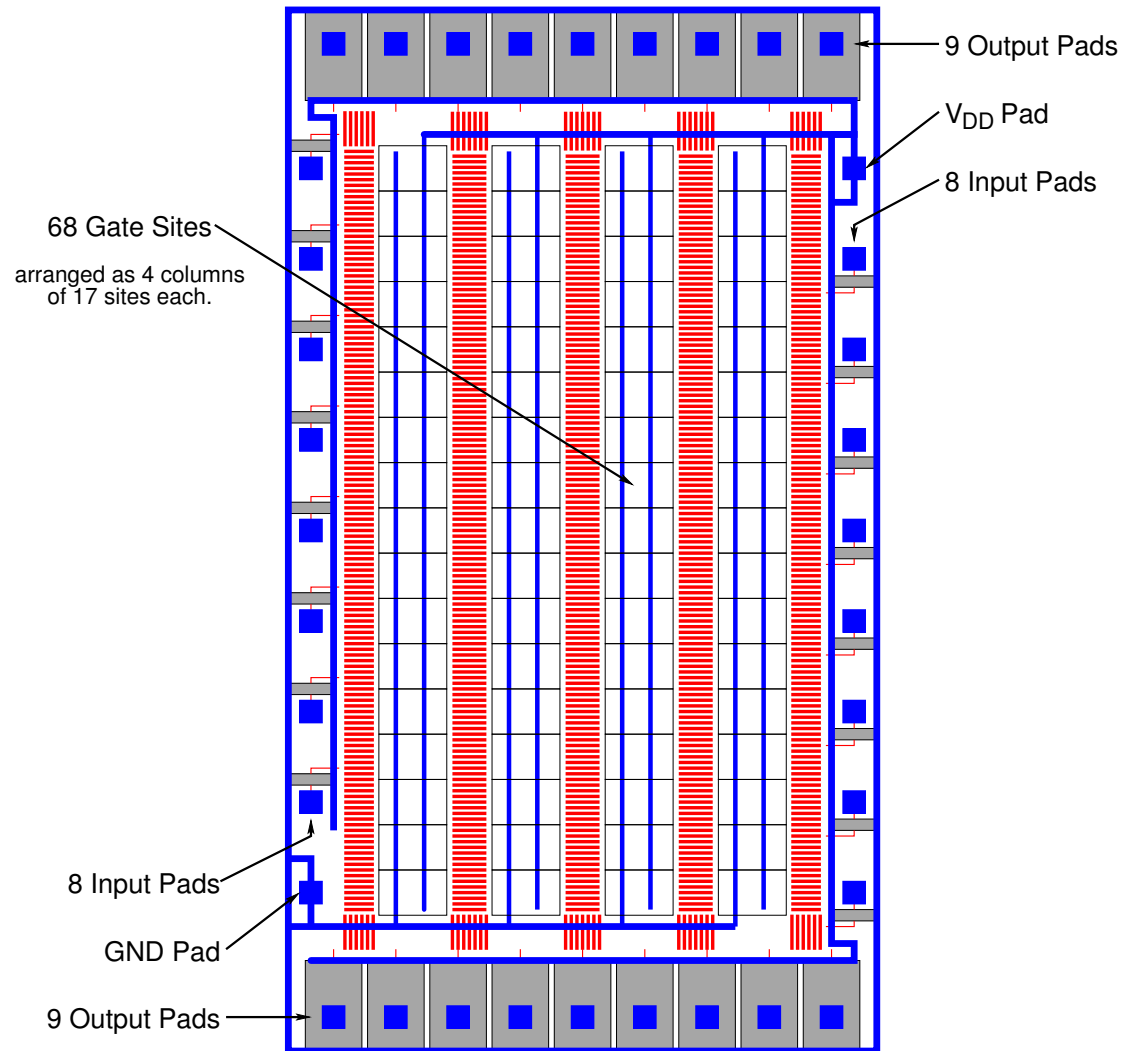
- One or more soft-core processors
- Program memory
- Data memory
- + specialist hardware

The new trend is for FPGAs with hard processors built in:

- Xilinx Zync-7000 includes dual-core ARM A9
- Intel Cyclone V SE includes dual-core ARM A9
- Cypress PSoC 4 includes ARM Cortex-M0 and programmable digital⁴ and analog blocks

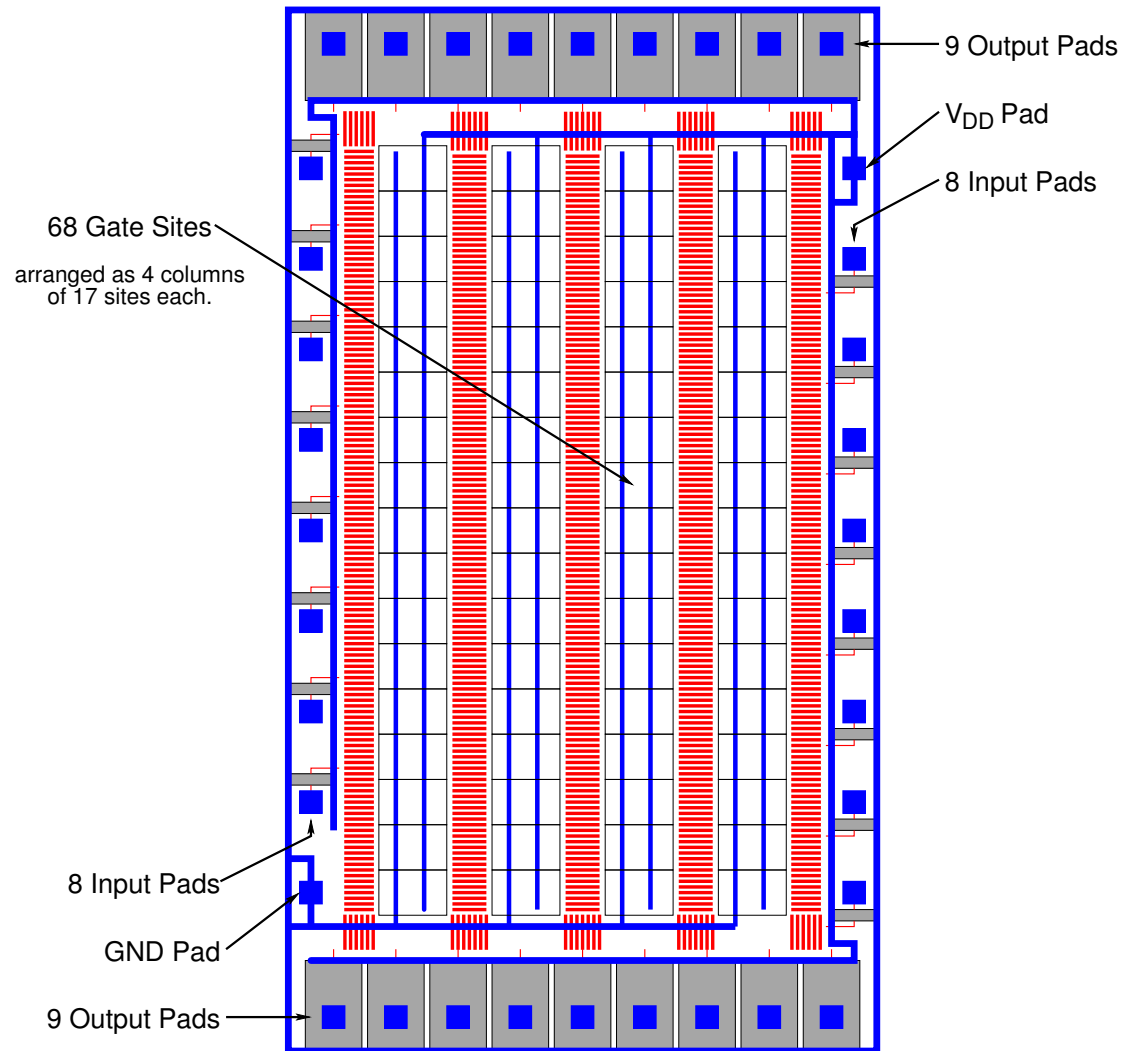
⁴here the digital block is PLD rather than FPGA

Mask Programmable Gate Array



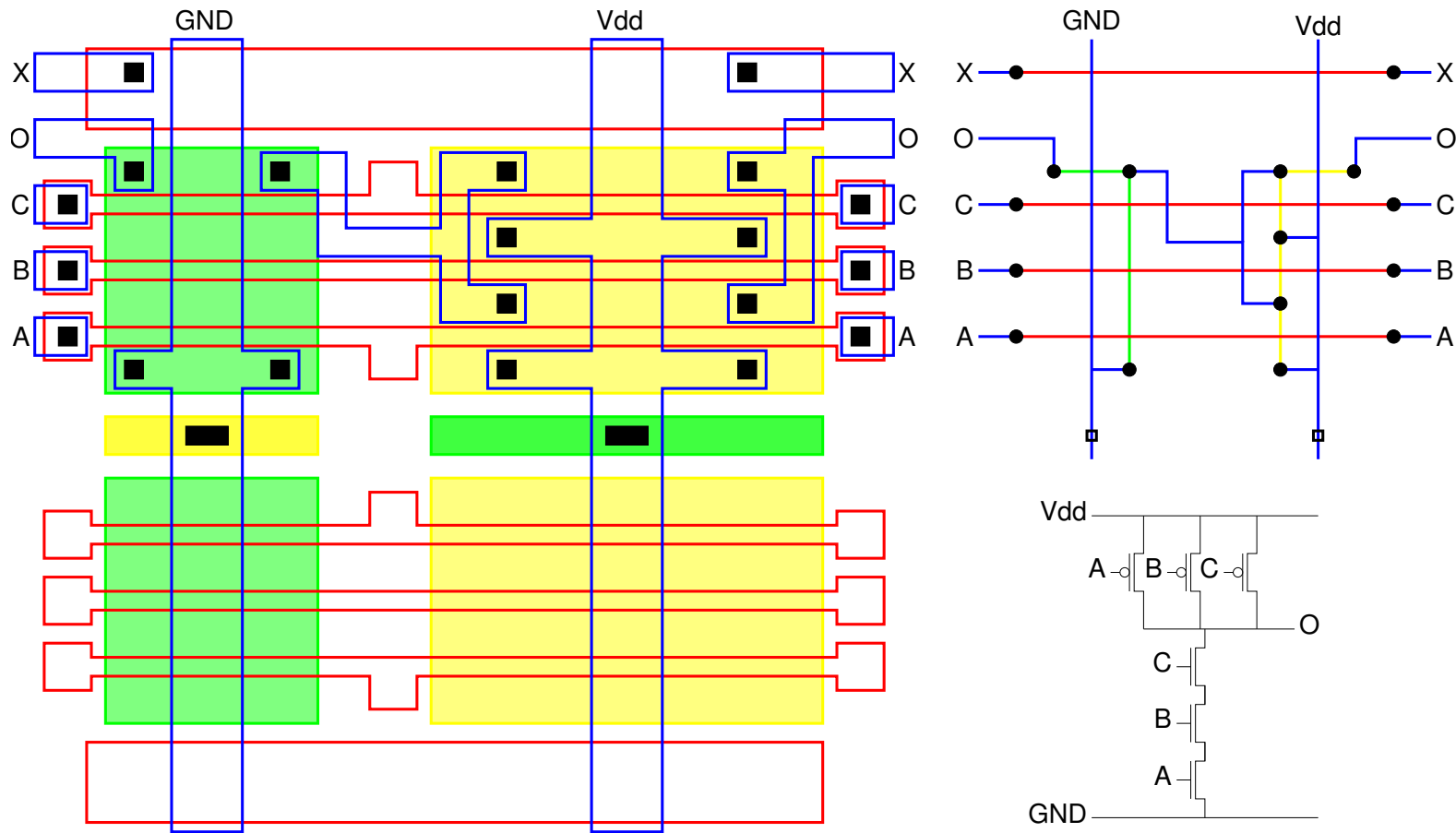
11009

ECS CMOS Gate Array – Designed by Iain McNally (c. 1995)



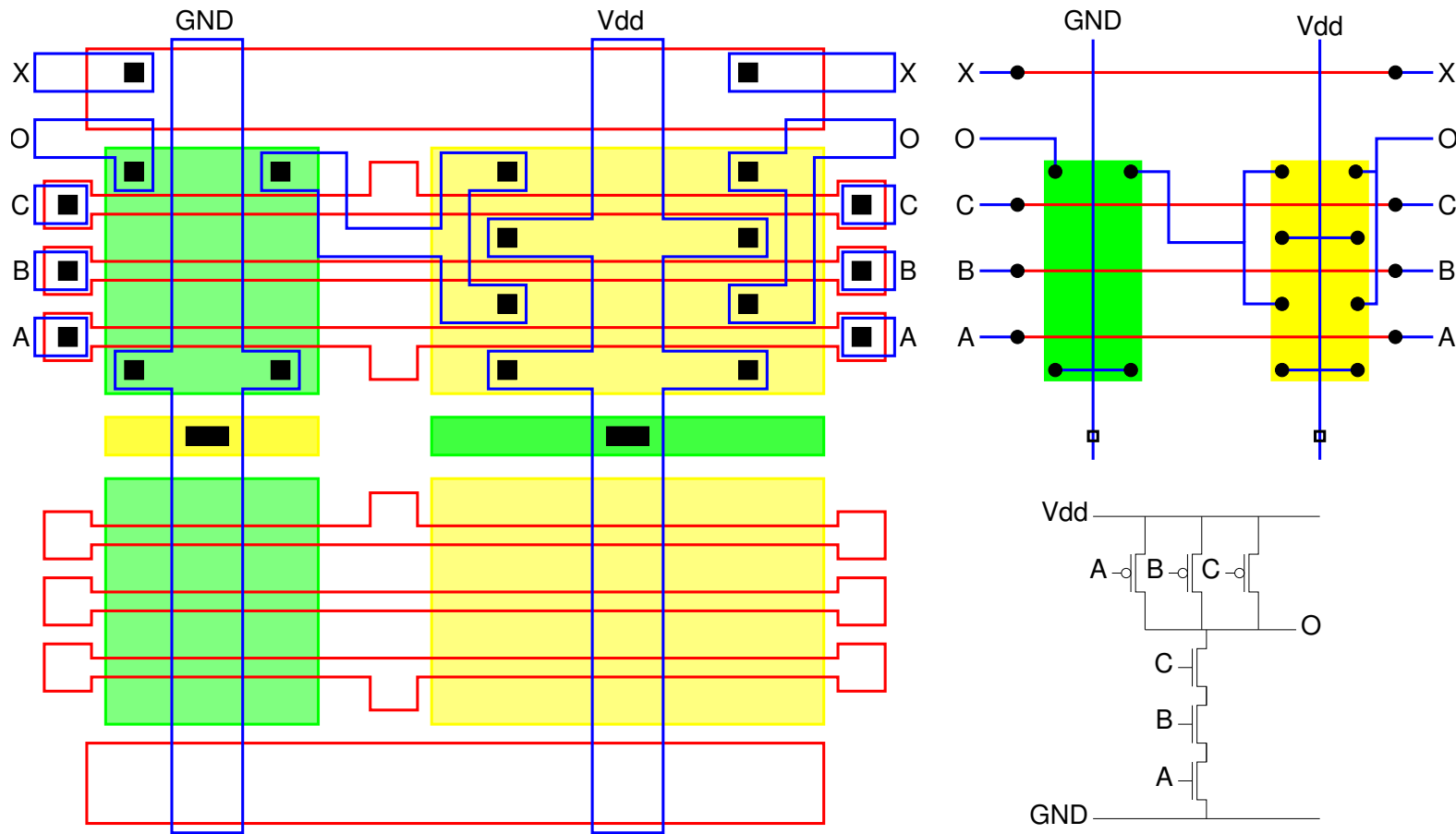
11009

Mask Programmable Gate Array



- Customize Metal and Contact Window masks only.

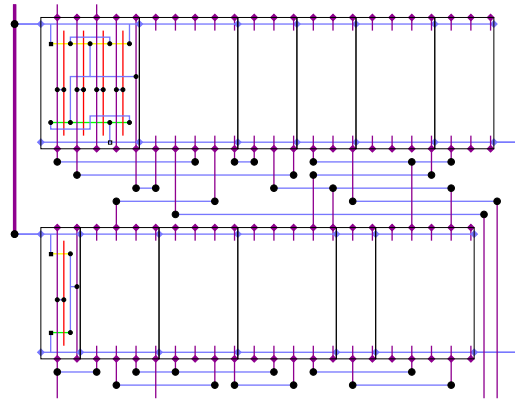
Mask Programmable Gate Array



- Stick diagrams cannot always show the full picture.

Standard Cell Design

- Logic Functions



- Auto Generated Macro Blocks

- PLA
- ROM
- RAM

- System Level Blocks

- Microprocessor core⁵

⁵Will support System On Chip applications.

Full Custom

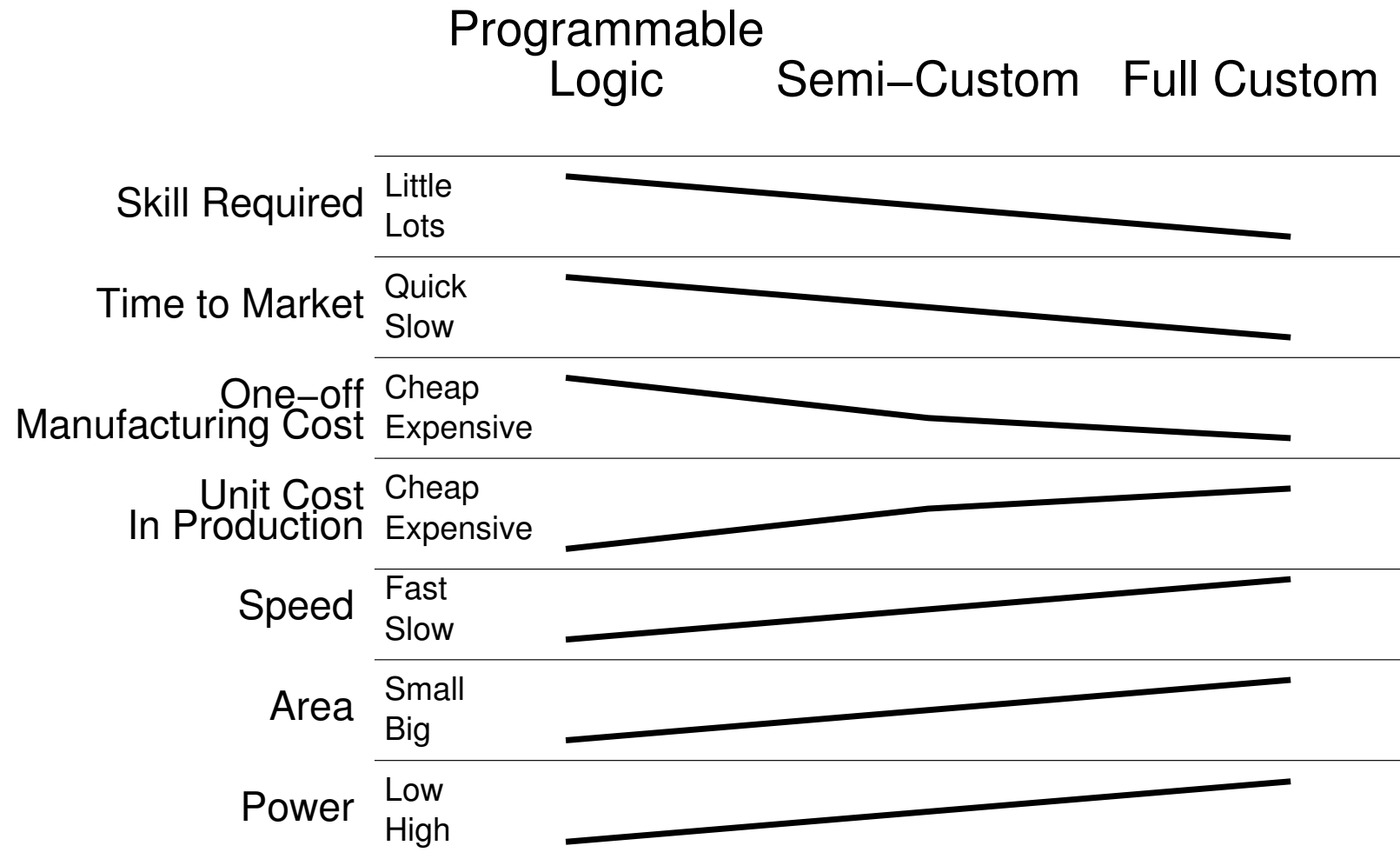
All design styles need full custom designers

- to design the base programmable logic chips
- to design building blocks for semi-custom

Where large ASICs use full custom techniques they are likely to be used alongside semi-custom techniques.

e.g. Hand-held computer game chip

- Full custom bitslice datapath
hand crafted for optimum area efficiency and low power consumption
- Standard cell controller
- Macro block RAM, ROM



All design styles need full custom designers

A large ASIC (especially SoC) may mix Semi-Custom and Full Custom