# Synchronous Systems



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- The data may change between active clock transitions but must be stable by the time the next active transition occurs<sup>1</sup>.

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- Valid data should be present on D input for at least  $t_{setup}$  before the active clock edge and at least  $t_{hold}$  after the clock edge.
- The minimum D-type cycle time will be limited by the sum  $t_{setup} + t_{pQ}$ .



• To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup}$$

• To avoid a hold violation:

$$t_{pQ} + t_{comb} > t_{hold}$$

# Static Timing Analysis

- Predicts the timing of a circuit without simulation<sup>2</sup>
- Analysis of gate network based on:
  - Propagation delays
  - Set-up and hold times for storage elements
  - Constraints such as desired operating freqency and the timing of inputs and outputs

Note that the examples given here are simplified in that they reduce the propagation delay through a gate to a single number - in reality there are predictable and unpredicatble variations in gate delays which must be accounted for by static timing analysis tools.

<sup>&</sup>lt;sup>2</sup>timing simulations for large digital systems are slow and will usually not catch all edge and coner cases



• To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup}$$

• To avoid a hold violation:

$$t_{pQ} + t_{comb-min} > t_{hold}$$



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• Critcal path analysis allows us to determine the maximum feasible clock frequency:

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup}$$
$$f_{max} = \frac{1}{t_{pQ} + t_{comb-max} + t_{setup}}$$
$$20006$$



 $t_{pQ} + t_{comb-min} > t_{hold}$ 

If we have an ideal clock and  $t_{pQ} > t_{hold}$  we won't see hold violations even with if  $t_{comb-min} = 0$ .



• Clock Distribution

The process of distributing clocks from a central source gives rise to delays.

**Clock skew** is the difference between the arrival times of the clock at different points in the circuit.

• Clock Skew may cause unexpected timing violations

**Hold:** if *D-type* #1 clocks first, D input of *D-type* #2 may change too early<sup>3</sup> **Setup:** if *D-type* #1 clocks second, D input of *D-type* #2 may change too late

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<sup>&</sup>lt;sup>3</sup>most likely where combinational logic is minimal or absent



• To avoid a setup violation:

$$ClockPeriod + t_{d2} > t_{pQ} + t_{comb} + t_{setup} + t_{d1}$$

• To avoid a hold violation:

$$t_{pQ} + t_{comb} + t_{d1} > t_{hold} + t_{d2}$$



• To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup} + (t_{d1} - t_{d2})$$

• To avoid a hold violation:

$$t_{pQ} + t_{comb} > t_{hold} + (t_{d2} - t_{d1})$$



• What is the maximum operating frequency of the circuit if the clock skew is no more than 16ps?

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup} + t_{skew}$$

• What is the maximum clock skew that can be tolerated before we have a hold violation?

$$t_{pQ} + t_{comb} > t_{hold} + t_{skew}$$

#### Critical Path



• To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + t_{skew}$$

#### Critical Path



• To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d1} - t_{d4})$$



 $ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d1} - t_{d4})$ 

• If we can control the skew (e.g. by increasing  $t_{d4}$ ), we can ease the timing constraint.<sup>4</sup>

<sup>&</sup>lt;sup>4</sup>this may result in the critical path moving to another part of the circuit



 $ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$ 

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• Calculate  $f_{max}$  in the presence of intentional clock skew.



- Calculate  $f_{max}$  in the presence of intentional clock skew.
- Suggest suitable values for  $t_{d1}$ ,  $t_{d2}$ ,  $t_{d3}$ ,  $t_{d4}$ ,  $t_{d5}$ ,  $t_{d6}$



- Calculate  $f_{max}$  in the presence of intentional clock skew.
- Suggest suitable values for  $t_{d1}$ ,  $t_{d2}$ ,  $t_{d3}$ ,  $t_{d4}$ ,  $t_{d5}$ ,  $t_{d6}$ Initially set all to a minimum value (in this case 50ps)



- Calculate  $f_{max}$  in the presence of intentional clock skew.
- Suggest suitable values for  $t_{d1}$ ,  $t_{d2}$ ,  $t_{d3}$ ,  $t_{d4}$ ,  $t_{d5}$ ,  $t_{d6}$
- $\Rightarrow$  Identify longest timing paths



- Calculate  $f_{max}$  in the presence of intentional clock skew.
- Suggest suitable values for  $t_{d1}$ ,  $t_{d2}$ ,  $t_{d3}$ ,  $t_{d4}$ ,  $t_{d5}$ ,  $t_{d6}$
- $\Rightarrow$  Identify longest timing paths

$$t_{path-A} = t_{pQ} + t_{comb-A} + t_{setup} + (t_{d1} - t_{d4})$$



- Calculate  $f_{max}$  in the presence of intentional clock skew.
- Suggest suitable values for  $t_{d1}$ ,  $t_{d2}$ ,  $t_{d3}$ ,  $t_{d4}$ ,  $t_{d5}$ ,  $t_{d6}$
- $\Rightarrow$  Identify longest timing paths

$$t_{path-B} = t_{pQ} + t_{comb-B} + t_{setup} + (t_{d2} - t_{d4})$$



- Calculate  $f_{max}$  in the presence of intentional clock skew.
- Suggest suitable values for  $t_{d1}$ ,  $t_{d2}$ ,  $t_{d3}$ ,  $t_{d4}$ ,  $t_{d5}$ ,  $t_{d6}$
- $\Rightarrow$  Identify longest timing paths

$$t_{path-C} = t_{pQ} + t_{comb-C} + t_{setup} + (t_{d4} - t_{d6})$$



- Calculate  $f_{max}$  in the presence of intentional clock skew.
- Suggest suitable values for  $t_{d1}$ ,  $t_{d2}$ ,  $t_{d3}$ ,  $t_{d4}$ ,  $t_{d5}$ ,  $t_{d6}$
- $\Rightarrow$  Identify longest timing paths

$$t_{path-D} = t_{pQ} + t_{comb-D} + t_{setup} + (t_{d5} - t_{d6})$$



- Calculate  $f_{max}$  in the presence of intentional clock skew.
- Suggest suitable values for  $t_{d1}$ ,  $t_{d2}$ ,  $t_{d3}$ ,  $t_{d4}$ ,  $t_{d5}$ ,  $t_{d6}$
- $\Rightarrow$  Identify longest timing paths

$$t_{path-E} = t_{pQ} + t_{comb-E} + t_{setup} + (t_{d4} - t_{d1})$$



- Calculate  $f_{max}$  in the presence of intentional clock skew.
- Suggest suitable values for  $t_{d1}$ ,  $t_{d2}$ ,  $t_{d3}$ ,  $t_{d4}$ ,  $t_{d5}$ ,  $t_{d6}$
- $\Rightarrow$  Identify longest timing paths

$$t_{path} = t_{pQ} + t_{comb} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$



 $ClockPeriod > t_{pQ} + t_{comb-A} + t_{setup} + (t_{d1} - t_{d4})$ 

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-A} + t_{setup} + (t_{d1} - t_{d4})}$$



$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})}$$



 $\Rightarrow$  Initially try increasing  $t_{d4}$  by 20ps



$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})}$$



$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})}$$



- Calculate  $f_{max}$  in the presence of intentional clock skew.
- Suggest suitable values for *t*<sub>d1</sub>, *t*<sub>d2</sub>, *t*<sub>d3</sub>, *t*<sub>d4</sub> given that the minimum delay through the clock tree is 50ps

remember to check for hold violations

# Synchronous Systems - Jitter



• Jitter

Jitter is the cycle-by-cycle variation in the arrival time of the clock.

- Caused by
  - Variation in frequency/phase of clock source<sup>5</sup>
  - Power supply noise affecting clock distribution
  - Cross-talk affecting clock distribution
- Jitter may cause unexpected timing violations

<sup>&</sup>lt;sup>5</sup>primary clock source or Phase-Locked Loop (PLL)



• To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup} + (t_{d1} - t_{d2}) + 2 \times t_{jitter}$$

• To avoid a hold violation:

$$t_{pQ} + t_{comb} > t_{hold} + (t_{d2} - t_{d1}) + 2 \times t_{jitter}$$

## Synchronous Systems - Static Timing Analysis (skew + jitter)



• What is the maximum jitter that can be tolerated given an operating frequency of 6GHz and clock skew of no more than 16ps?<sup>6</sup>

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup} + t_{skew} + 2 \times t_{jitter}$$

$$t_{pQ} + t_{comb-min} > t_{hold} + t_{skew} + 2 \times t_{jitter}$$

<sup>&</sup>lt;sup>6</sup>remember to consider both setup and hold violations

#### Ideal Clock

• To avoid a setup violation:

 $ClockPeriod > t_{pQ} + t_{comb} + t_{setup}$ 

• To avoid a hold violation:

$$t_{pQ} + t_{comb} > t_{hold}$$

With Skew and Jitter

• To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup} + t_{skew} + 2 \times t_{jitter}$$

• To avoid a hold violation:

$$t_{pQ} + t_{comb} > t_{hold} + t_{skew} + 2 \times t_{jitter}$$