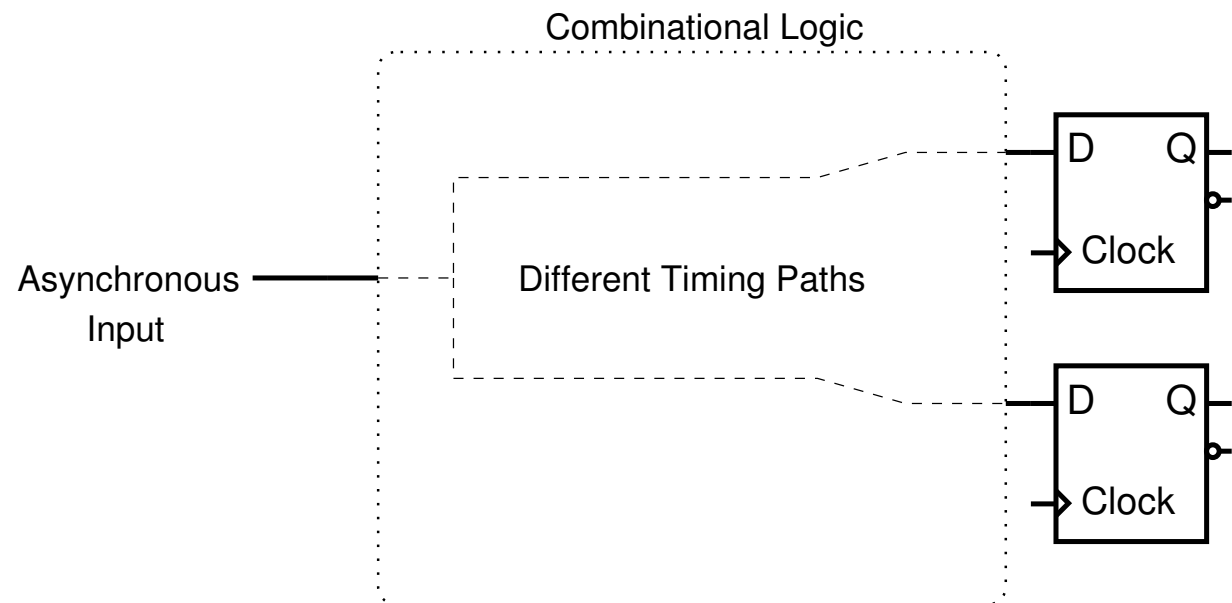


Synchronous Systems

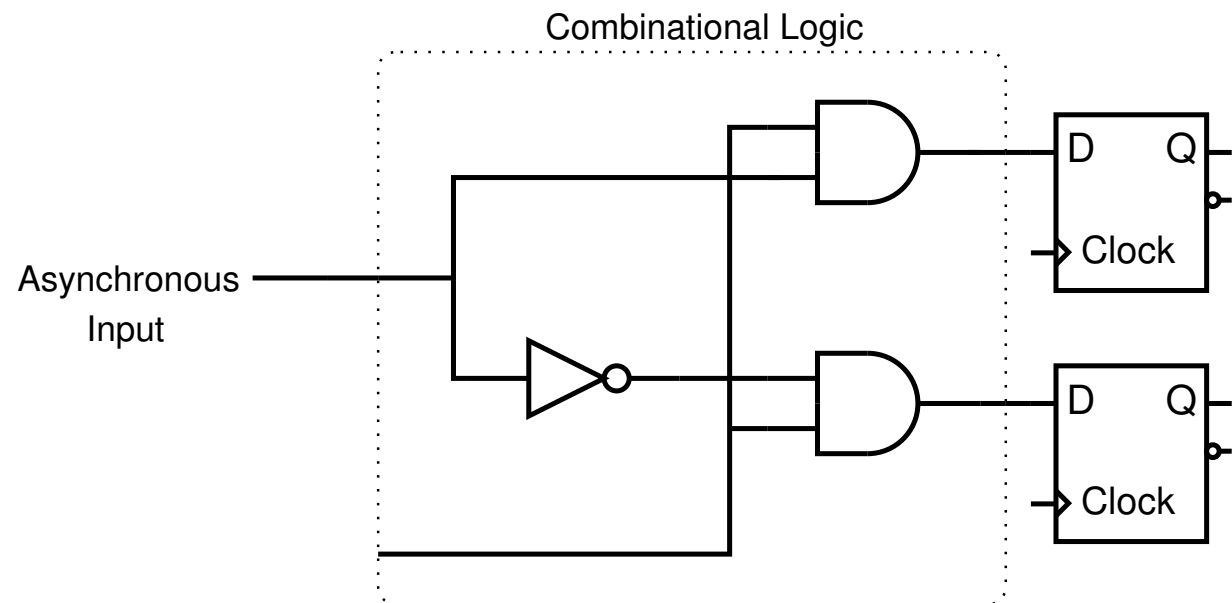
Asynchronous Inputs



With different timing paths through combinational logic, we can get unexpected results.

Synchronous Systems

Asynchronous Inputs

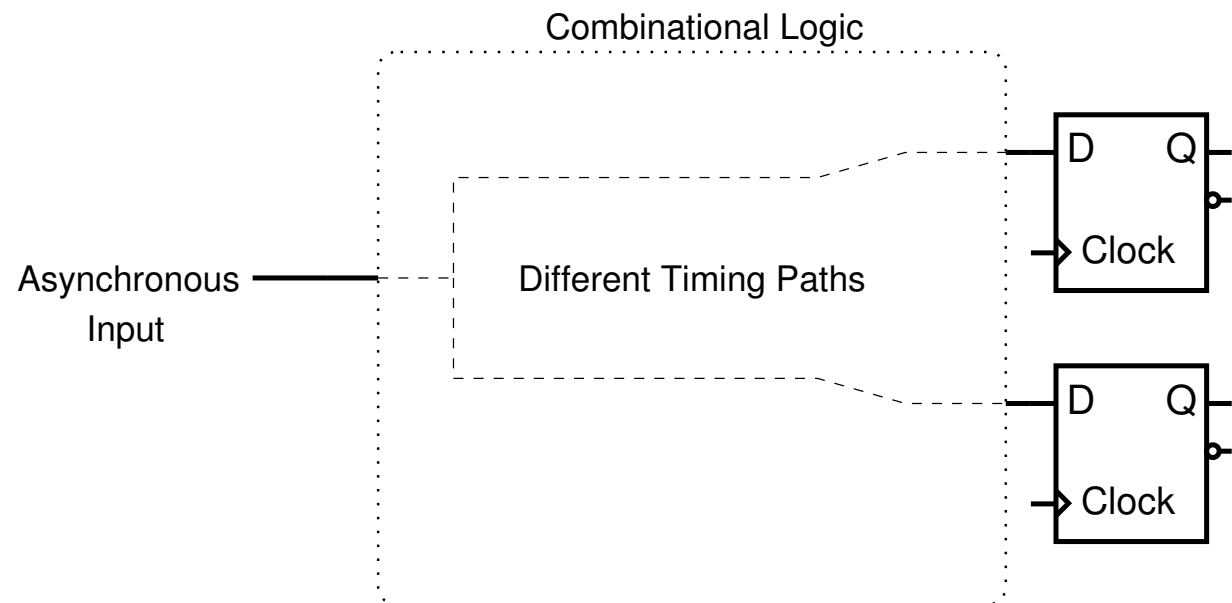


With different timing paths through combinational logic, we can get unexpected results.

In this example, a falling input we may be registered as neither high nor low.

Synchronous Systems

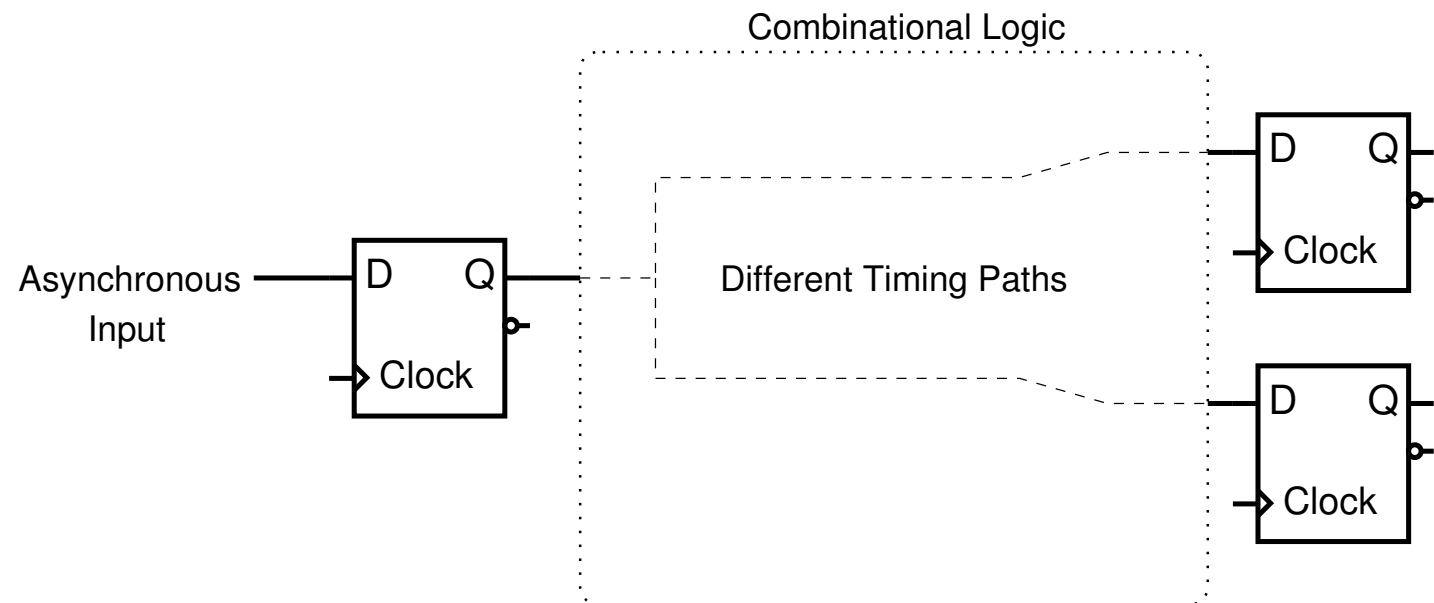
Asynchronous Inputs



Retiming the asynchronous input before the combinational logic block should give more predictable results.

Synchronous Systems

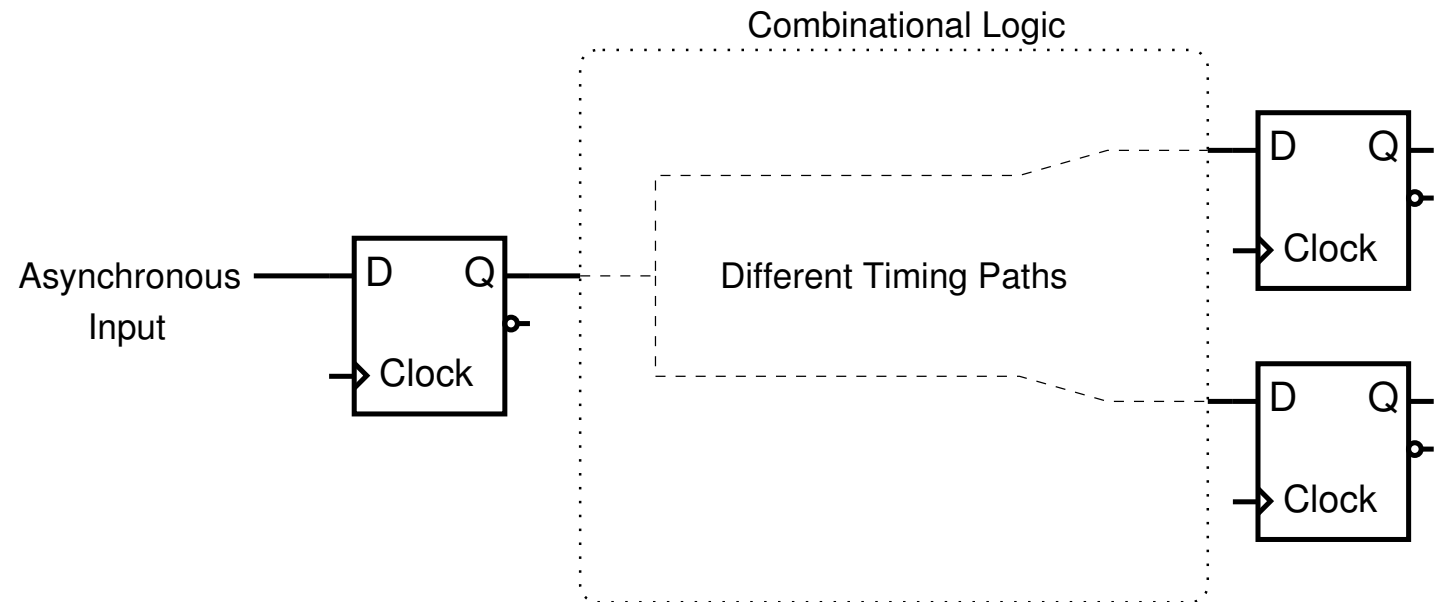
Asynchronous Inputs



Retiming the asynchronous input before the combinational logic block should give more predictable results.

Synchronous Systems

Asynchronous Inputs



To avoid a setup violation¹:

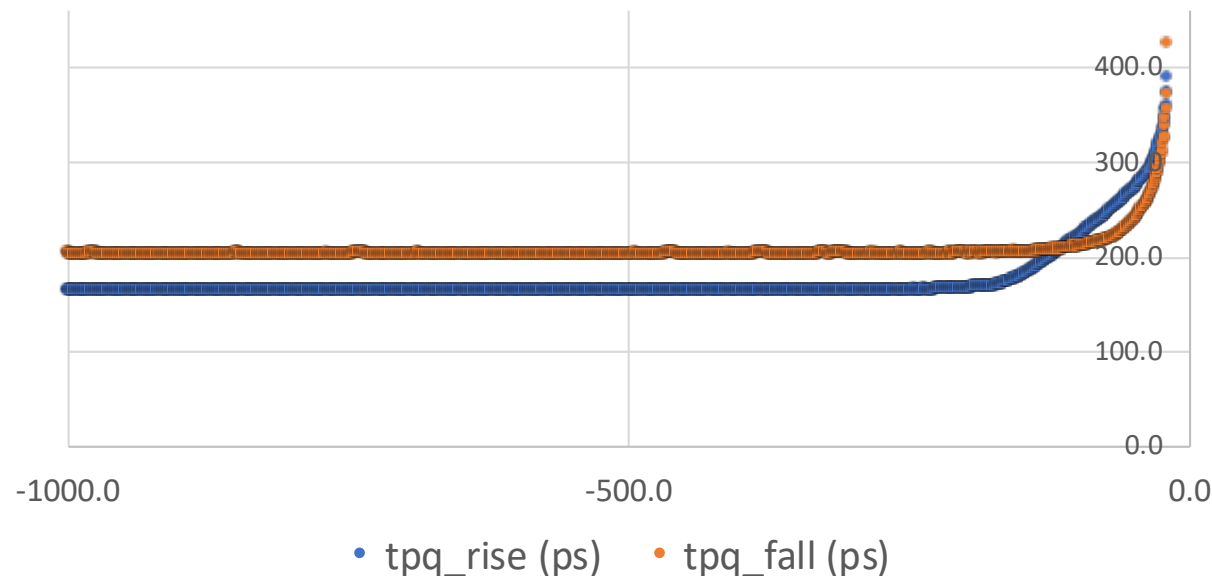
$$ClockPeriod > t_{pQ} + t_{critical_path} + t_{setup}$$

but t_{pQ} may now be unpredictable

¹assuming ideal clock

Synchronous Systems

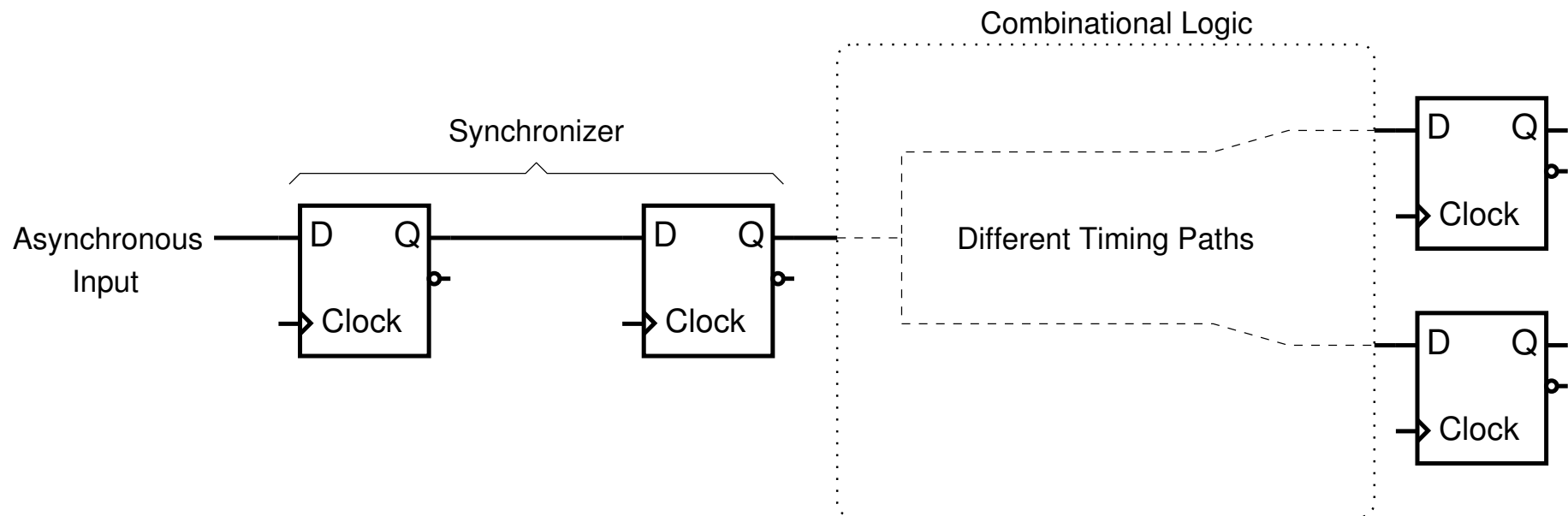
t_{pQ} Variation with Late Arriving Data



- As the setup time (t_{setup}) is reduced (close to its absolute minimum value), the clock-to-Q delay (t_{pQ}) increases sharply.
- A flip-flop datasheet will quote a t_{pQ} value for a minimum t_{setup} value. When we violate the minimum specified t_{setup} value, the quoted t_{pQ} value is no longer valid.

Synchronous Systems

Asynchronous Inputs



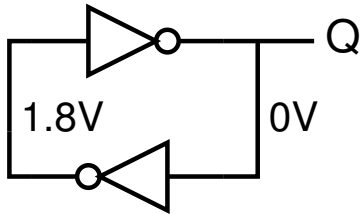
A second flip-flop in the synchronizer gives a predictable t_{pQ} for our equation:

$$ClockPeriod > t_{pQ} + t_{critical_path} + t_{setup}$$

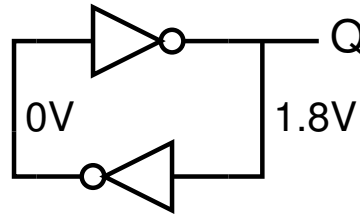
Synchronous Systems

Flip-Flop Stable States

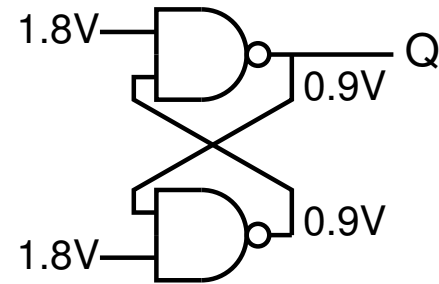
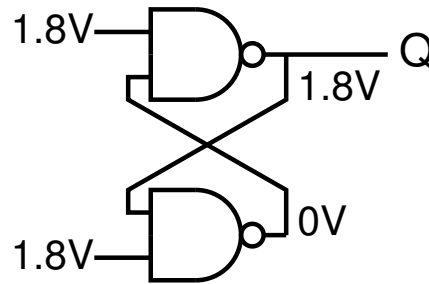
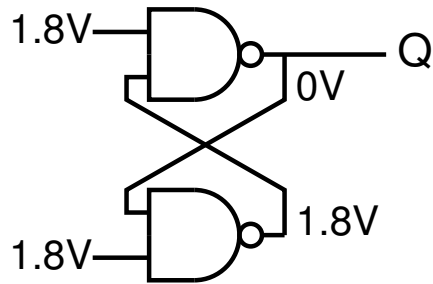
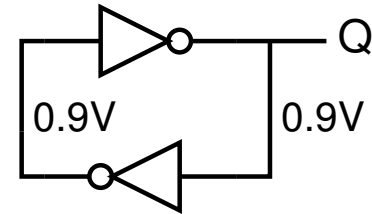
Q=0



Q=1



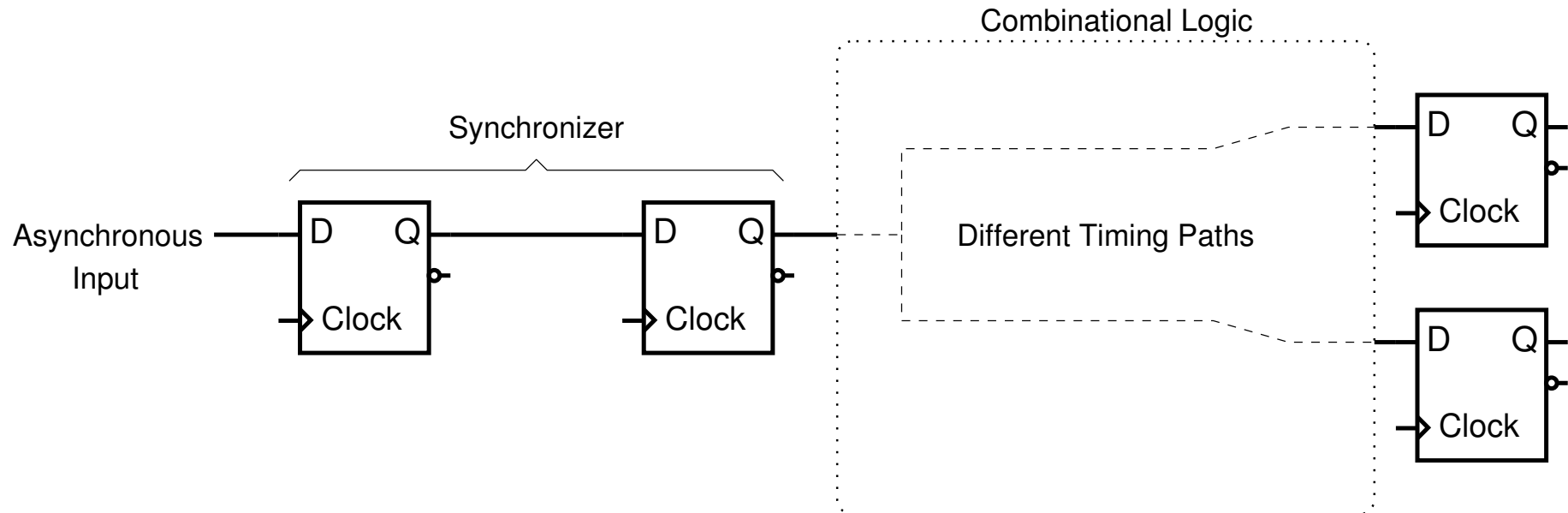
Q=?



The third state is described as *metastable* since a slight perturbation in one of the 50%-of- V_{DD} voltages will result in a move to one of the other states.

Synchronous Systems

Metastability



- The first flip-flop in our synchronizer may go metastable in the extreme case where the set-up time for D is reduced and t_{pQ} increases.
- The two flip-flop synchronizer gives a full clock cycle for the metastable state to resolve itself into one or other normal state.

Summary