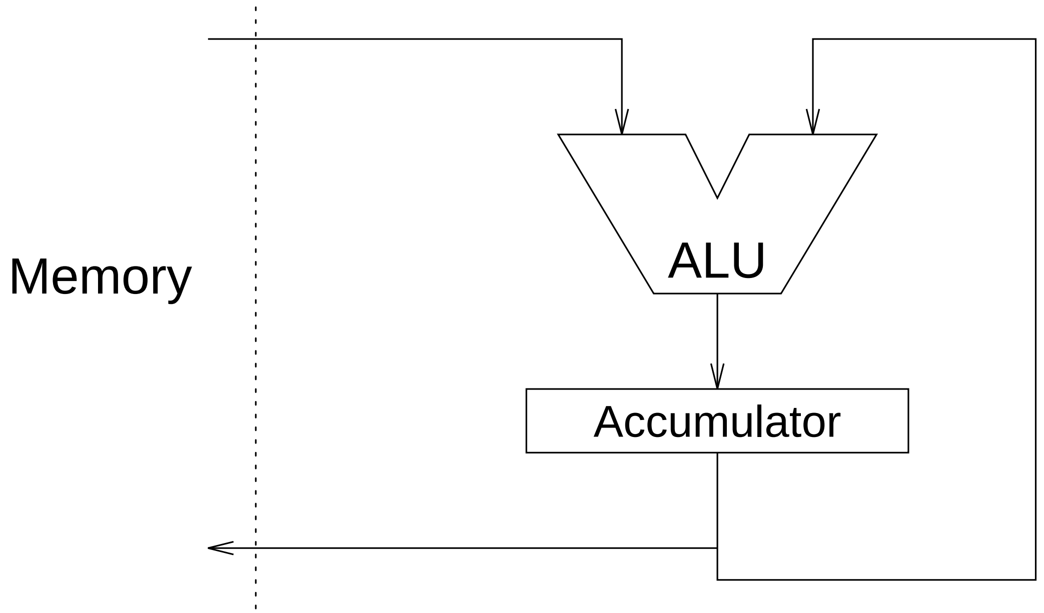
Architecture

Simple architecture

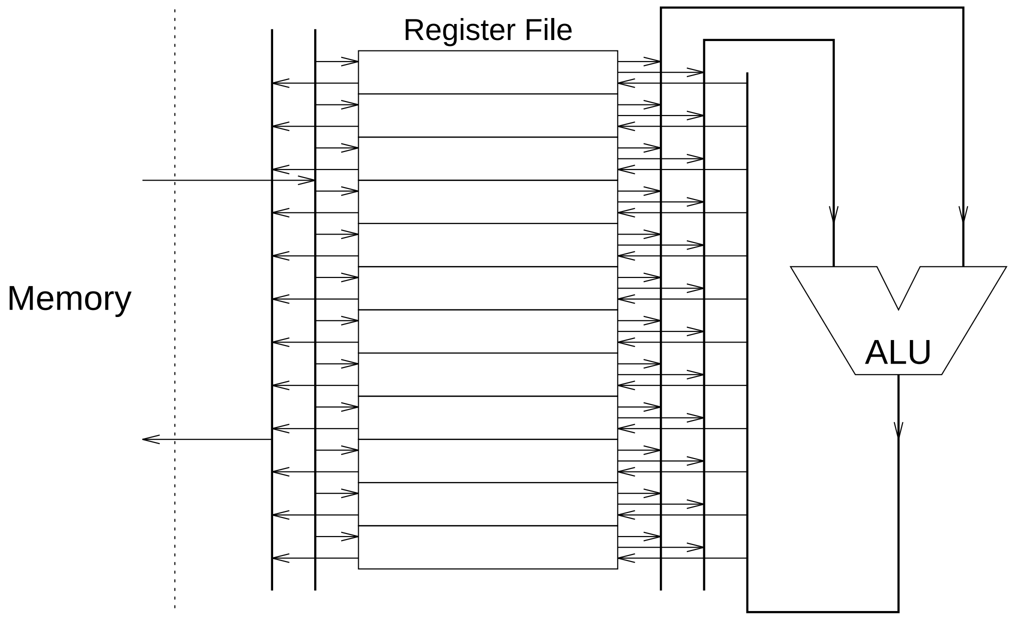


- Register / Memory architecture[1]:
  - `ADD 123` Acc ← Acc + Mem[123]

[1] a.k.a. Single address architecture.

Architecture

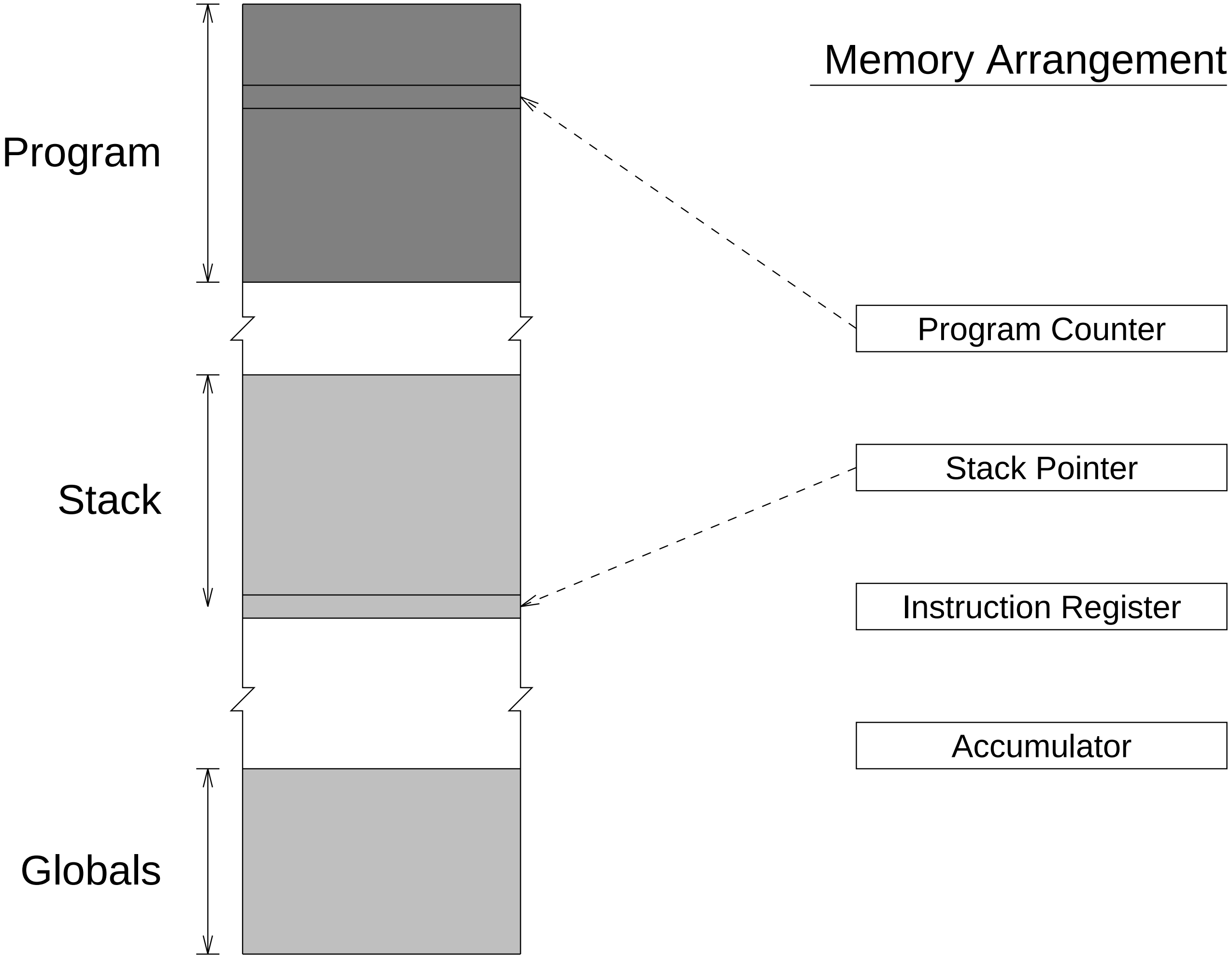
Memory access is slow – use more registers.



- Register / Register architecture[2]:
  - `ADD B,F,D` regD ← regB + regF

[2] a.k.a. Three address architecture.

Architecture



Architecture

Address Registers and Addressing Modes

- Program Counter
  - `IR` $\leftarrow$ `(PC), PC` $\leftarrow$ `PC + 1`

- Stack Pointer
  - `PSHS B`   `SP`$\Downarrow$ `B`   `SP` $\leftarrow$ `SP - 1, (SP)` $\leftarrow$ `regB`[3]
  - `PULS B`   `SP`$\Uparrow$ `B`   `regB` $\leftarrow$ `(SP), SP` $\leftarrow$ `SP + 1`

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[3] note that stack is upsidedown

Architecture

- Index Register
  - `STA 3,X`   `(regX + 3)` $\leftarrow$ `regA`
  - `STA ,X`   `(regX)` $\leftarrow$ `regA`
  - `LDA Y,X`   `regA` $\leftarrow$ `(regX + regY)`
  - `LDB +3,SP`   `regB` $\leftarrow$ `(SP + 3)`

- General Purpose Registers

  In many modern machines the registers are general purpose, any register may be used as a stack pointer or index register as well as a data register.

Calls and Context

- Call Subroutine
  - `JSR 1234`

$$\texttt{SP}\Downarrow \texttt{PC}$$
$$\texttt{PC} \leftarrow \texttt{1234}$$

- Return
  - `RTS`

$$\texttt{SP}\Uparrow \texttt{PC}$$

The processor will automatically store the PC value (return address) on the stack.

Calls and Context

Other local values may be stored automatically or explicitly.

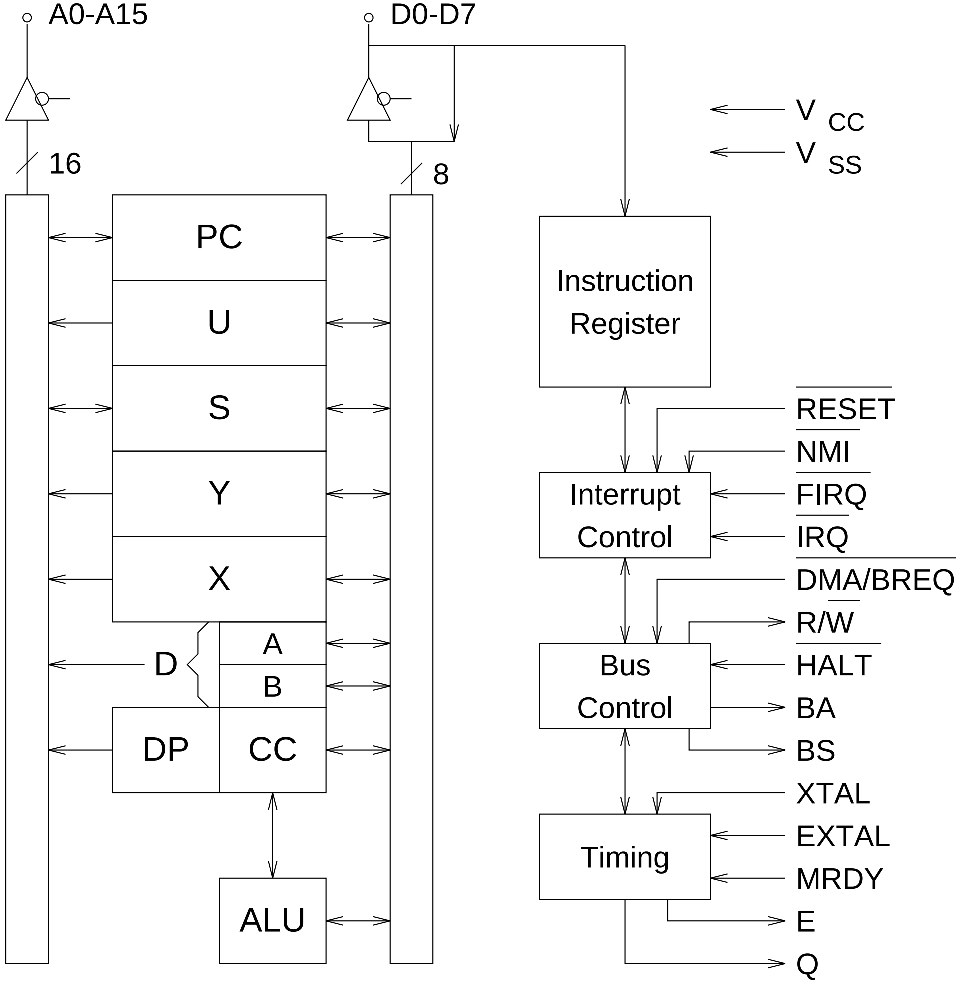
- Context saved by calling routine

```
   .
   .
   .
PSHS A,Y        1234:   .
JSR 1234                .
PULS Y,A                .
   .                    .
   .                    RTS
   .
```

- Context saved by subroutine

```
   .
   .
   .            1234:   PSHS A,B,X
JSR 1234                .
   .                    .
   .                    .
   .                    PULS X,B,A
                        RTS
```

6809 Architecture



MC6809 Expanded Block Diagram

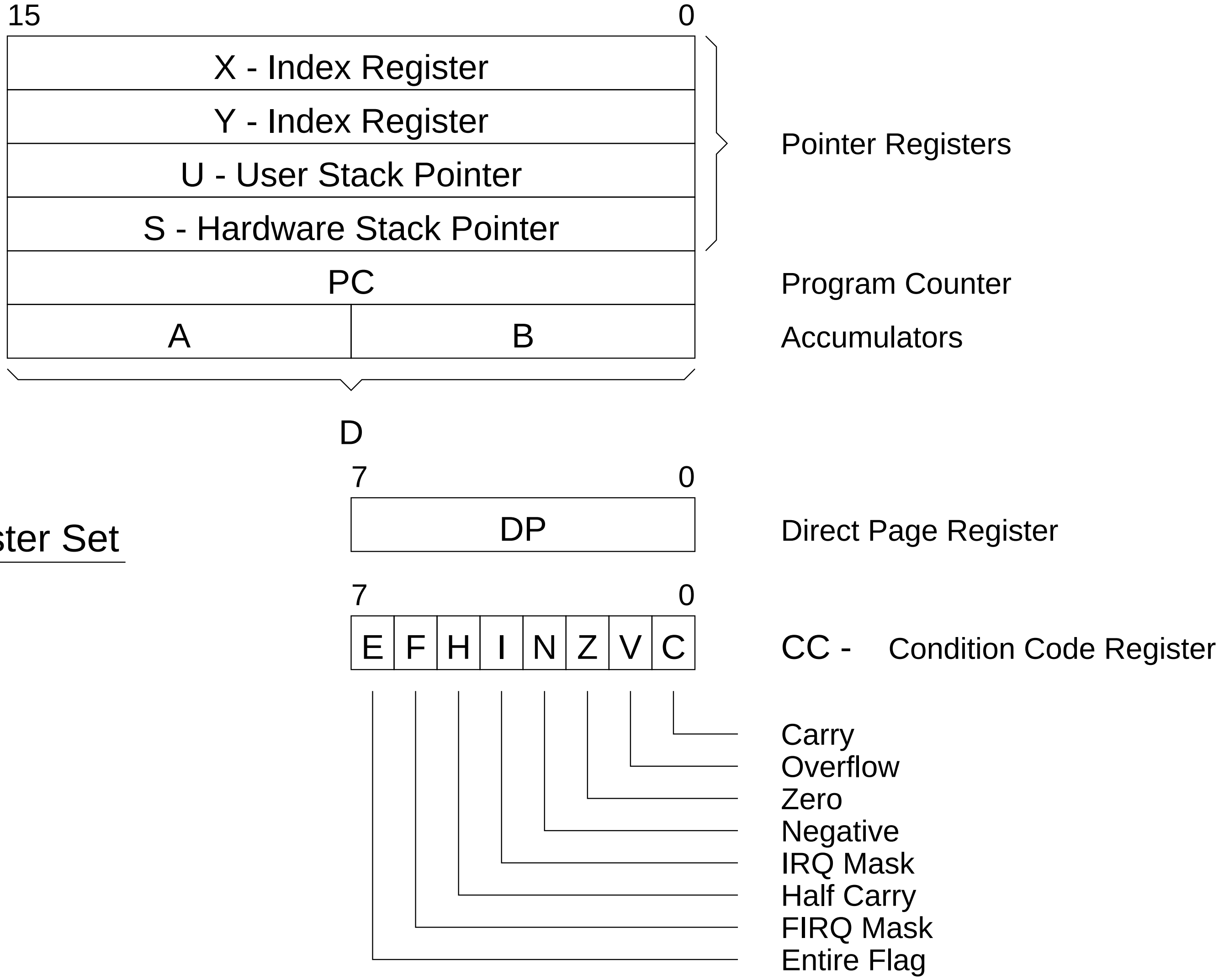
6809 Architecture

- Simple μP
- 8 bit Data Bus (mixed 8/16 bit internal architecture).
- 16 bit Address Bus.
- Registers

  The 6809 has a number of special purpose registers to support a variety of addressing modes.

  - A & B registers combine as 16 bit D register.
  - Two stack pointers; S, U.
  - Two index registers; X, Y.
  - Direct Page register, DP, nominates one page for local addressing.
  - Condition Code register, CC, contains 8 status and control bits for the processor.

6809 Architecture



MC6809 Register Set