Near-Capacity Three-Stage MMSE Turbo Equalization Using Irregular Convolutional Codes

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Abstract

Traditional Turbo EQualization (TEQ) schemes suffer from residual bit errors due to the non-recursive nature of the channel imposing Inter-Symbol-Interference (ISI). The performance of the traditional TEQ scheme may, however, be improved if an intermediate recursive channel codec is invoked, which results in a three-stage serially concatenated system. This intermediate code is necessary, especially when the inner module cannot be rendered recursive, for example, when a Minimum Mean Square Error (MMSE) equalizer is invoked. Our EXtrinsic Information Transfer (EXIT) chart analysis explicitly explains the performance gain, and based on this explanation IRregular Convolutional Codes (IRCCs) are constructed to be used as the outer code for the sake of achieving near capacity performance. Furthermore, the proposed analysis and design procedure may be applied in the context of diverse iterative receivers employing multiple soft-in/soft-out (SISO) modules.

1 Introduction

It is widely recognized that in a serially concatenated code employing iterative decoding the inner code should be recursive in order to maximize the interleaver gain [1]. This rule may be generalized to diverse serially concatenated systems. For example, in the classic turbo equalization scheme [2], the dispersive channel may be viewed as a specific non-recursive convolutional encoder and the APP-based channel equalizer may be regarded as the corresponding non-recursive convolutional decoder, which hence limits the overall performance. When a simple unity-rate recursive precoder is incorporated at the transmitter, which renders the channel to appear recursive to the receiver, the attainable performance may be further improved [3], [4]. In this case, the precoder's feedback shift-register model may be combined with the feedforward shift-register model of the dispersive channel, resulting in a single recursive shift-register model. Based on this model, a so-called super-trellis of the joint precoder and dispersive channel can be constructed. Then the APP equalizer may be used for simultaneously performing both decoding and equalization. Hence no separate decoder is required for the precoder and the receiver remains a two-stage scheme. Similar schemes, invoking trellis-based APP equalizers were studied in [7], where the author inferred that three-stage concatenated schemes do not achieve any additional performance gain compared to suitably designed two-stage systems employing precoders, provided that the decoders can be chosen without any constraints.

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However, not all inner modules of serially concatenated schemes can be rendered recursive. For example, if a soft-in/soft-out (SISO) Minimum Mean Square Error (MMSE) equalizer [5], [6] is invoked instead of the trellis-based APP equalizer of [7] in a turbo equalization scheme [2], the super-trellis model cannot be adopted for the MMSE equalizer, since the structure of the latter is not trellis-based. For these scenarios the three-stage concatenated schemes considered in this contribution may have to be used. To be specific, at the transmitter an additional interleaver is needed to separate the recursive "precoder" and the channel, while at the receiver the inner MMSE equalizer, the intermediate channel decoder and the outer channel decoder constitute a three-stage serially concatenated system, which performs iterative equalization/decoding across the three components.

To elaborate a little further, the broad goal of this paper is to design three-stage concatenated schemes for the sake of achieving near-capacity performance. Our approach is based on EXIT chart analysis [8] and the underlying procedures are demonstrated using the design example of a three-stage MMSE turbo equalization scheme. Specifically, IRregular Convolutional Codes (IRCCs) [9], [10] are constructed, which are used as the outer code for the sake of solving the EXIT curve fitting problem of [11], i.e. that of minimizing the width of the EXIT chart tunnel and hence the system becomes capable of approaching the achievable capacity.

The outline of the paper is as follows. Our system model is outlined in Section 2. The system's convergence behaviour is analyzed in Section 3 with the aid of 3D EXIT charts and their 2D projections. Section

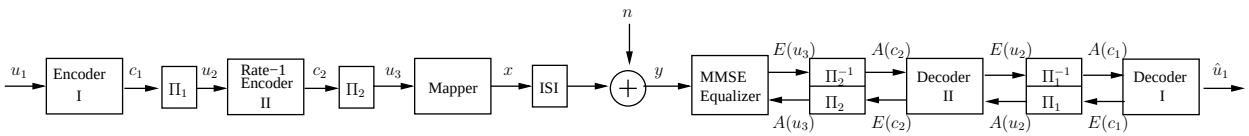


Fig. 1. System diagram of two serially concatenated channel codes and MMSE equalization.

4 describes the design procedure of IRCCs, while our simulation results are presented in Section 5. Section 6 concludes the paper.

2 System Model

Fig. 1 shows the system model of a three-stage serial concatenation scheme[1] . At the transmitter, a block of K information bits u_1 is encoded by channel Encoder I first. Then the outer encoded bits c_1 are interleaved yielding the permuted bits u_2, which are fed through the rate-1 Encoder II. The resultant double-encoded bits c_2 are interleaved by a second interleaver, yielding the interleaved bits u_3, which are fed to a bit-to-modulated-symbol mapper, as seen in Fig. 1. After mapping, the modulated signal x is transmitted over a dispersive channel contaminated by the AWGN n. At the receiver of Fig. 1, an iterative equalization/decoding structure is employed, where extrinsic information is exchanged between the three SISO modules, namely the MMSE equalizer, APP-based Decoder II and APP-based Decoder I in a number of consecutive iterations. To be specific, in Fig. 1, $A(\cdot)$ denotes *a priori* information represented in terms of Log-Likelihood Ratios (LLRs), while $E(\cdot)$ denotes *extrinsic* information also expressed in terms of LLRs. Note that Decoder II processes two *a priori* inputs arriving from both the MMSE equalizer and Decoder I and generates two *extrinsic* outputs as well, which is not encountered in a traditional two-stage turbo equalization scheme.Following the last iteration, the estimates $\hat{u}_1$ of the original bits are generated by Decoder I, as seen in Fig. 1.

In our forthcoming EXIT chart analysis and in the Monte Carlo simulations, we assume that the channel is time-invariant and that the Channel Impulse Response (CIR) is known at the receiver. For the sake of simplicity, BPSK modulation is used.

3 EXIT Chart Analysis

Following the approach of [12], [13], we now carry out the EXIT chart analysis of the three-stage concatenated system of Fig. 1. Consider a half-rate Recursive Systematic Convolutional (RSC) code as Encoder I, a simple rate-1 accumulator as Encoder II, described by the generator polynomials of (2/3) in Proakis' octal form (i.e. $1/(1+D)$), where 3 represents the feedback polynomial. Moreover, the ISI channel used is a simple three-path channel adopted from [14] having the CIR of $h[n] = 0.407\delta[n] + 0.815\delta[n-1] + 0.407\delta[n-2]$.

Let $I_{A(x)}$ denote the mutual information (MI) [15] between the *a priori* value $A(x)$ and the symbol x. And let $I_{E(x)}$ denote the MI between the *extrinsic* value $E(x)$ and the symbol x. As seen from Fig. 1, Decoder II has two *extrinsic* MI outputs, namely $I_{E(u_2)}$ and $I_{E(c_2)}$, both of which are functions of the *a priori* MI inputs, namely $I_{A(u_2)}$ and $I_{A(c_2)}$. The two EXIT functions [8], [13] are defined by

$$I_{E(u_2)} = T_{u_2}(I_{A(u_2)}, I_{A(c_2)}), \quad (1)$$

$$I_{E(c_2)} = T_{c_2}(I_{A(u_2)}, I_{A(c_2)}). \quad (2)$$

By contrast, for the MMSE equalizer and Decoder I, only one a *priori* input is available in Fig. 1 and the corresponding EXIT functions are:

$$I_{E(u_3)} = T_{u_3}(I_{A(u_3)}, E_b/N_0) \quad (3)$$

for the equalizer and

$$I_{E(c_1)} = T_{c_1}(I_{A(c_1)}) \quad (4)$$

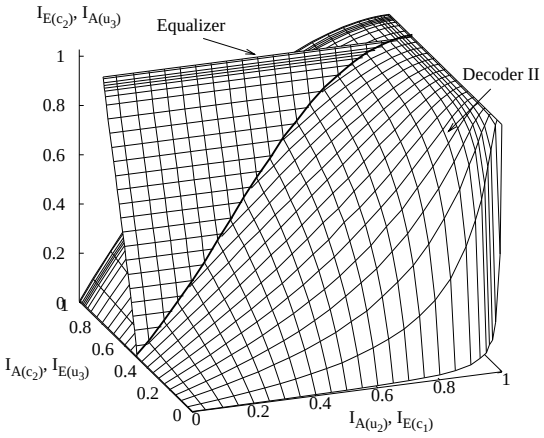
for Decoder I. Hence two 3D EXIT charts are required for plotting all the EXIT functions, namely one for the EXIT functions of Eq. (2) and Eq. (3) as shown in Fig. 2(a), and another for the EXIT functions of Eq. (1) and Eq. (4), as shown in Fig. 2(b).

The intersection of the surfaces seen in Fig. 2(a) characterizes the best possible attainable performance when exchanging information between the equalizer and Decoder II of Fig. 1 for different fixed values of $I_{A(u_2)}$, which is shown as a thick solid line. For each point ($I_{A(u_2)}$, $I_{A(c_2)}$, $I_{E(c_2)}$) of this line in the 3D space of Fig. 2(a), there is a specific value of $I_{E(u_2)}$ determined by $I_{A(u_2)}$ and $I_{A(c_2)}$ according to the EXIT function of Eq. (1). Therefore the solid line on the surface of the EXIT function of Decoder II seen in Fig. 2(a) is mapped to the solid line shown in Fig. 2(b). In order to avoid the cumbersome 3D representation, we now project the bold EXIT curve of Fig. 2(b) onto the 2D plane at $I_{A(c_2)} = 0$, yielding the dotted line denoted with circles in Fig. 2(c). Let us describe this projected EXIT curve as:

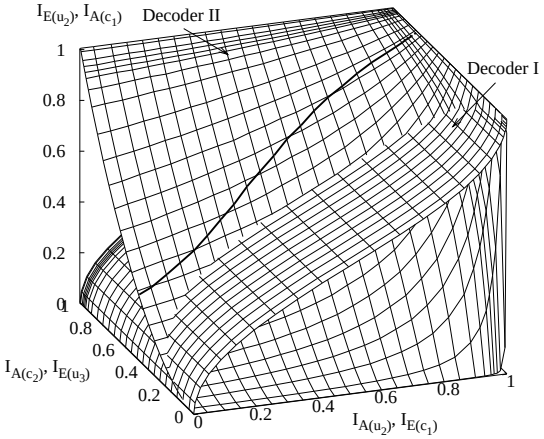
$$I_{E(u_2)} = T^p_{u_2}(I_{A(u_2)}, E_b/N_0). \quad (5)$$

This projected EXIT curve is useful in determining the convergence threshold of the three-stage decoded

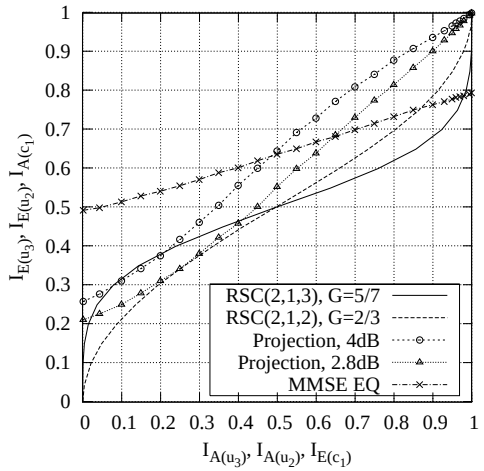
[1]If an APP equalizer is invoked, the (de-)interleaver pair Π_2^{-1} and Π_2 as well as Decoder II of the receiver and the interleaver Π_2 of the transmitter are not needed. Hence we have a two-stage serially concatenated scheme.



(a) Decoder II and the equalizer at $E_b/N_0 = 4$dB



(b) Decoder II and Decoder I



(c) All three SISO modules at $E_b/N_0 = 4$dB

Fig. 2. EXIT charts for the three-stage SISO system.

system. For more details on this 3D-to-2D projection operation, please refer to [12], [13].

The EXIT curves of the MMSE equalizer and Decoder I are also shown in Fig. 2(c), where the classic maximum free-distance RSC(2,1,3) code [14] having the octal generator polynomials of (5/7) was first used. It can be seen that the projected EXIT curve intersects with that of the RSC(2,1,3) code at $E_b/N_0 = 4$ dB. To be specific, the E_b/N_0 convergence threshold is approximately 4.1 dB for this system setup. Other RSC codes having different constraint lengths and generator polynomials were also searched, and the RSC(2,1,2) code having the octal generator polynomials of (2/3) was found to offer a lower convergence threshold of about 2.8 dB, despite its lower complexity. The EXIT function of this RSC(2,1,2) code is also shown in Fig. 2(c).

As for a traditional two-stage turbo equalization scheme, the EXIT curve of the MMSE equalizer and that of the outer code are used for analyzing the associated convergence behaviour. As seen from Fig. 2(c), the EXIT curve of the MMSE equalizer cannot reach the convergence point of (1,1) and intersects with the EXIT curve of the outer RSC code, which implies that residual errors persist, regardless of both the number of iterations used and the size of the interleaver. This explains the Bit-Error Rate (BER) performance bound of the traditional two-stage turbo equalization scheme [2], [5], [6]. On the other hand, if the inner MMSE equalizer and the intermediate decoder are viewed as one joint inner SISO module, then the projected EXIT function of Eq. (5) is the EXIT function of this module, which is capable of reaching the convergence point of (1,1). As long as there is an open tunnel between the EXIT curve of this joint inner module and that of the outer decoder, the three-stage concatenated system is capable of converging, achieving infinitesimally BERs.

Let us now elaborate on the desired features of beneficial EXIT characteristics and on how they can be designed for the sake of matching those of the other components in the system. According to the area properties [11] of the EXIT charts, the area under the EXIT curve of the inner MMSE equalizer is approximately equal to the channel capacity attained, when the channel's input is uniformly distributed. Furthermore, the area under the EXIT curve of the outer code is approximately equal to (1-R_I), where R_I is the outer code rate. Although these properties were only proven for the family of binary erasure channels (BECs) [11], they have been observed to hold for AWGN and ISI channels [7], [10], too. More explicitly, let A_I and $\bar{A}_I$ be the areas under $T_{c_1}(i)$ and its inverse $T_{c_1}^{-1}(i)$, $i \in [0, 1]$, respectively, which are expressed as:

$$A_I = \int_0^1 T_{c_1}(i)\mathrm{d}i, \quad \bar{A}_I = \int_0^1 T_{c_1}^{-1}(i)\mathrm{d}i = 1 - A_I. \tag{6}$$

Similarly, we define the areas A_{II} and $\bar{A}_{II}$ for $T_{u_2}^{p}(i)$,

A_{III} and $\bar{A}_{III}$ for $T_{u_3}(i)$. Then we have,

$$\bar{A}_I \approx R_I, \tag{7}$$

and for BPSK modulation

$$A_{III} \approx C_{UI}, \tag{8}$$

where C_{UI} is the uniform-input capacity of the communication channel in Fig. 1. Since the intermediate code has unity rate, the area under the projected EXIT curve A_{II} is also approximately equal to the above-mentioned uniform-input channel capacity C_{UI}. As seen from Fig. 2(c), even if the RSC(2,1,2) code is invoked, there is space between the projected EXIT curve and the EXIT curve of the outer RSC code at the convergence threshold of $E_b/N_0 = 2.8$ dB, i.e., $A_{II} - \bar{A}_I > 0$, which means the channel capacity cannot be reached. More explicitly, the area under the projected EXIT curve at $E_b/N_0 = 2.8$ dB is $A_{II} \approx 0.56$, which is larger than the outer code rate of $R_I = 0.5$. Therefore a lower E_b/N_0 convergence threshold may be attained, provided that the EXIT curve of the outer code matches the projected EXIT curve more closely. An IRCC [9], [10] constitutes a code that exhibits flexible EXIT characteristics, which can be optimized to match the projected EXIT curve, in order to create an appropriately shaped EXIT-chart convergence tunnel.

4 Design of Irregular Convolutional Codes

Tüchler and Hagenauer [9], [10] proposed the employment of IRCCs, which are constituted by a family of convolutional codes having different code rates. They were specifically designed with the aid of EXIT charts [8], for the sake of improving the convergence behaviour of iteratively decoded systems. To be specific, an IRCC is constructed from a family of P subcodes. First, a rate-r convolutional mother code C_1 is selected and the $(P-1)$ other subcodes C_k of rate $r_k > r$ are obtained by puncturing. Let L denote the total number of encoded bits generated from the K uncoded information bits. Each subcode encodes a fraction of $\alpha_k r_k L$ of the original uncoded information bits and generates $\alpha_k L$ encoded bits. Given the target overall average code rate of $R \in [0,1]$, the weighting coefficient α_k has to satisfy:

$$1 = \sum_{k=1}^{P} \alpha_k, \; R = \sum_{k=1}^{P} \alpha_k r_k, \text{ and } \alpha_k \in [0,1], \; \forall k. \tag{9}$$

Clearly, the individual code rates r_k and the weighting coefficients α_k play a crucial role in shaping the EXIT function of the resultant IRCC. For example, in [10] a family of $P = 17$ subcodes were constructed from a systematic, rate-1/2, memory-4 mother code defined by the generator polynomial $(1, g_1/g_0)$, where $g_0 = 1 + D + D^4$ is the feedback polynomial and $g_1 = 1 + D^2 + D^3 + D^4$ is the feedforward one. Higher code rates may be obtained by puncturing, while lower rates are created by adding more generators and by puncturing under the constraint of maximizing the achievable free distance. The two additional generators used are $g_2 = 1 + D + D^2 + D^4$ and $g_3 = 1 + D + D^3 + D^4$. The resultant 17 subcodes have coding rates spanning from $0.1, 0.15, 0.2, \cdots$, to 0.9.

The IRCC constructed using this procedure has the advantage that the decoding of all subcodes may be performed using the same mother code trellis, except that at the beginning of each block of $\alpha_k r_k L$ number of trellis transitions/sections corresponding to the subcode C_k, the puncturing pattern has to be restarted. Trellis termination is necessary only after all of the K uncoded information bits have been encoded.

The EXIT function of an IRCC can be obtained from those of its subcodes. Denote the EXIT function of the subcode k as $T_{c_1,k}(I_{A(c_1)})$. Assuming that the trellis segments of the subcodes do not significantly interfere with each other, which might change the associated transfer characteristics, the EXIT function $T_{c_1}(I_{A(c_1)})$ of the target IRCC is the weighted superposition of the EXIT function $T_{c_1,k}(I_{A(c_1)})$ [10], yielding,

$$T_{c_1}(I_{A(c_1)}) = \sum_{k=1}^{P} \alpha_k T_{c_1,k}(I_{A(c_1)}). \tag{10}$$

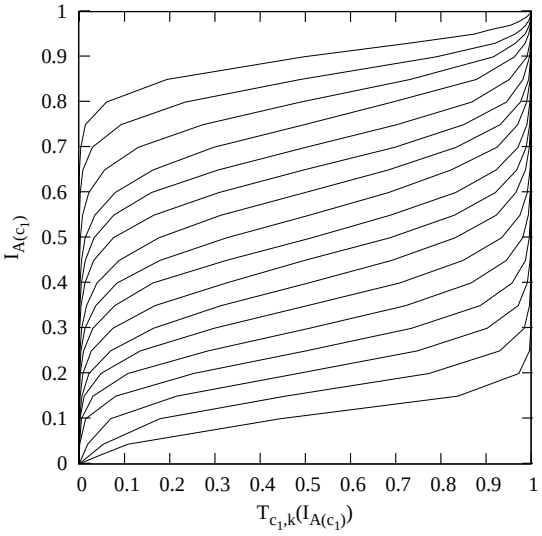


Fig. 3. EXIT functions of the 17 subcodes in [10].

For example, the EXIT functions of the 17 subcodes used in [10] are shown in Fig. 3. We now optimize the weighting coefficients, $\{\alpha_k\}$, so that the IRCC's EXIT curve of Eq. (10) matches the projected EXIT curve of Eq. (5). The area under the projected EXIT curve of Eq. (5) at $E_b/N_0 = 1.8$ dB is $A_{II} \approx 0.51$, which indicates that this E_b/N_0 value is close to the lowest possible convergence threshold for a system having an

outer coding rate of $R_I = 0.5$. We optimize $T_{c_1}(I_{A(c_1)})$ of Eq. (10) at $E_b/N_0 = 1.8$ dB by minimizing the square of the error function

$$e(i) = [T^p_{u_2}(i, E_b/N_0) - T^{-1}_{c_1}(i)] \quad (11)$$

subject to the constraints of (9) and $e(i) > 0$ over all i:

$$J(\alpha_1, \cdots, \alpha_P) = \int_0^1 e(i)^2 \mathrm{d}i, \quad e(i) > 0, \forall i \in [0, 1]. \quad (12)$$

In tangible physical terms we minimize the area between the projected EXIT curve and the EXIT curve of the outer code as seen in Fig. 2(c). This results in a good match between the two curves, ultimately leading to a narrow EXIT-chart tunnel, which implies a near-capacity operation attained at the cost of a potentially high number of decoding iterations. The associated high complexity is characteristic of schemes operating beyond the Shannonian cut-off rate. In order to solve the curve-fitting problem portrayed in Eq. (12), an iterative solution was proposed in [9]. With the aid of this algorithm [9], the optimized weighting coefficients are obtained as:

$$\begin{aligned}[\alpha_1, \cdots, \alpha_{17}] \quad = \quad & [0\ 0\ 0\ 0.317294\ 0.04734\ 0 \\ & 0.0530961\ 0.0934305\ 0.113418\ 0\ 0 \\ & 0.0951124\ 0.129086\ 0.0118142 \\ & 0\ 0\ 0.138448]. \end{aligned} \quad (13)$$

The resultant EXIT curve of the optimized IRCC is shown in Fig. 4.

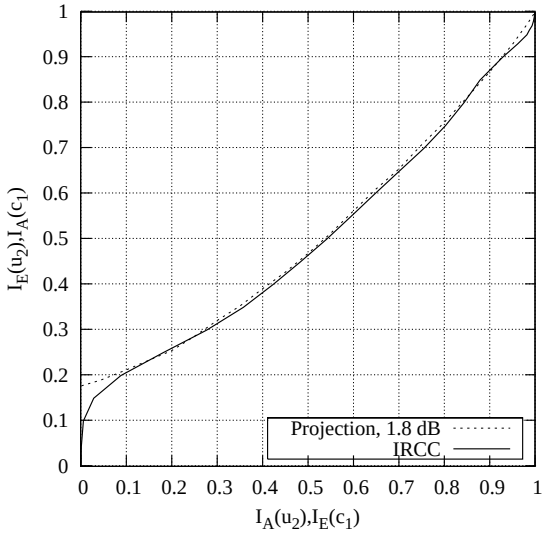


Fig. 4. The projected EXIT curve of Eq (5) and the EXIT function of the optimized IRCC at $E_b/N_0 = 1.8$ dB.

5 Simulation Results

Monte Carlo simulations were performed for characterizing both the IRCC design of Section 4 and the convergence predictions of Section 3. As our benchmarker scheme, the RSC(2,1,2) code having octal generator polynomials of (2/3) is employed as Encoder I of Fig. 1. As our proposed scheme, the IRCC designed in Section 4 is used as Encoder I. The rest of the system components are the same for both schemes and all the system parameters are listed in Table I. Fig. 5 depicts the BER performances of both schemes. Also shown

TABLE I
SYSTEM PARAMETERS

Encoder I	Half-rate RSC code or Half-rate IRCC
Encoder II	Generator Polynomials 1/3
Modulation	BPSK
CIR	$[\mathbf{0.407\ 0.815\ 0.407}]^T$
Block Length	K = 10 000 bits
Overall Coding Rate	0.5

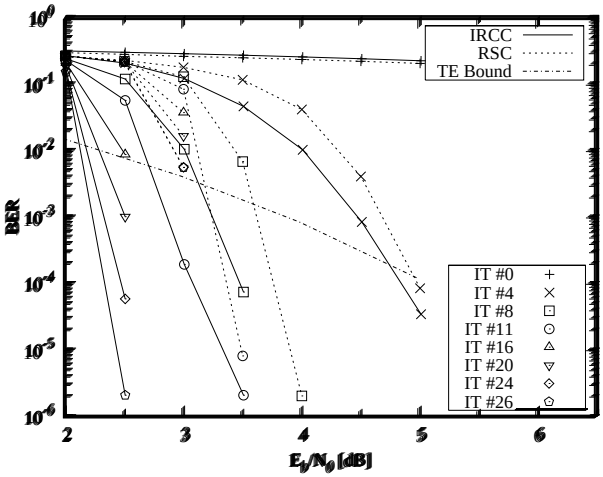


Fig. 5. BER performances for three-stage serial concatenation schemes using both regular RSC code and IRCC.

in Fig. 5 is the performance bound for a traditional two-stage turbo equalization scheme using a RSC(2,1,3) code having the octal generator polynomials of (5/7) as the outer code. It can be seen from Fig. 5 that both three-stage serially concatenated schemes are capable of outperforming the traditional two-stage turbo equalization scheme. Furthermore, the three-stage scheme employing an IRCC is capable of achieving a BER of 10^{-5} at about $E_b/N_0 = 2.5$ dB, while the three-stage scheme using a regular RSC code achieves a similar BER at about $E_b/N_0 = 3.5$ dB. Hence, an approximately 1 dB E_b/N_0 gain is achieved by using the optimized IRCC. Note that owing to the limited interleaver size, both schemes fall short of converging at the thresholds predicted by the EXIT chart analysis, which are 1.8 dB and 2.8 dB, respectively.

The decoding trajectory recorded during our Monte Carlo simulations using the optimized IRCC is depicted in Fig. 6. It can be seen that the recorded

trajectory matches the EXIT chart prediction quite closely. Furthermore, since the tunnel between the two EXIT curves is very narrow, a significant number of iterations are required for enabling the iterative receiver to converge at the point of (1,1). When approaching the channel capacity, the tunnel becomes even narrower, therefore more iterations will be needed, resulting in a drastically increased complexity. At the same time, even longer interleavers will be required to ensure that the soft information exchanged between the SISO modules is uncorrelated, so that the trajectory will follow the EXIT curves. This is another manifestation of Shannon's channel capacity theorem [15].

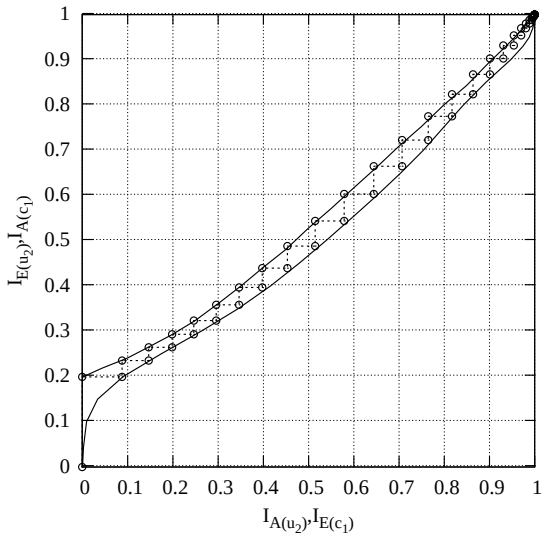


Fig. 6. EXIT charts and recorded decoding trajectory for the three-stage system using IRCC at $E_b/N_0 = 2.5$ dB.

6 Conclusion

We advocate three-stage serial concatenated schemes when the inner SISO module cannot be rendered recursive. The advocated system design principle was exemplified by an iterative three-stage MMSE equalization scheme, where the iterative receiver was constituted by three SISO modules, namely the inner MMSE equalizer, the intermediate channel decoder and the outer channel decoder. Furthermore, the convergence behaviour of our design example was analyzed using 3D EXIT charts and their 2D projections. It has been pointed out that although the EXIT function of the inner MMSE equalizer cannot reach the convergence point of (1,1), the joint EXIT function (obtained by projection) of the inner MMSE equalizer and the intermediate channel decoder can. Therefore the three-stage system is capable of eliminating the residual BER encountered in the conventional two-stage system [5], [6]. With the advent of 2D projection, an IRCC was constructed to be used as the outer code whose EXIT function was matched to the joint EXIT function, and, as a result, the channel capacity may be closely approached.

Furthermore, the analysis and design procedure advocated here may be applied in the context of diverse iterative receivers, employing multiple SISO modules, such as the jointly designed source coding and space-time coded modulation schemes of [16], [17]. The design of further such systems constitutes our future research.

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